

RZ/T2N Group

RZ/T2N Evaluation Board Manual

RZ/T Series for Real-Time Control

RZ Family

64-Bit & 32-Bit Arm[®]-Based High-End MPUs

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(Rev.5.0-1 October 2020)

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TOYOSU FORESIA, 3-2-24 Toyosu,
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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This product is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the equipment.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that which the receiver is connected.
- Power down the equipment when not in use.
- Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

- The user is advised that mobile phones should not be used within 10 m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Evaluation Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

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How to Use This Manual

1. Purpose and Target Readers

The intention of this manual is to assist users in understanding the hardware functionality and electrical characteristics of the evaluation board in overview. The target users of this manual are engineers designing sample code that runs on the platform of the evaluation board, with the use of various peripheral devices.

Though this manual includes an overview of the functionality of the evaluation board, it is not intended to be a guide for embedded programming or hardware design.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Handling Precautions section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/T2N Evaluation Board. Be sure to refer to the latest versions of these documents. The newest versions of the listed documents are available on the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Board manual	Explanation of the hardware specifications of the evaluation board	RZ/T2N Evaluation Board Manual	R20UT5574EJ0100 (this manual)
Quick start guide	Explanation of the flow from turning on the power to confirming initial operation	RZ/T2N Evaluation Board Quick Start Guide	R20QS0099EJ
Hardware manual	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and descriptions of operation	RZ/T2N Group Hardware Manual	R01UH1084EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
bps	bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
DIP	Dual In-line Package
DNF	Do Not Fit
EEPROM	Electrically Erasable Programmable Read Only Memory
ESC	EtherCAT Slave Controller
ESD	Electrostatic Discharge
EtherCAT	Ethernet for Control Automation Technology
GPT	General PWM Timer
I ² C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
J-Link™	SEGGER debug probe
J-Link™ OB	SEGGER On-board debug probe
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MAC	Media Access Control
MCU	Micro Controller Unit
MPU	Micro Processor Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not Applicable
n/c (NC)	Not Connected
OTG	On-The-Go
OTP	One-Time Programmable Memory
PC	Personal Computer
PCB	Printed Circuit Board
POE	Port Output Enable
POEG	Port Output Enable for GPT
PWM	Pulse Width Modulation
RAM	Random Access Memory
RGMII	Reduced Gigabit Media-Independent Interface
RMII	Reduced Media-Independent Interface
RMW	Renesas Motor Workbench
ROM	Read Only Memory
SCI	Serial Communications Interface
SEI	System Error Interrupt
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

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1. Overview

1.1 Purpose

This evaluation board (hereafter referred to as this board) is an evaluation tool for a Renesas microprocessor. This manual describes the technical elements of the hardware of this board in detail. The method for installing software and the debugging environment are explained in the quick start guide.

1.2 Features

This board has the following features.

- Programming of a Renesas microprocessor
- Debugging of user code
- User circuits for switches, LEDs, and potentiometers

This board is equipped with all of the circuits that are required for operating the microprocessor.

1.3 Board Specifications

Table 1-1 and Table 1-2 list the board specifications.

Table 1-1 Board Specifications (1)

Item	Specification
Microprocessor	Part No.: R9A07G076M48GBG
	Package: 537-pin FBGA
	On-chip memory: 2 Mbytes of RAM
On-board memory	OctaFlash: 512 Mbits
	QSPI serial flash memory: 128 Mbits
	I ² C EEPROM: 32 Kbits
	LPDDR4: 2 Gbytes
	eMMC: 32 Gbytes
	NAND flash memory: 1 Gbyte
Input clocks	RZ/T2N: 25 MHz
	PCIe: 25 MHz
	USB-to-serial conversion IC: 12 MHz
Power supplies	Power inputs: 15-V/3-A USB PD supporting USB Type-C® connector (J7) 24-V/8-A (Max.) bipolar terminal block (J10)
	Power-supply IC: 24-V input, 15-V output
	Power-supply IC: 15-V input, 12-V output (for PCIe)
	Power-supply IC: 15-V input, 5-V output
	Power-supply IC: 5-V input, 3.3-V output, 1.8-V output, 1.1-V output, 2.5-V output (for Ethernet PHY), 1.0-V output (for Ethernet PHY)
	Power-supply IC: 5-V input, 3.3-V output (for PCIe), 3.3-V output (for INV)
	Power-supply IC: 15-V input, 3.3-V output (for USB PD controller)
Debugging interfaces	MIPI-20: 1.27-mm pitch, 20-pin box header (J31)
	J-Link™ OB: USB Micro-B (J32)
Slide switch	Power-supply switch: Single-pole double-throw type × 1 (SW1)
DIP switches	Switches for mode setting: 4 poles × 1 (SW8), 10 poles × 1 (SW10)
	Switches for signal selection: 8 poles × 3 (SW7, SW9, and SW12), 10 poles × 2 (SW11 and SW13), 2 poles × 1 (SW14)
	Switch for the user: 4 poles × 1 (SW6)
Push switches	Reset switch × 1 (SW5)
	Switch for the user × 3 (SW2, SW3, and SW4)
Potentiometer (for A/D conversion)	10-kΩ single-turn type (R198)

Table 1-2 Board Specifications (2)

Item	Specification
LEDs	For the power supply: 15-V (yellow) × 1 (LED1), 3.3-V (green) × 1 (LED2)
	For the user: (green) × 2 (LED8 and LED9), (yellow) × 1 (LED10), (red) × 1 (LED11)
	Shared by the user and EtherCAT status: (green) × 4 (LED3, LED5, LED6, and LED7), (red) × 1 (LED4)
	For the Ethernet status: (green) × 5, (yellow) × 5 (built in to the RJ45)
Ethernet ports	For the J-Link™ OB status: (yellow) × 1 (LED12)
Ethernet ports	Connectors: RJ45 2 ports × 2 (J8 and J36), RJ45 1 port × 1 (J30)
	PHY: Single-channel PHY × 5
USB	USB host interface: USB Type-A (J2)
	USB function interface: USB Micro-B (J3)
	USB OTG interface: USB Micro-AB (J4)
CAN	Connector*: 2.54-mm pitch, 3 pins × 1 (J37)
	CAN transceiver × 1
RS485	Connector*: 10 pins × 1 (J38)
	RS485 transceiver × 1
USB-to-serial conversion interface	Connector: USB Micro-B (J33)
	Converter × 1
Pmod™	PMOD Type2A, 6A: 12-pin connector (J34)
	PMOD Type3A: 12-pin connector (J35)
Serial host interface	2.54-mm pitch, 14 pins × 1 (J45)*
SPI expansion connector	2.54-mm pitch, 14 pins × 1 (J26)*
microSD	Card slot × 1 (J27)
PCIe	The selectable configurations are 1 lane × 1 port and root complex or endpoint.
	Connector: 1 lane (J6)
Inverter board interface (INV)	Connectors: 50-pin right-angle × 2 (J49 and J50) and 50-pin straight × 2 (J51 and J52)
RMW interface	Connector: 4 pins × 1 (J40)
Pin headers (2.54-mm pitch)	BSC: 40 pins × 2 (J46 and J47)*
	GPIO: 14 pins × 1 (J55)*
	ADC: 14 pins × 1 (J56)*

Note: The connector is not mounted on the product as shipped.

2. Power Supply

2.1 Specifications of Power Supply

This board has a USB Type-C® connector (J7) and a bipolar terminal block (J10). Power can be supplied from either of these. Table 2-1 lists the specifications of power supply.

Table 2-1 Specifications of Power Supply

Connector	Specifications and Supply Voltage
J7	USB power delivery (USB PD) supporting USB Type-C®, 15-V/3-A DC*1
J10	5.08-mm pitch bipolar terminal block, 24-V/8-A (Max.) DC*2

Notes: 1. When supplying power through J7, always use an AC adapter for USB that supports 15 V/3 A.
 2. When supplying power through J10, always use a stabilized power source that is capable of supplying at least 24 V/4 A. When supplying 24-V power from this board with inverter boards connected, supply power through J10. The maximum current that can be supplied through J10 is 8 A. If the total current drawn by this board and the inverter boards will exceed 8 A, do not supply 24-V power from this board to the inverter boards. In such cases, supply 15-V power to this board through J7 and directly supply 24-V power to the inverter boards.

2.2 Methods for Turning the Power On and Off

This board is equipped with a power switch (slide switch POWER_SW: SW1). When turning the power on, connect the power to J7 or J10 with the power switch turned off, and then turn the power switch on to start the power supply. To end the supply of power, turn the power switch off and then disconnect the power cable from J7 or J10. Figure 2-1 shows the arrangement and manipulation method of the power switch.

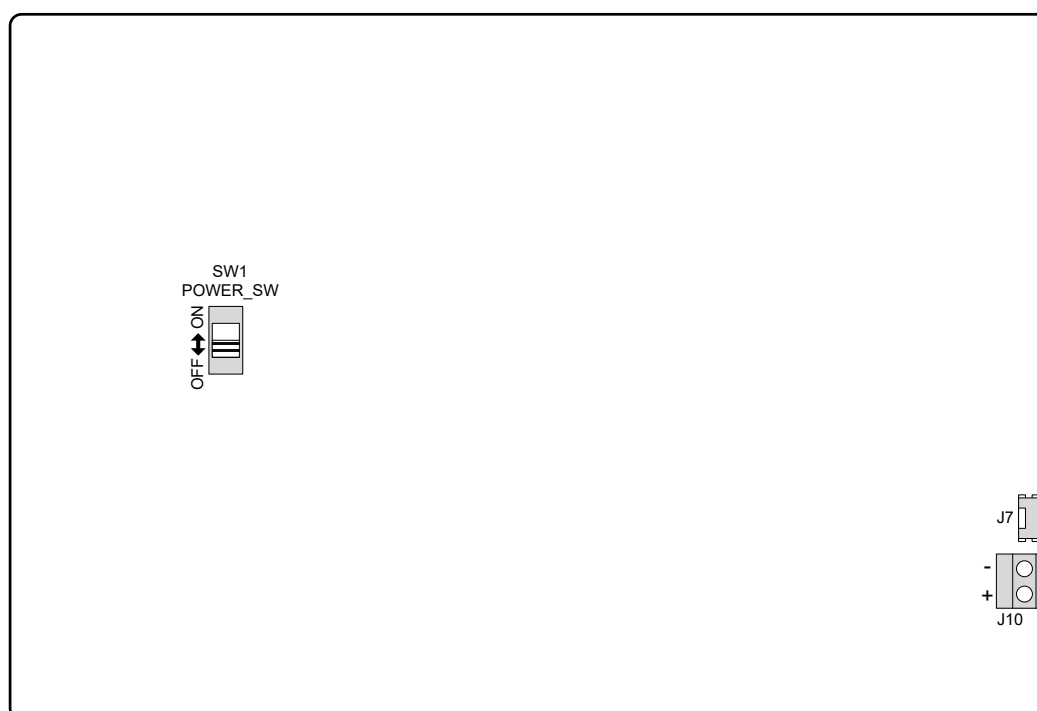


Figure 2-1 Arrangement and Method of Manipulating the Power Switch

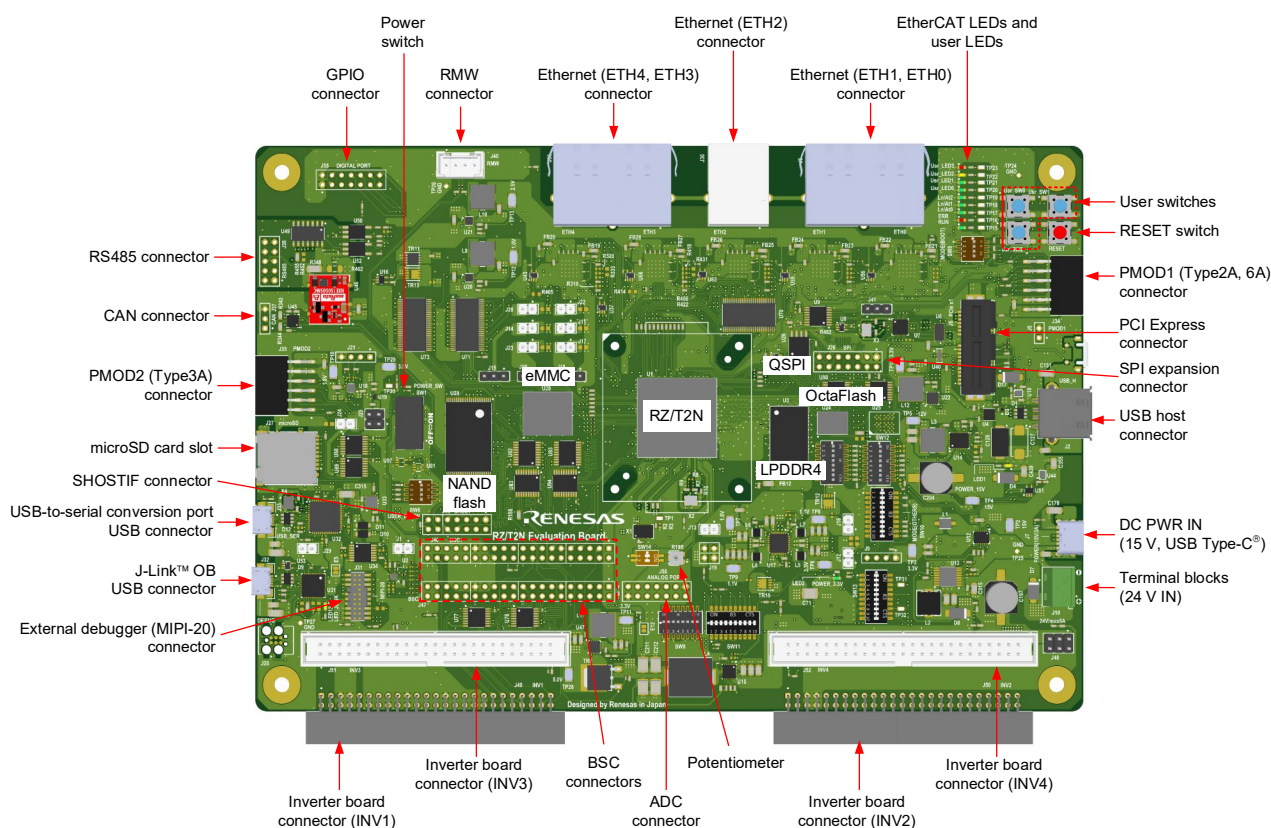
2.3 Jumper Blocks for Current Measurement

This board has jumper blocks for measuring currents, and each current value can be measured by inserting an ammeter between pins 1-2 of the given connector. See **6.4.4 Current Measurement Jumper Blocks J11 to J14, J16, J17, J19, J20, and J22 to J24** for details.

3. Board Layout

3.1 Component Layouts

Figure 3-1 and Figure 3-2 show the component layouts on the top and on the soldered side of this board.



Notes: 1. For the details of each function, refer to chapter 7.

2. The MAC address shown in the figure is an example. Use a unique MAC address when running Ethernet software.

Figure 3-1 Board Layout (Top Side)

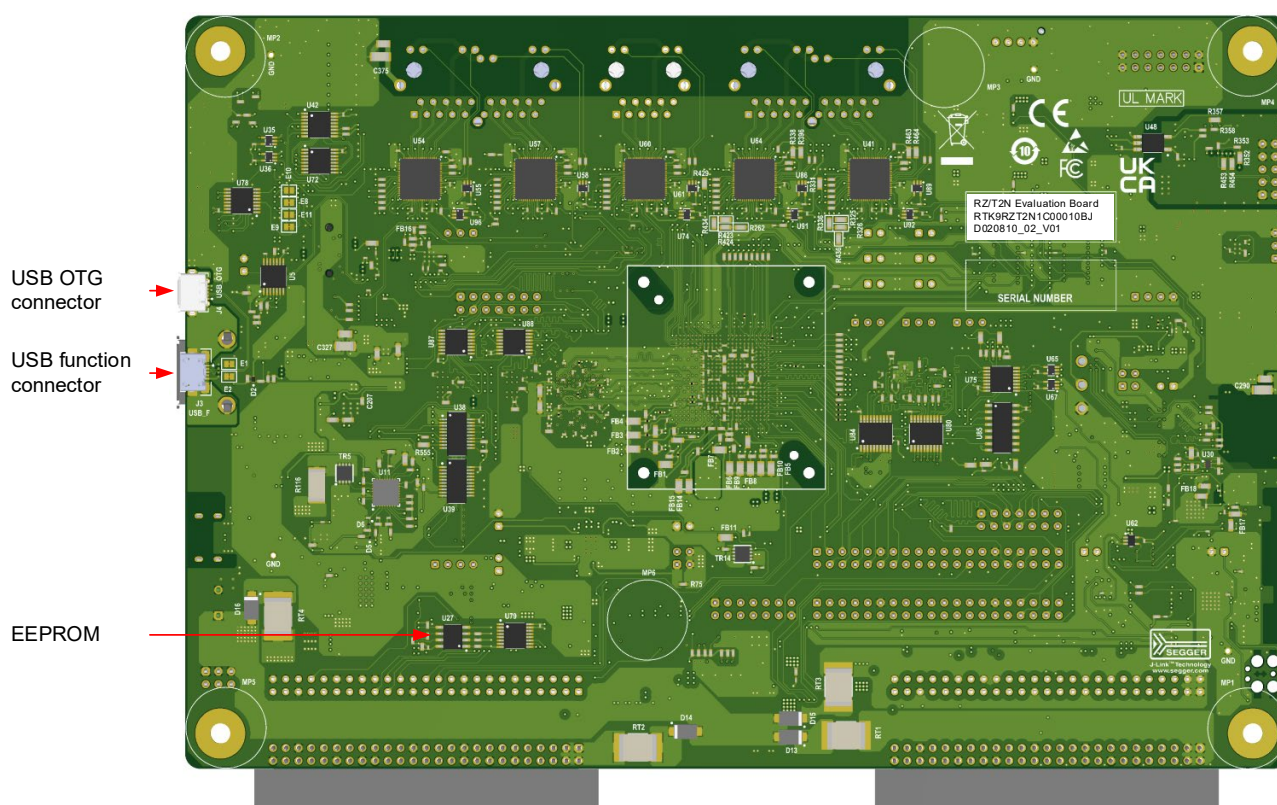


Figure 3-2 Board Layout (Bottom Side)

4. Connections

4.1 Internal Connections of the Board

Figure 4-1 shows the connections between components of this board and the RZ/T2N.

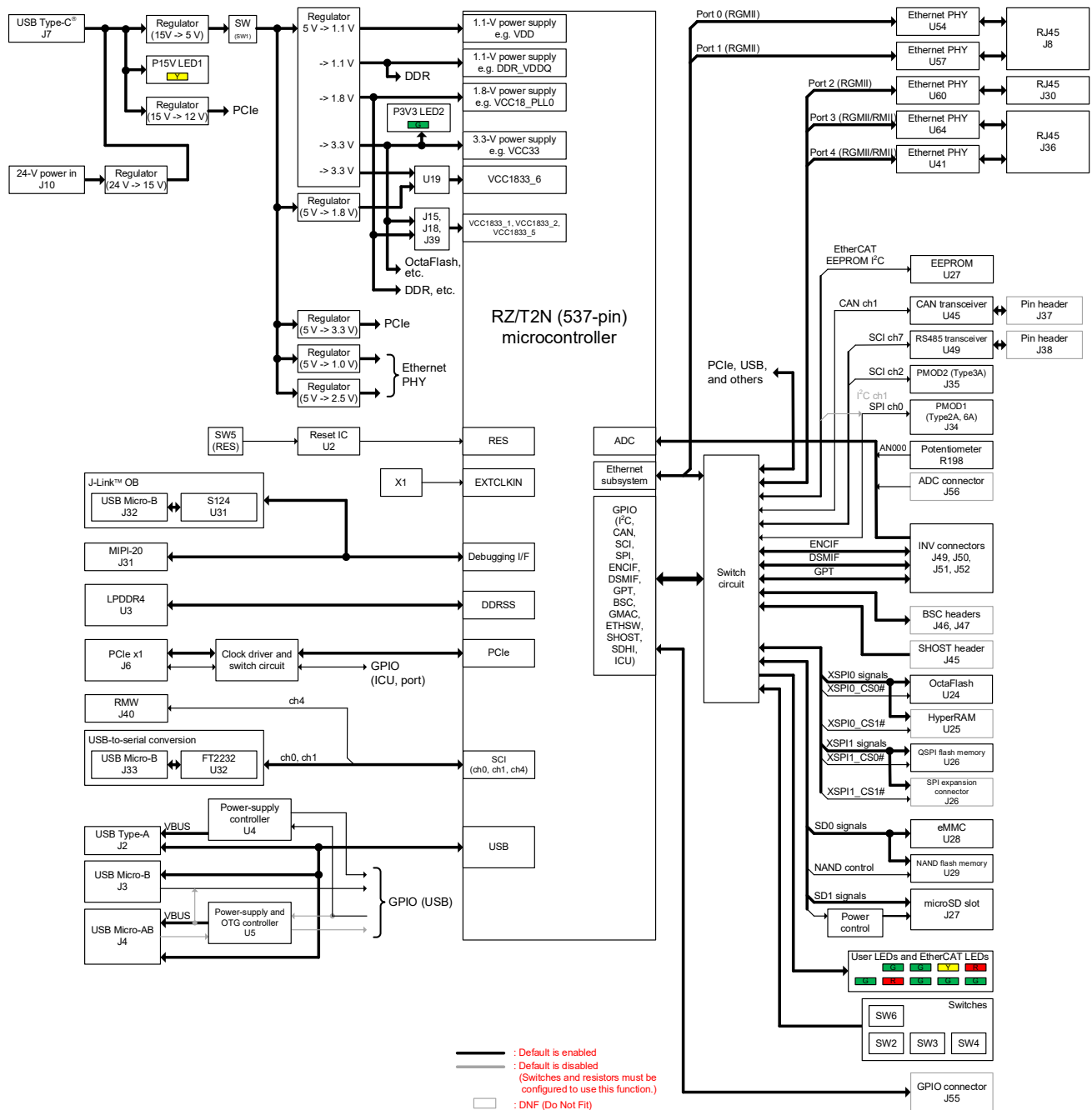


Figure 4-1 Internal Connections of the Board

4.2 Connections in the Debugging Environment

Figure 4-2 shows the connection between this board, the emulator, and the host PC. Figure 4-3 shows the connection between this board and the host PC when J-Link™ OB on this board is used.

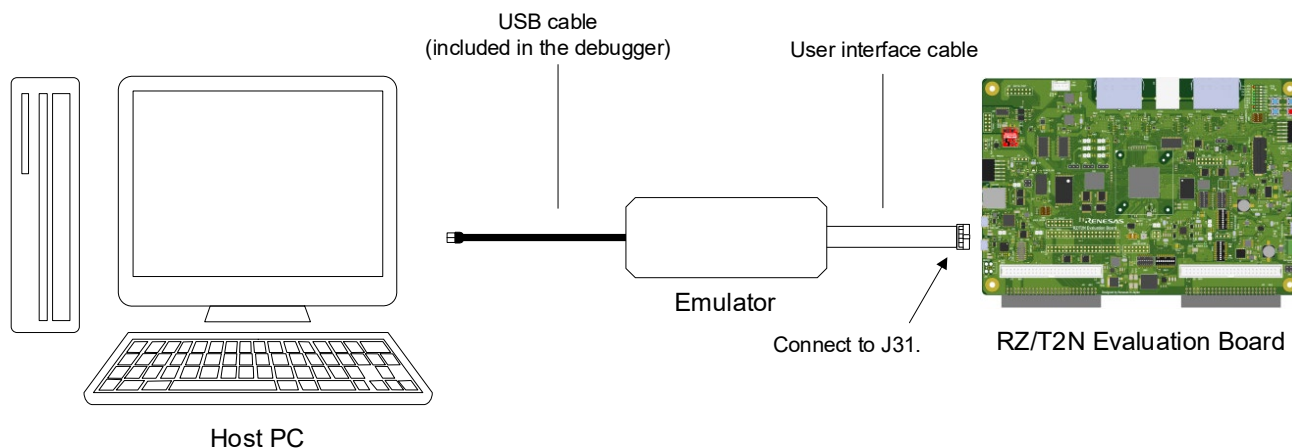


Figure 4-2 Connections in the Debugging Environment (with an Emulator)

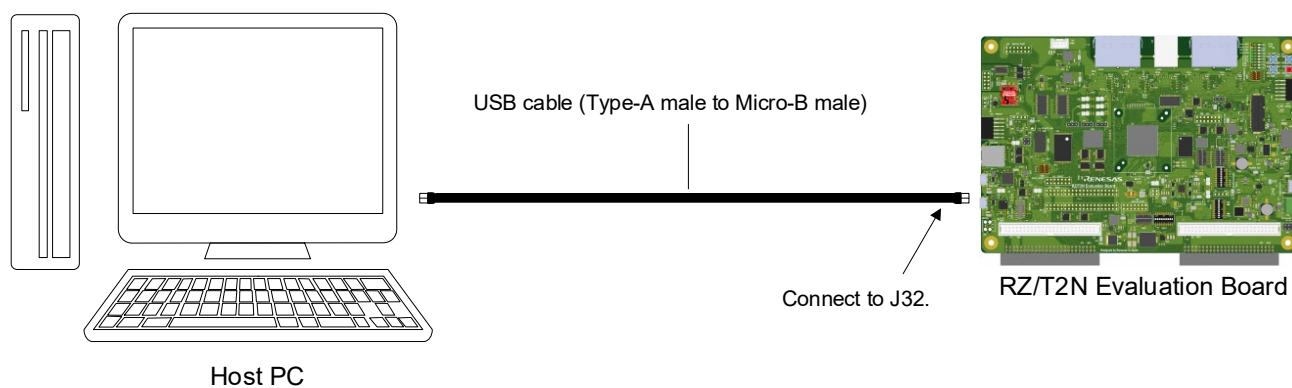


Figure 4-3 Connections in the Debugging Environment (with J-Link™ OB)

5. List of RZ/T2N Pin Functions

Table 5-1 to Table 5-25 are lists of the functions of RZ/T2N pins used on this board. **Text in bold blue type** in the tables indicates the settings at the time of shipment of the board and the functions available with those settings. However, a signal that is connected to multiple connectors can be used in only one of the connectors at a time.

Table 5-1 List of RZ/T2N Pin Function Selections (1)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
A1	VSS				
A2	P23_5/IRQ23_5/GTIOC4_2B/DE3/ETH2_TXEN/ESC_LEDERR/SPI_SSL02/MCLK30/MCLK42/HDSL7_MOSI1	MCLK30	Clock MCLK30 of DSMIF	J52-21	SW7-2: OFF
		ETH2_TXEN	TXEN of Ethernet port 2		SW7-2: ON
A3	P23_0/IRQ23_0/GTIOC3_3A/GTIOC4_0A/RXD3/SCL3/MISO3/ETH2_TXCLK/SPI_RSPCK0/MDAT01/HDSL7_LINK	ETH2_TXCLK	TXCLK of Ethernet port 2		
A4	VSS				
A5	P22_2/IRQ22_2/GTIOC0_3A/GTIOC4_5B/GTIOC5_0B/ETH1_RXD2/HDSL6_MISO1	ETH1_RXD2	RXD2 of Ethernet port 1		
A6	P21_6/IRQ21_6/ETH1_TXEN/HDSL6_LINK	ETH1_TXEN	TXEN of Ethernet port 1		
A7	VSS				
A8	P21_4/IRQ21_4/ETH1_TXD2/HDSL5_MISO2	ETH1_TXD2	TXD2 of Ethernet port 1		
A9	P20_4/MD0/IRQ20_4/GMAC0_MDC/GMAC1_MDC/GMAC2_MDC/ETHSW_MDC/ESC_MDC/ESWM_MDC/CANTX1	MD0	Input of MD0 setting		
		GMAC0_MDC	MDC of Ethernet port 0		SW12-3: ON
			MDC of Ethernet port 1		
			MDC of Ethernet port 2		SW12-4: ON
A10	P20_1/IRQ20_1/ETH0_RXD2/CANRXDP0/HDSL4_MISO2	ETH0_RXD2	RXD2 of Ethernet port 0		
A11	VSS				
A12	P19_5/IRQ19_5/ETH0_TXEN/HDSL4_MISO1	ETH0_TXEN	TXEN of Ethernet port 0		
A13	VSS				
A14	P18_4/IRQ18_4/GTETRGA/DEE4/ESWM_TASGATE1_5/XSPI0_IO5/MDAT21/ENCIFOE4/HDSL3_MOSI1	XSPI0_IO5	Data IO5 of XSPI0		SW7-6: ON
		ENCIFOE4	Output enable ENCIFOE4 of ENCIF	J49-47	SW7-6: OFF
A15	P18_1/IRQ18_1/ESWM_TASGATE1_2/XSPI0_IO2/MCLK32/HDSL3_CLK1	XSPI0_IO2	Data IO2 of XSPI0		
A16	P17_6/IRQ17_6/ESWM_TASGATE0_8/XSPI0_DS/MCLK20/HDSL2_MOSI2	XSPI0_DS	Data strobe DS of XSPI0		
A17	VSS				

A18	P17_1/IRQ17_1/MTIOC0B/MTIOC6C/GTIOC4_4B/RXDE3/IIC_SDA1/ETH2_COL/ETH3_COL/CANTX0/XSPI1_IO7/MDAT31/MBX_HINT#/ENCIFDI3/HDSL2_MISO1	IIC_SDA1	SDA1 of PCIe clock driver		SW13-6: OFF, SW13-7: ON
			SDA1 of PMOD1	J34-4	SW13-6: OFF, SW13-7: ON, E9: Open-circuit, E11: Short-circuit
		XSPI1_IO7	IO7 of SPI expansion connector	J26-5	SW13-6: ON, SW13-7: OFF
		ENCIFDI3	Data input ENCIFDI3 of ENCIF	J52-44	
A19	P16_4/IRQ16_4/MTIOC7B/GTIOC3_2A/GTIOC4_2A/RXD4/SCL3/MISO3/SCKE7/ETH4_CRS/SPI_MISO0/XSPI1_IO2/MCLK01/ENCIFCK7/HDSL1_MOSI2	XSPI1_IO2	Data IO2 of XSPI1	J26-10	SW7-5: ON
		SPI_MISO0	Data MISO0 of PMOD1	J34-3	SW7-5: OFF, E8: Short-circuit, E10: Open-circuit
		GTIOC3_2A	Input/output GTIOC3_2A of GPT	J52-32	SW7-5: OFF
A20	P16_1/IRQ16_1/MTIOC6D/GTIOC3_0B/GTIOC4_0B/TXD1/SDA1/MOSI1/RXDE1/IIC_SDA2/ESWM_TASGATE0_3/XSPI1_DS/MDAT22/ENCIFDI1/HDSL1_CLK2	P16_1	RESETOUT of Ethernet ports 3 and 4		SW7-3: ON
		GTIOC3_0B	Input/output GTIOC3_0B of GPT	J52-29	SW7-3: OFF
A21	VSS				
A22	P15_3/IRQ15_3/D10/MTIOC1A/MTIOC3C/GTIOC2_4B/CMTW1_TOC0/RXDE2/SD1_IOVS/ADTRG0#/HD10/ENCIFDI2/HDSL1_LINK	D10	Data D10 of external bus	J47-23	
		ENCIFDI2	Data input ENCIFDI2 of ENCIF	J51-44	
A23	P14_6/IRQ14_6/D5/MTIOC1B/MTIOC4B/GTIOC2_2A/CMTW0_TIC0/SD0_PWEN/HD5/HDSL0_MOSI1/POUTA	D5	Data D5 of external bus	J47-13	
		GTIOC2_2A	Input/output GTIOC2_2A of GPT	J50-32	
A24	P14_3/IRQ14_3/D2/POE0#/GTIOC0_2A/GTETRGA/RTCAT1HZ/SCIEXTCLK/ADTRG0#/USB_EXICEN/HD2/MBX_HI NT#/HDSL0_CLK1	D2	Data D2 of external bus	J47-5	SW11-8: OFF, SW11-9: ON
		USB_EXICEN	Control of USB_OTG power-supply IC		SW11-8: ON, SW11-9: OFF
A25	VSS				

Table 5-2 List of RZ/T2N Pin Function Selections (2)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
B1	P24_3/IRQ24_3/GTIOC4_5B/CMTW0_TIC1/RXD5/SDA5/MOSI5/IIC_SCL1/ETH0_RXER/ETH2_RXDV/ESC_I2CCLK/SPI_MOSI1/SD0_PWEN/MDAT12/HD SL0_LINK	ETH2_RXDV	RXDV of Ethernet port 2		SW7-2: ON
		MDAT12	Data MDAT12 of DSMIF	J50-26	SW7-2: OFF
B2	P23_6/IRQ23_6/GTIOC4_3A/GTIOC5_3A/RTCAT1HZ/SCK4/ETH2_RXCLK/ESC_LED RUN/SD0_CD/MDAT30/MDA T42/HDSL7_CLK2	ETH2_RXCLK	RXCLK of Ethernet port 2		SW7-2: ON
		MDAT30	Data MDAT30 of DSMIF	J52-22	SW7-2: OFF
B3	P23_2/IRQ23_2/GTIOC4_1A/IIC_SDA0/ETH2_TXD1/ESC_LINKACT0/CANTXDP1/SPI_MOSI0/MDAT21/MDAT40/ HDSL7_CLK1	ETH2_TXD1	TXD1 of Ethernet port 2		SW7-2: ON
		MDAT21	Data MDAT21 of DSMIF	J51-24	SW7-2: OFF
B4	P22_4/IRQ22_4/GTIOC0_2B/ETH1_RXDV/HDSL6_CLK2	ETH1_RXDV	RXDV of Ethernet port 1		
B5	P22_6/ETH1_REFCLK/RMII1_REFCLK/IRQ22_6/HDSL6_MISO2	ETH1_REFCLK	REFCLK of Ethernet port 1		
B6	P21_5/IRQ21_5/ETH1_TXD3/HDSL5_MOSI2	ETH1_TXD3	TXD3 of Ethernet port 1		
B7	P21_7/IRQ21_7/GTIOC4_4A/ETH1_RXCLK/HDSL6_SMPL	ETH1_RXCLK	RXCLK of Ethernet port 1		
B8	P21_1/IRQ21_1/ETH1_TXCLK/HDSL5_MOSI1	ETH1_TXCLK	TXCLK of Ethernet port 1		
B9	P20_6/IRQ20_6/ETHSW_PHYLINK0/ESC_PHYLINK0/ESWM_PHYLINK0/HP SW_PHYLINK0/CANRXDP1/HDSL5_CLK1	ETHSW_PHYLNK0	PHYLINK0 of Ethernet port 0		
B10	P20_7/ETH0_REFCLK/RMII0_REFCLK/IRQ20_7/CANTXDP1/HDSL5_SEL1	ETH0_REFCLK	REFCLK of Ethernet port 0		
B11	P19_6/IRQ19_6/ETH0_RXCLK/HDSL4_MOSI1	ETH0_RXCLK	RXCLK of Ethernet port 0		
B12	P19_2/IRQ19_2/ETH0_TXD1/HDSL4_SMPL	ETH0_TXD1	TXD1 of Ethernet port 0		
B13	P19_0/IRQ19_0/ETH0_TXCLK/HDSL3_MOSI2	ETH0_TXCLK	TXCLK of Ethernet port 0		
B14	P18_5/IRQ18_5/GTETRGB/RXDE4/ESWM_TASGATE1_6/XSPI0_IO6/MCLK20/ENCIFDI4/HDSL3_CLK2	XSPI0_IO6	Data IO6 of XSPI0		SW7-6: ON
		MCLK20	Clock MCLK20 of DSMIF	J51-21	SW7-6: OFF
B15	P18_0/IRQ18_0/ESWM_TASGATE1_1/XSPI0_IO1/MCLK02/HDSL3_SMPL	XSPI0_IO1	Data IO1 of XSPI0		
B16	P17_3/IRQ17_3/DEE7/ESWM_TASGATE0_5/XSPI0_CKN/MDAT30/ENCIFOE7/HDSL2_CLK2	XSPI0_CKN	Clock CKN of XSPI0		
B17	P17_2/IRQ17_2/SCKE7/ESWM_TASGATE0_4/XSPI0_CKP/MCLK30/ENCIFCK7/HDSL2_MOSI1	XSPI0_CKP	Clock CKP of XSPI0		

B18	P16_6/IRQ16_6/MTCLKC/MTIOC0C/GTIOC3_3A/SCKE3/IIC_SCL0/ETH2_TXER/ETH3_TXER/CANRXDP0/SPI_RSCK0/XSPI1_IO4/MCLK30/ENCIFCK3/HDSL2_SMPL	XSPI1_IO4	IO4 of SPI expansion connector	J26-8	
		SPI_RSPCK0	Clock RSPCK0 of PMOD1	J34-4	E9: Short-circuit, E11: Open-circuit
		GTIOC3_3A	Input/output GTIOC3_3A of GPT	J52-37	SW9-8: ON
		ENCIFCK3	Clock ENCIFCK3 of ENCIF	J52-41	SW9-8: OFF
B19	P16_3/IRQ16_3/MTIOC7C/GTIOC3_1A/GTIOC4_1B/TXD5/SDA5/MOSI5/TXDE4/ETH4_RXER/SPI_SSL02/XSPI1_IO1/ENCIFDO4/HDSL1_MISO2	GTIOC3_1A	Input/output GTIOC3_1A of GPT	J52-30	SW7-5: OFF
		SPI_SSL02	SSL02 of PMOD1	J34-10	
		XSPI1_IO1	Data IO1 of XSPI1	J26-11	SW7-5: ON
B20	P16_0/IRQ16_0/MTIOC1B/MTIOC6B/GTIOC3_0A/GTIOC4_0A/RXD1/SCL1/MISO1/TXDE1/IIC_SCL2/ESWM_TASGATE0_2/XSPI1_CS1#MCLK22/ENCIFDO1/HDSL1_MOSI1	P16_0	RST of PMOD1	J34-8	
		GTIOC3_0A	Input/output GTIOC3_0A of GPT	J52-28	
		XSPI1_CS1#	CS1# of SPI expansion connector	J26-4	
B21	P15_6/IRQ15_6/GTIOC0_4A/DE1/TXD E6/TXDE7/IIC_SCL1/ESWM_TASGATE0_0/XSPI1_CKP/MCLK21/ENCIFDO6/ENCIFDO7/HDSL1_SEL1	XSPI1_CKP	Clock CKP of XSPI1	J26-3	R482: Fit
B22	P15_1/IRQ15_1/D8/MTCLKB/MTIOC8D/GTIOC2_3B/CMTW0_TOC1/DEE2/SD1_WP/HD8/ENCIFOE2/HDSL0_MISO2	IRQ15_1	MDINT of Ethernet port 4		SW7-4: ON
		D8	Data D8 of external bus	J47-19	SW7-4: OFF
		GTIOC2_3B	Input/output GTIOC2_3B of GPT	J51-38	SW7-4: OFF, SW9-7: ON
		ENCIFOE2	Output enable ENCIFOE2 of ENCIF	J51-42	SW7-4: OFF, SW9-7: OFF
B23	P14_7/IRQ14_7/D6/MTIOC1A/MTIOC4D/GTIOC2_2B/CMTW0_TOC0/SD0_IOVS/HD6/HDSL0_CLK2/POUTB	D6	Data D6 of external bus	J47-15	
		GTIOC2_2B	Input/output GTIOC2_2B of GPT	J50-33	
B24	P14_1/IRQ14_1/D0/MTIOC3B/MTIOC8A/GTIOC0_0A/GTIOC2_0A/GTIOC4_6A/SCKE6/ETH2_TXER/ETH3_TXER/USB_VBUSEN/HD0/ENCIFCK6/HDSL0_LINK	D0	Data D0 of external bus	J47-1	
		GTIOC2_0A	Input/output GTIOC2_0A of GPT	J50-28	
B25	P13_4/IRQ13_4/D23/GTADSM3_1/RT CAT1HZ/ETH1_COL/GMAC0_MDIO/GMAC1_MDIO/GMAC2_MDIO/ETHSW_MDIO/ESC_MDIO/ESWM_MDIO/SD1_IOVS/MDAT42/HD23/HDSL7_MOSI1	P13_4	GPIO connector	J55-10	

Table 5-3 List of RZ/T2N Pin Function Selections (3)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
C1	P25_0/IRQ25_0/RXD1/SCL1/MISO1/RXD3/SCL3/MISO3/ETHSW_PHYLINK2/ESC_PHYLINK2/CANTX1/SPI_SSL03/MCLK22	MCLK22	Clock MCLK22 of DSMIF	J51-25	SW7-2: OFF
		ETHSW_PHYLINK2	PHYLINK2 of Ethernet port 2		SW7-2: ON
C2	P24_2/IRQ24_2/TEND/POE8#/GTIOC4_5A/CMTW0_TOC0/CTS4#/RXDE0/ETH2_RXD3/ESC_RESETOUT#/SPI_SSL11/MDAT11/ENCIFDI0/HDSL7_MOSI2	TEND	End of DMA transfer	J46-40	SW7-2: OFF
		MDAT11	Data MDAT11 of DSMIF	J50-24	
		ETH2_RXD3	RXD3 of Ethernet port 2		SW7-2: ON
C3	P24_0/IRQ24_0/DREQ/POE0#/GTIOC4_4A/DEE0/IIC_SDA1/ETH0_CRSETH2_RXD1/ESC_LINKACT2/SPI_SSL13/SD1_CD/MDAT10/MDAT32/ENCIFDI0/HDSL7_MISO2	DREQ	DMA request	J46-28	SW7-2: OFF
		MDAT32	Data MDAT32 of DSMIF	J52-26	
		ETH2_RXD1	RXD1 of Ethernet port 2		SW7-2: ON
C4	P23_3/IRQ23_3/GTIOC4_1B/GTIOC4_3A/SS3#/CTS3#/RTS3#/ETH2_TXD2/ESC_LINKACT1/SPI_SSL00/MCLK01/MCLK41/HDSL7_SEL1	ETH2_TXD2	TXD2 of Ethernet port 2		
C5	P23_1/IRQ23_1/GTIOC3_3B/GTIOC4_0B/SCK3/IIC_SCL0/ETH2_TXD0/GMAC0_PTPTRG0/ESC_LATCH0/CANRXDP1/SPI_MISO0/MCLK21/MCLK40/HDSL7_SMPL	ETH2_TXD0	TXD0 of Ethernet port 2		SW7-2: ON
		MCLK21	Clock MCLK21 of DSMIF	J51-23	SW7-2: OFF
C6	P22_0/IRQ22_0/GTIOC4_4B/ETH1_RXD0/HDSL6_CLK1	ETH1_RXD0	RXD0 of Ethernet port 1		
C7	P20_5/IRQ20_5/GMAC0_MDIO/GMAC1_MDIO/GMAC2_MDIO/ETHSW_MDIO/ESC_MDIO/ESWM_MDIO/CANRX1/HDSL5_SMPL	GMAC0_MDIO	MDIO of Ethernet port 0		SW12-3: ON
			MDIO of Ethernet port 1		
			MDIO of Ethernet port 2		SW12-4: ON
C8	P21_3/IRQ21_3/ETH1_TXD1/HDSL5_SEL2	ETH1_TXD1	TXD1 of Ethernet port 1		
C9	P21_0/IRQ21_0/HDSL5_MISO1	IRQ21_0	MDINT of Ethernet port 0		
C10	P20_2/IRQ20_2/ETH0_RXD3/CANTXDP0/HDSL4_MOSI2	ETH0_RXD3	RXD3 of Ethernet port 0		
C11	P20_0/IRQ20_0/ETH0_RXD1/CANTX0/HDSL4_SEL2	ETH0_RXD1	RXD1 of Ethernet port 0		
C12	P19_3/IRQ19_3/ETH0_TXD2/HDSL4_CLK1	ETH0_TXD2	TXD2 of Ethernet port 0		
C13	P18_7/IRQ18_7/ESWM_TASGATE1_8/XSPI0_RESETO#/MCLK30/MDAT02/HDSL3_MISO2	XSPI0_RESET0#	Reset 0 of XSPI0		
C14	P18_2/IRQ18_2/ESWM_TASGATE1_3/XSPI0_IO3/MDAT32/HDSL3_SEL1	XSPI0_IO3	Data IO3 of XSPI0		
C15	P17_7/IRQ17_7/ESWM_TASGATE1_0/XSPI0_IO0/MDAT20/HDSL3_LINK	XSPI0_IO0	Data IO0 of XSPI0		
C16	P17_5/IRQ17_5/RXDE7/ESWM_TASGATE0_7/XSPI0_CS1#/MDAT31/ENCIFDI7/HDSL2_MISO2	XSPI0_CS1#	Chip select CS1# of XSPI0		SW7-6: ON
		ENCIFDI7	Data input ENCIFDI7 of ENCIF	J52-49	SW7-6: OFF

C17	P17_0/IRQ17_0/MTIOC0A/MTIOC6A/GTIOC3_4A/TXDE3/IIC_SCL1/ETH2_CRS/ETH3_CRS/CANRX0/XSPI1_IO6/MCLK31/USB_VBUSEN/ENCIFDO3/HDSL2_SEL1	GTIOC3_4A	Input/output GTIOC3_4A of GPT	J52-39	SW9-8: ON, SW12-5: ON, SW13-1: ON, SW13-2: OFF
		ENCIFDO3	Data output ENCIFDO3 of ENCIF	J52-43	SW9-8: OFF, SW12-5: ON, SW13-1: ON, SW13-2: OFF
		IIC_SCL1	SCL1 of PCIe clock driver		SW13-1: OFF, SW13-2: ON
			SCL1 of PMOD1	J34-3	SW13-1: OFF, SW13-2: ON, E8: Open-circuit, E10: Short-circuit
		XSPI1_IO6	IO6 of SPI expansion connector	J26-6	SW13-1: ON, SW13-2: OFF
C18	P16_5/IRQ16_5/MTIOC7D/GTIOC3_2B/GTIOC4_2B/TXD3/SDA3/MOSI3/DEE7/ETH4_COL/SPI_MOSI0/XSPI1_IO3/MDAT01/ENCIFOE7/HDSL2_LINK	GTIOC3_2B	Input/output GTIOC3_2B of GPT	J52-33	SW7-5: OFF
		SPI_MOSI0	MOSI0 of PMOD1	J34-2	
		XSPI1_IO3	Data IO3 of XSPI1	J26-9	SW7-5: ON
C19	P15_7/IRQ15_7/GTIOC0_4B/DE3/RXD E6/RXDE7/IIC_SDA1/ESWM_TASGAT E0_1/XSPI1_CS0#/MDAT21/ENCIFDI6/ENCIFDI7/HDSL1_MISO1	XSPI1_CS0#	Chip select CS0# of XSPI1		SW7-5: ON
		ENCIFDI6	Data input ENCIFDI6 of ENCIF	J50-49	SW7-5: OFF
C20	P15_2/IRQ15_2/D9/MTIOC3A/MTIC5W/GTIOC2_4A/CMTW1_TIC0/TXDE2/SD1_PWEN/HD9/ENCIFDO2/HDSL0_MOSI2	D9	Data D9 of external bus	J47-21	
		GTIOC2_4A	Input/output GTIOC2_4A of GPT	J51-39	SW9-7: ON
		ENCIFDO2	Data output ENCIFDO2 of ENCIF	J51-43	SW9-7: OFF
C21	P15_4/IRQ15_4/D11/GTIOC2_0A/CMTW1_TIC1/SCKE6/IIC_SCL0/ESC_I2CCLK/MCLK20/ADTRG1#/HD11/ENCIFCK6/HDSL1_SMPL	P15_4	USB_OTG_STATUS1		SW13-3: OFF, SW13-4: OFF, SW13-5: ON
			GPI00 of PMOD2	J35-9	SW13-3: OFF, SW13-4: ON, SW13-5: OFF
		D11	Data D11 of external bus	J47-25	
		ESC_I2CCLK	I²C clock for EEPROM of ESC		SW13-3: ON, SW13-4: OFF, SW13-5: OFF
C22	P14_4/IRQ14_4/D3/MTIOC4A/MTIC5U/GTIOC0_1B/GTIOC2_1A/TXDE6/ETH2_CRS/ETH3_CRS/ADTRG1#/HD3/ENCIFDO6/HDSL0_SEL1	D3	Data D3 of external bus	J47-7	
		GTIOC2_1A	Input/output GTIOC2_1A of GPT	J50-30	
C23	P14_2/IRQ14_2/D1/MTIOC3D/MTIOC8B/GTIOC0_0B/GTIOC2_0B/GTIOC4_6B/DEE6/ETH2_RXER/ETH3_RXER/USB_OVRCUR/HD1/ENCIFOE6/HDSL0_SMPL	D1	Data D1 of external bus	J47-3	
		GTIOC2_0B	Input/output GTIOC2_0B of GPT	J50-29	
C24	P13_3/IRQ13_3/D22/GTADSM3_0/ETH1_CRS/GMAC0_MDC/GMAC1_MDC/GMAC2_MDC/ETHSW_MDC/ESC_MD C/ESWM_MDC/SD1_PWEN/MCLK42/HD22/HDSL7_MISO1	P13_3	Control of user LED0 (LED8)		
C25	P13_2/IRQ13_2/D21/GTADSM2_1/ESC_EDERR/SD1_IOVS/MDAT10/HD21/HDSL7_SEL1	SD1_IOVS	Selection of SDHI ch1 (microSD) power		

Table 5-4 List of RZ/T2N Pin Function Selections (4)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
D1	VSS				
D2	P24_7/IRQ24_7/TXD3/SDA3/MOSI3/GMAC0_MDIO/GMAC1_MDIO/GMAC2_MDIO/ETHSW_MDIO/ESC_MDIO/ESWM_MDIO/CANRX1/SPI_RSPCK1	GMAC1_MDIO	MDIO of Ethernet port 0		SW12-3: OFF
			MDIO of Ethernet port 2		SW12-4: OFF
D3	P24_6/MD1/IRQ24_6/DE5/GMAC0_MDC/GMAC1_MDC/GMAC2_MDC/ETHSW_MDC/ESC_MDC/ESWM_MDC	MD1	Input of MD1 setting		
		GMAC1_MDC	MDC of Ethernet port 0		SW12-3: OFF
			MDC of Ethernet port 2		SW12-4: OFF
D4	P24_1/IRQ24_1/DACK/POE4#/GTIOC4_4B/CMTW0_TIC0/SS4#/CTS4#/RTS4#/TXDE0/ETH0_TXER/ETH2_RXD2/ESC_IRQ/SPI_SSL10/SD1_WP/MCLK11/MBX_HINT#/ENCIFDO0	ETH2_RXD2	RXD2 of Ethernet port 2		SW7-2: ON
		DACK	DACK of external bus	J46-26	SW7-2: OFF
		MCLK11	Clock MCLK11 of DSMIF	J50-23	
D5	P23_4/IRQ23_4/GTIOC4_2A/GTIOC4_3B/CTS3#/ETH2_TXD3/ETHSW_PTP_OUT2/ESC_SYNC0/SPI_SSL01/MDAT01/MDAT41/HDSL7_MISO1	ETH2_TXD3	TXD3 of Ethernet port 2		SW7-2: ON
		P23_4	GPIO connector	J55-12	SW7-2: OFF
D6	P22_3/IRQ22_3/GTIOC0_3B/ETH1_RXD3/HDSL6_MOSI1	ETH1_RXD3	RXD3 of Ethernet port 1		
D7	P22_1/IRQ22_1/GTIOC4_5A/GTIOC5_0A/ETH1_RXD1/HDSL6_SEL1	ETH1_RXD1	RXD1 of Ethernet port 1		
D8	P21_2/IRQ21_2/ETH1_TXD0/HDSL5_CLK2	ETH1_TXD0	TXD0 of Ethernet port 1		
D9	P22_5/IRQ22_5/ETHSW_PHYLINK1/ESC_PHYLINK1/ESWM_PHYLINK1/HP_SW_PHYLINK1/HDSL6_SEL2	ETHSW_PHYLINK1	PHYLINK1 of Ethernet port 1		
D10	P20_3/IRQ20_3/ETH0_RXDV/HDSL5_LINK	ETH0_RXDV	RXDV of Ethernet port 0		
D11	P19_7/IRQ19_7/ETH0_RXD0/CANRX0/HDSL4_CLK2	ETH0_RXD0	RXD0 of Ethernet port 0		
D12	P19_4/IRQ19_4/ETH0_TXD3/HDSL4_SEL1	ETH0_TXD3	TXD3 of Ethernet port 0		
D13	P19_1/IRQ19_1/ETH0_TXD0/HDSL4_LINK	ETH0_TXD0	TXD0 of Ethernet port 0		
D14	P18_6/IRQ18_6/GTETRGC/TXDE4/ESWM_TASGATE1_7/XSPI0_IO7/MDAT20/ENCIFDO4/HDSL3_SEL2	MDAT20	Data MDAT20 of DSMIF	J51-22	SW7-6: OFF
		XSPI0_IO7	Data IO7 of XSPI0		SW7-6: ON
D15	P18_3/IRQ18_3/SCKE4/ESWM_TASGATE1_4/XSPI0_IO4/MCLK21/ENCIFCK4/HDSL3_MISO1	XSPI0_IO4	Data IO4 of XSPI0		SW7-6: ON
		ENCIFCK4	Clock ENCIFCK4 of ENCIF	J49-46	SW7-6: OFF
D16	P17_4/IRQ17_4/TXDE7/ESWM_TASGATE0_6/XSPI0_CS0#/MCLK31/ENCIFDO7/HDSL2_SEL2	XSPI0_CS0#	Chip select CS0# of XSPI0		

D17	P16_7/IRQ16_7/MTCLKD/MTIOC0D/GTIOC3_3B/DEE3/IIC_SDA0/ETH2_RXER/ETH3_RXER/CANTXDP0/SPI_SSL00/XSPI1_IO5/MDAT30/ENCIFOE3/HDLS2_CLK1	GTIOC3_3B	Input/output GTIOC3_3B of GPT	J52-38	SW7-3: OFF, SW9-8: ON
		ENCIFOE3	Output enable ENCIFOE3 of ENCIF	J52-42	SW7-3: OFF, SW9-8: OFF
		SPI_SSL00	SSL00 of PMOD1	J34-1	SW7-3: OFF
		XSPI1_IO5	IO5 of SPI expansion connector	J26-7	
		ETH3_RXER	RXER of Ethernet port 3		SW7-3: ON , R429: DNF, R431: Fit,
D18	P16_2/IRQ16_2/MTIOC7A/GTIOC3_1B/GTIOC4_1A/RXD5/SCL5/MISO5/RXDE4/ETH4_TXER/SPI_SSL01/XSPI1_IO0/ENCIFDI4/HDLS1_SEL2	GTIOC3_1B	Input/output GTIOC3_1B of GPT	J52-31	SW7-5: OFF
		SPI_SSL01	SSL01 of PMOD1	J34-9	
		XSPI1_IO0	Data IO0 of XSPI1	J26-12	SW7-5: ON
D19	P15_5/IRQ15_5/D12/GTIOC2_0B/CMTW1_TOC1/RTCAT1HZ/DEE6/IIC_SDA0/ESC_I2CDATA/MDAT20/ADTRG2#/HD12/ENCIFDO6/HDLS1_CLK1	P15_5	USB_OTG_STATUS2		SW13-8: OFF, SW13-9: OFF , SW13-10: ON
			GPIO1 of PMOD2	J35-10	SW13-8: OFF, SW13-9: ON, SW13-10: OFF
		D12	Data D12 of external bus	J47-27	SW13-8: ON , SW13-9: OFF , SW13-10: OFF
		ESC_I2CDATA	I²C data for EEPROM of ESC		
D20	P14_5/IRQ14_5/D4/MTIOC4C/MTIC5V/GTIOC0_1A/GTIOC2_1B/RXDE6/ETH2_COL/ETH3_COL/ADTRG2#/HD4/ENCIFDI6/HDLS0_MISO1	D4	Data D4 of external bus	J47-9	
		GTIOC2_1B	Input/output GTIOC2_1B of GPT	J50-31	
D21	P15_0/IRQ15_0/D7/MTCLKA/MTIOC8C/GTIOC2_3A/CMTW0_TIC1/SCKE2/SD1_CD/HD7/ENCIFCK2/HDLS0_SEL2/POUTZ	D7	Data D7 of external bus	J47-17	SW7-1: OFF
		GTIOC2_3A	Input/output GTIOC2_3A of GPT	J51-37	SW7-1: OFF, SW9-7: ON
		ENCIFCK2	Clock ENCIFCK2 of ENCIF	J51-41	SW7-1: OFF, SW9-7: OFF
		SD1_CD	CD of SDHI ch1 (microSD)	J27-9	SW7-1: ON
D22	P13_5/IRQ13_5/D24/GTADSM4_0/SCKE7/ESC_LEDSTER/MCLK11/HD24/ENCIFCK7/HDLS7_CLK2	P13_5	Control of user LED1 (LED9)		
D23	P13_1/IRQ13_1/D20/TEND/GTADSM2_0/ESC_LED RUN/SD1_PWEN/MCLK10/HD20/HDLS7_CLK1	SD1_PWEN	Enabling of SDHI ch1 (microSD) power		
D24	P13_0/IRQ13_0/D19/GTADSM1_1/CMTW1_TOC1/ETHSW_PTPOUT1/ESC_SYNC1/MDAT41/HD19/HDLS7_SMPL	P13_0	GPIO connector	J55-11	
D25	P12_6/IRQ12_6/D17/DACK/GTADSM0_1/GTETRGC/CMTW1_TOC0/MDAT40/HD17/HDLS6_MOSI2	MDAT40	Data MDAT40 of DSMIF	J55-3	
		P12_6	GPIO connector		

Table 5-5 List of RZ/T2N Pin Function Selections (5)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
E1	P00_0/IRQ00_0/A16/MTIOC3B/GTIOC0_0A/GTADSM0_0/SCKE1/ETH3_TXCLK/SPI_RSPCK2/HA16/ENCIFCK1/HDSL0_SEL1	A16	Address A16 of external bus	J46-4	SW7-3: OFF
		GTIOC0_0A	Input/output GTIOC0_0A of GPT	J49-28	
		ETH3_TXCLK	TXCLK of Ethernet port 3		SW7-3: ON, R423: Fit, R262: DNF
E2	P00_6/IRQ00_6/A22/MTCLKA/MTIOC8D/GTIOC0_3A/GTADSM3_0/RXD4/SCL4/MISO4/SCKE0/SCKE6/ETH3_RXCLK/SPI_SSL23/MBX_HINT#/ENCIFCK0/ENCIFCK6	A22	Address A22 of external bus	J46-16	SW7-3: OFF
		GTIOC0_3A	Input/output GTIOC0_3A of GPT	J49-37	SW7-3: OFF, SW9-5: ON
		ENCIFCK0	Clock ENCIFCK0 of ENCIF	J49-41	SW7-3: OFF, SW9-5: OFF
		ETH3_RXCLK	RXCLK of Ethernet port 3		SW7-3: ON
E3	P24_5/IRQ24_5/POE10#/GTIOC4_6B/GTETRGA/TXD4/SDA4/MOSI4/SCIEXTCLK/MDAT22/PCIE_RSTOUTB/HDSL0_CLK1	MDAT22	Data MDAT22 of DSMIF	J51-26	
		PCIE_RSTOUTB	RESETOUTB signal of PCIe	J6-A11	SW12-6: ON
E4	P00_1/IRQ00_1/A17/MTIOC3D/GTIOC0_0B/GTADSM0_1/DEE1/IIC_SCL2/ETH3_TXD0/CANRX0/SPI_MISO2/HA17/ENCIFOE1/HDSL0_MISO1	A17	Address A17 of external bus	J46-6	SW7-3: OFF
		GTIOC0_0B	Input/output GTIOC0_0B of GPT	J49-29	
		ETH3_TXD0	TXD0 of Ethernet port 3		SW7-3: ON
E5	P23_7/IRQ23_7/GTIOC4_3B/GTIOC5_3B/SCKE0/IIC_SCL1/ETH0_COL/ETH2_RXD0/SPI_SSL12/SD0_WP/MCLK10/MCLK32/ENCIFCK0/HDSL7_SEL2	ETH2_RXD0	RXD0 of Ethernet port 2		SW7-2: ON
		MCLK32	Clock MCLK32 of DSMIF	J52-25	SW7-2: OFF
E6	P22_7/IRQ22_7/HDSL6_MOSI2	IRQ22_7	MDINT of Ethernet port 1		
E7	VCC1833_1				
E8	VSS				
E9	VCC1833_0				
E10	VSS				
E11	VCC1833_0				
E12	VSS				
E13	VCC1833_3				
E14	VSS				
E15	VSS				
E16	VCC1833_4				
E17	VSS				
E18	VCC33				
E19	VSS				
E20	P13_7/IRQ13_7/D26/TXDE7/MCLK12/HD26/ENCIFDO7/HDSL7_MISO2	TXDE7	Transmit data TXDE7 of RS485		
E21	P14_0/IRQ14_0/D27/RXDE7/ETHSW_PTPOUT3/ESC_SYNC1/MDAT12/HD27/ENCIFDI7/HDSL7_MOSI2	RXDE7	Receive data RXDE7 of RS485		
E22	P12_7/IRQ12_7/D18/GTADSM1_0/GTETRGD/CMTW1_TIC1/ETHSW_PTPOUT0/ESC_SYNC0/MCLK41/HD18/HDSL7_LINK	P12_7	GPIO connector	J55-8	

E23	P13_6/IRQ13_6/D25/GTADSM4_1/DE E7/MDAT11/HD25/ENCIFOE7/HDSL7 _SEL2	DEE7	Data enable DEE7 of RS485		
E24	P12_5/IRQ12_5/D16/DREQ/GTADSM0 _0/GTETRGB/CMTW1_TIC0/MCLK40/ HD16/HDSL6_MISO2	MCLK40	Clock MCLK40 of DSMIF	J55-4	
		P12_5	GPIO connector		
E25	VSS				

Table 5-6 List of RZ/T2N Pin Function Selections (6)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
F1	P00_3/IRQ00_3/A19/MTIOC4C/GTIOC0_1A/GTADSM1_1/RXDE1/ETH3_TXD2/CANRXDP0/SPI_SSL20/MDAT41/H A19/ENCIFDI1/HDSL0_CLK2	A19	Address A19 of external bus	J46-10	SW7-3: OFF
		GTIOC0_1A	Input/output GTIOC0_1A of GPT	J49-30	
		ETH3_TXD2	TXD2 of Ethernet port 3		SW7-3: ON
F2	P00_5/IRQ00_5/A21/MTIOC4D/MTIOC8C/GTIOC0_2B/GTADSM2_1/RXDE6/ETH3_TXEN/SPI_SSL22/MDAT20/H A21/ENCIFDI6/HDSL0_MISO2	A21	Address A21 of external bus	J46-14	SW7-3: OFF
		GTIOC0_2B	Input/output GTIOC0_2B of GPT	J49-33	
		ETH3_TXEN	TXEN of Ethernet port 3		SW7-3: ON
F3	P00_2/IRQ00_2/A18/MTIOC4A/GTIOC0_1B/GTADSM1_0/TXDE1/IIC_SDA2/ETH3_TXD1/CANTX0/SPI_MOSI2/MC LK41/H A18/ENCIFDI1/HDSL0_MOSI1	A18	Address A18 of external bus	J46-8	SW7-3: OFF
		GTIOC0_1B	Input/output GTIOC0_1B of GPT	J49-31	
		ETH3_TXD1	TXD1 of Ethernet port 3		SW7-3: ON
F4	P00_4/IRQ00_4/A20/MTIOC4B/GTIOC0_2A/GTADSM2_0/TXDE6/ETH3_TXD3/CANTXDP0/SPI_SSL21/MCLK20/H A20/ENCIFDI6/HDSL0_SEL2	A20	Address A20 of external bus	J46-12	SW7-3: OFF
		GTIOC0_2A	Input/output GTIOC0_2A of GPT	J49-32	
		ETH3_TXD3	TXD3 of Ethernet port 3		SW7-3: ON
F5	P24_4/ETH2_REFCLK/RMII2_REFCLK/IRQ24_4/POE11#/GTIOC4_6A/CMTW0_TOC1/RXD5/SCL5/MISO5/IIC_SDA1/ETH1_RXER/ESC_I2CDATA/SPI_MISO1/SD0_IOVS/MCLK12/HDSL0_S MPL	ETH2_REFCLK	REFCLK of Ethernet port 2		SW7-2: ON
		MCLK12	Clock MCLK12 of DSMIF	J50-25	SW7-2: OFF
F6	VSS				
F7	VCC1833_1				
F8	VSS				
F9	VCC1833_0				
F10	VSS				
F11	VCC1833_0				
F12	VSS				
F13	VCC1833_3				
F14	VSS				
F15	VCC18_PLL1				
F16	VCC1833_4				
F17	VSS				
F18	VCC33				
F19	VSS				
F20	VCC33				
F21	VSS				
F22	VSS				
F23	VSS				
F24	VSS				
F25	VSS				

Table 5-7 List of RZ/T2N Pin Function Selections (7)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
G1	VSS				
G2	P01_4/ETH3_REFCLK/RMII3_REFCLK/IRQ01_4/CS5#/TEND/TXD1/SDA1/MOSI1/RXDE4/IIC_SDA1/ETH1_RXER/ETH1_CRS/ESC_I2CDATA/SPI_RSPCK2/MCLK01/USB_EXICEN/ADTRG2#/ENCIFDI4	CS5#	CS5# of external bus	J46-20	SW7-3: OFF
		ETH3_REFCLK	REFCLK of Ethernet port 3		SW7-3: ON
G3	P01_5/IRQ01_5/CS2#/DREQ/TXDE4/ETH1_COL/ETH3_TXER/ESC_RESETO/UT#ESWM_PHYLINK0/HPSW_PHYLINK0/SPI_SSL20/MDAT01/USB_EXICEN/HCS1#/ENCIFDO4	CS2#	CS2# of external bus	J46-34	SW7-3: OFF
		MDAT01	Data MDAT01 of DSMIF	J49-24	
		ESWM_PHYLINK0	PHYLINK0 of Ethernet port 3		SW7-3: ON
G4	P01_2/IRQ01_2/BS#/DREQ/SS5#/CTS5#/RST5#/TXD5/SDA5/MOSI5/SCKE4/ETH3_RXD3/SPI_MOSI2/SD1_IOVS/MCLK00/ADTRG0#/HBS#/ENCIFCK4	BS#	BS# of external bus	J46-30	SW7-3: OFF
		MCLK00	Clock MCLK00 of DSMIF	J49-21	
		ETH3_RXD3	RXD3 of Ethernet port 3		SW7-3: ON, R429: Fit, R431: DNF
G5	P00_7/IRQ00_7/A23/MTCLKB/MTIOC1B/GTIOC0_3B/GTADSM3_1/TXD4/SDA4/MOSI4/DEE0/DEE6/ETH3_RXD0/SPI_SSL22/HERROT#/ENCIFOE0/ENCIFOE6	A23	Address A23 of external bus	J46-18	SW7-3: OFF
		GTIOC0_3B	Input/output GTIOC0_3B of GPT	J49-38	SW7-3: OFF, SW9-5: ON
		ENCIFOE0	Output enable ENCIFOE0 of ENCIF	J49-42	SW7-3: OFF, SW9-5: OFF
		ETH3_RXD0	RXD0 of Ethernet port 3		SW7-3: ON
G6	VSS				
G7	—				
G8	—				
G9	—				
G10	—				
G11	—				
G12	—				
G13	—				
G14	—				
G15	—				
G16	—				
G17	—				
G18	—				
G19	—				
G20	DDR_VDDQ				
G21	VSS				
G22	VSS				
G23	VSS				
G24	VSS				
G25	VSS				

Table 5-8 List of RZ/T2N Pin Function Selections (8)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
H1	P01_6/IRQ01_6/D13/MTIOC6B/MTIOC8B/GTIOC1_0A/GTADSM0_0/GTETR GB/CMTW1_TIC0/SCK1/ETH0_RXER/ETH4_TXCLK/SPI_RSPCK3/SD1_CD/MCLK02/HD13	D13	Data D13 of external bus	J47-31	SW7-4: OFF
		MCLK02	Clock MCLK02 of DSMIF	J49-25	
		ETH4_TXCLK	TXCLK of Ethernet port 4		SW7-4: ON, R325: Fit, R436: DNF
H2	P01_1/IRQ01_1/RD/WR#/MITOC3C/MTIOC8A/GTIOC0_4B/GTADSM4_1/SCK5/RXD5/SCL5/MISO5/RXDE0/ETH3_RXD2/SD1_PWEN/USB_OVRCUR/HWRSTB#/ENCIFDI0	RD/WR#	RD/WR# of external bus	J46-38	SW7-3: OFF
		ENCIFDI0	Data input ENCIFDI0 of ENCIF	J49-44	
		ETH3_RXD2	RXD2 of Ethernet port 3		SW7-3: ON
H3	P01_3/IRQ01_3/CS3#/DACK/CTS5#/RXD1/SCL1/MISO1/DEE4/IIC_SCL1/ETH1_TXER/ETH3_RXDV/ESC_I2CCLK/SPI_MISO2/MDAT00/ADTRG1#/MBX_HINT#/ENCIFOE4	CS3#	CS3# of external bus	J46-36	SW7-3: OFF
		ETH3_RXDV	RXDV of Ethernet port 3		SW7-3: ON
H4	P01_0/IRQ01_0/A0/MTIOC1A/MTIOC3A/GTIOC0_4A/GTADSM4_0/DE4/TXD E0/ETH3_RXD1/SPI_SSL21/HA0/ENCIFDO0	A0	Address A0 of external bus	J46-1	SW7-3: OFF
		GTIOC0_4A	Input/output GTIOC0_4A of GPT	J49-39	SW7-3: OFF, SW9-5: ON
		ENCIFDO0	Data output ENCIFDO0 of ENCIF	J49-43	SW7-3: OFF, SW9-5: OFF
		ETH3_RXD1	RXD1 of Ethernet port 3		SW7-3: ON
H5	VSS				
H6	VSS				
H7	—				
H8	—				
H9	—				
H10	—				
H11	—				
H12	—				
H13	—				
H14	—				
H15	—				
H16	—				
H17	—				
H18	—				
H19	—				
H20	DDR_VDDQ				
H21	VSS				
H22	DDR_DQA15	DDR_DQA15	Data DQ[14] of LPDDR4		
H23	DDR_DQA8	DDR_DQA8	Data DQ[9] of LPDDR4		
H24	VSS				
H25	DDR_DQA14	DDR_DQA14	Data DQ[8] of LPDDR4		

Table 5-9 List of RZ/T2N Pin Function Selections (9)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
J1	P02_5/IRQ02_5/A11/MTCLKD/MTIOC0D/GTIOC1_3B/GTADSM3_1/RXD2/SCL2/MISO2/DEE1/ETH4_RXD0/GMAC2_PTPTRG1/SPI_SSL32/MDAT12/MDAT40/HA11/ENCIFOE1	A11	Address A11 of external bus	J46-25	SW7-4: OFF
		GTIOC1_3B	Input/output GTIOC1_3B of GPT	J50-38	SW7-4: OFF, SW9-6: ON
		ENCIFOE1	Output enable ENCIFOE1 of ENCIF	J50-42	SW7-4: OFF, SW9-6: OFF
		ETH4_RXD0	RXD0 of Ethernet port 4		SW7-4: ON
J2	P02_1/IRQ02_1/WE3#/AH#/MTIC5W/MTIOC7C/GTIOC1_1A/GTADSM1_1/S1#/CTS1#/RTS1#/RXD3/SCL3/MISO3/TXDE5/ETH4_TXD2/GMAC0_PTPTRG0/ESC_LATCH0/SPI_SSL30/SPI_SL00/HWR3#/ENCIFDO5	IRQ02_1	IRQ of PMOD1	J34-7	SW7-4: OFF
		AH#	AH# of external bus	J47-40	
		ETH4_TXD2	TXD2 of Ethernet port 4		SW7-4: ON
J3	P02_0/IRQ02_0/WE2#/MTIC5V/MTIOC7A/GTIOC1_1B/GTADSM1_0/GTETRGD/TXD1/SDA1/MOSI1/SCIEXTCLK/ETH4_TXD1/ETHSW_PTPOUT0/ESC_SYNC0/SPI_MOSI3/SD1_PWEN/HWR2#	GTETRGD	Trigger input D of GPT/POEG	J52-35	SW7-4: OFF
		ETH4_TXD1	TXD1 of Ethernet port 4		SW7-4: ON
J4	P01_7/IRQ01_7/D14/MTIC5U/MTIOC6D/GTIOC1_0B/GTADSM0_1/GTETRG C/CMTW1_TOC0/RXD1/SCL1/MISO1/ETH1_RXER/ETH4_TXD0/SPI_MISO3/SD1_WP/MDAT02/HD14	D14	Data D14 of external bus	J47-33	SW7-4: OFF
		MDAT02	Data MDAT02 of DSMIF	J49-26	
		ETH4_TXD0	TXD0 of Ethernet port 4		SW7-4: ON
J5	VCC1833_2				
J6	VCC1833_2				
J7	—				
J8	—				
J9	VDD				
J10	VSS				
J11	VSS				
J12	VDD				
J13	VDD				
J14	VSS				
J15	VSS				
J16	VDD				
J17	VDD				
J18	—				
J19	—				
J20	VSS				
J21	DDR_DQA12	DDR_DQA12	Data DQ[10] of LPDDR4		
J22	DDR_DQA11	DDR_DQA11	Data DQ[11] of LPDDR4		
J23	VSS				
J24	DDR_DQSA_T1	DDR_DQSA_T1	DQS1_T of LPDDR4		
J25	DDR_DQSA_C1	DDR_DQSA_C1	DQS1_C of LPDDR4		

Table 5-10 List of RZ/T2N Pin Function Selections (10)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
K1	VSS				
K2	P02_4/IRQ02_4/A10/MTCLKC/MTIOC0C/GTIOC1_3A/GTADSM3_0/SCK2/SCKE1/ETH4_RXCLK/GMAC1_PTPTRG1/SPI_SSL03/SPI_SSL33/MCLK12/MCLK40/HA10/ENCIFCK1	A10	Address A10 of external bus	J46-23	SW7-4: OFF
		GTIOC1_3A	Input/output GTIOC1_3A of GPT	J50-37	SW7-4: OFF, SW9-6: ON
		ENCIFCK1	Clock ENCIFCK1 of ENCIF	J50-41	SW7-4: OFF, SW9-6: OFF
		ETH4_RXCLK	RXCLK of Ethernet port 4		SW7-4: ON
K3	P03_1/IRQ03_1/A15/GTIOC3_3B/DE2/DEE5/IIC_SDA2/ETH0_CRS/ETH4_RXDV/ETHSW_PTPOUT3/ESC_SYNC1/SPI_MISO3/MDAT10/HA15/ENCIFOE5/SI3#/HDSL1_LINK	A15	Address A15 of external bus	J46-35	SW7-4: OFF
		MDAT10	Data MDAT10 of DSMIF	J50-22	
		ETH4_RXDV	RXDV of Ethernet port 4		SW7-4: ON
K4	P02_2/IRQ02_2/D15/MTIOC0A/MTIOC7B/GTIOC1_2A/GTADSM2_0/CTS1#/ETH4_TXD3/GMAC0_PTPTRG1/ESC_LED_RUN/ESC_LATCH1/SPI_SSL01/SPI_SSL31/SD1_PWEN/HD15	D15	Data D15 of external bus	J47-35	SW7-4: OFF
		ETH4_TXD3	TXD3 of Ethernet port 4		SW7-4: ON
K5	P02_3/IRQ02_3/A9/MTIOC0B/MTIOC7D/GTIOC1_2B/GTADSM2_1/DE1/ETH4_TXEN/GMAC1_PTPTRG0/ESC_LEDERR/SPI_SSL02/SPI_SSL32/SD1_IOVS/HA9	A9	Address A9 of external bus	J46-21	SW7-4: OFF
		ETH4_TXEN	TXEN of Ethernet port 4		SW7-4: ON
K6	VCC1833_2				
K7	—				
K8	—				
K9	VSS				
K10	VDD				
K11	VDD				
K12	VSS				
K13	VSS				
K14	VDD				
K15	VDD				
K16	VSS				
K17	VSS				
K18	—				
K19	—				
K20	DDR_VDDQ				
K21	DDR_DQA13	DDR_DQA13	Data DQ[13] of LPDDR4		
K22	VSS				
K23	DDR_DQA9	DDR_DQA9	Data DQ[15] of LPDDR4		
K24	DDR_DMIA1	DDR_DMIA1	DMI[1] of LPDDR4		
K25	VSS				

Table 5-11 List of RZ/T2N Pin Function Selections (11)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
L1	P03_3/IRQ03_3/TEND/CMTW1_TIC1/TXD1/SDA1/MOSI1/TXD3/SDA3/MOSI3/GMAC0_MDIO/GMAC1_MDIO/GMAC2_MDIO/ETHSW_MDIO/ESC_MDIO/ESWM_MDIO/ESC_LINKACT0/SD1_PWEN	GMAC1_MDIO	MDIO of Ethernet ports 3 and 4		
L2	P03_2/MD2/IRQ03_2/DACK/CMTW1_TOC1/RTCAT1HZ/DE2/TXDE4/ETH0_TXER/GMAC0_MDC/GMAC1_MDC/GMAC2_MDC/ETHSW_MDC/ESC_MDC/ESWM_MDC/SD1_IOVS/ENCIFDO4	MD2	Input of MD2 setting		
		GMAC1_MDC	MDC of Ethernet ports 3 and 4		
L3	P03_0/IRQ03_0/A14/GTIOC3_3A/CTS2#/SCKE5/IIC_SCL2/ETH0_COL/ETH4_RXD3/SPI_MOSI3/MCLK10/HA14/ENCIFCK5/TST_OUT3/HDSL0_MOSI2	A14	Address A14 of external bus	J46-33	SW7-4: OFF
		CTS2#	CTS2# of PMOD2	J35-1	
		MCLK10	Clock MCLK10 of DSMIF	J50-21	
		ETH4_RXD3	RXD3 of Ethernet port 4		SW7-4: ON, R331: Fit, R333: DNF
L4	P02_7/IRQ02_7/A13/MTIOC1B/MTIOC6C/GTIOC1_4B/GTADSM4_1/SS2#/CTS2#/RTS2#/RXDE1/ETH4_RXD2/MDAT11/MDAT42/HA13/ENCIFDI1/DUEI3	A13	Address A13 of external bus	J46-31	SW7-4: OFF
		RTS2#	RTS2# of PMOD2	J35-4	
		ENCIFDI1	Data input ENCIFDI1 of ENCIF	J50-44	
		ETH4_RXD2	RXD2 of Ethernet port 4		SW7-4: ON
L5	P02_6/IRQ02_6/A12/MTIOC1A/MTIOC6A/GTIOC1_4A/GTADSM4_0/TXD2/SDA2/MOSI2/TXDE1/ETH4_RXD1/GMAC2_PTPTRG0/ESC_LEDSTER/SPI_SL31/MCLK11/MCLK42/HA12/ENCIFDO1	A12	Address A12 of external bus	J46-27	SW7-4: OFF
		GTIOC1_4A	Input/output GTIOC1_4A of GPT	J50-39	SW7-4: OFF, SW9-6: ON
		ENCIFDO1	Data output ENCIFDO1 of ENCIF	J50-43	SW7-4: OFF, SW9-6: OFF
		ETH4_RXD1	RXD1 of Ethernet port 4		SW7-4: ON
L6	VCC1833_2				
L7	—				
L8	—				
L9	VDD				
L10	VSS				
L11	VSS				
L12	VSS				
L13	VSS				
L14	VSS				
L15	VSS				
L16	VDD				
L17	VDD				
L18	—				
L19	—				
L20	VSS				
L21	DDR_DQA10	DDR_DQA10	Data DQ[12] of LPDDR4		

L22	VSS				
L23	DDR_DQA1	DDR_DQA1	Data DQ[7] of LPDDR4		
L24	DDR_DQA3	DDR_DQA3	Data DQ[0] of LPDDR4		
L25	VSS				

Table 5-12 List of RZ/T2N Pin Function Selections (12)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
M1	P04_1/IRQ04_1/GTIOC1_1A/SS0#/CT S0#/RST0#/DEE1/SD1_DATA1/MDAT 00/MDAT30/ENCIFOE1/DUEI5/HDSL1 _MISO1	GTIOC1_1A	Input/output GTIOC1_1A of GPT	J51-30	SW7-1: OFF
		SD1_DATA1	Data DATA1 of SDHI ch1 (microSD)	J27-8	SW7-1: ON
M2	P03_5/IRQ03_5/A25/GTETRGSB/RXD 3/SCL3/MISO3/RXDE5/ETH4_RXER/E SWM_PHYLINK1/HPSW_PHYLINK1/S PI_MISO0/SPI_SSL30/SD1_WP/MDAT 11/MCLK30/ENCIFDI5	A25	Address A25 of external bus	J46-24	SW7-4: OFF
		ESWM_PHYLIN K1	PHYLINK1 of Ethernet port 4		SW7-4: ON
M3	P03_7/IRQ03_7/GTIOC1_0B/RXD0/SC L0/MISO0/DEE0/IIC_SCL0/SD1_CMD/ MDAT02/MDAT32/ENCIFOE0/TST_O UT4/HDSL1_CLK1	GTIOC1_0B	Input/output GTIOC1_0B of GPT	J51-29	SW7-1: OFF
		SD1_CMD	CMD of SDHI ch1 (microSD)	J27-3	SW7-1: ON
M4	P03_4/ETH4_REFCLK/RMII4_REFCL K/IRQ03_4/A24/GTETRGSB/TXDE5/E SC_RESETOUT#/SPI_MOSI0/SPI_RS PCK3/SD1_CD/MCLK11/ENCIFDO5	A24	Address A24 of external bus	J46-22	SW7-4: OFF
		ETH4_REFCLK	REFCLK of Ethernet port 4		SW7-4: ON
M5	VSS				
M6	VSS				
M7	—				
M8	—				
M9	VSS				
M10	VDD				
M11	VSS				
M12	VSS				
M13	VSS				
M14	VSS				
M15	VSS				
M16	VSS				
M17	VSS				
M18	—				
M19	—				
M20	DDR_VDDQ				
M21	DDR_DMIA0	DDR_DMIA0	DMI[0] of LPDDR4		
M22	DDR_DQA7	DDR_DQA7	Data DQ[5] of LPDDR4		
M23	VSS				
M24	DDR_DQSA_C0	DDR_DQSA_C0	DQS0_C of LPDDR4		
M25	DDR_DQSA_T0	DDR_DQSA_T0	DQS0_T of LPDDR4		

Table 5-13 List of RZ/T2N Pin Function Selections (13)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
N1	VSS				
N2	P03_6/IRQ03_6/GTIOC1_0A/SCK0/SCKE0/SD1_CLK/MCLK02/MCLK32/ENCIFCK0/DUEI4/HDLS1_SMPL	GTIOC1_0A	Input/output GTIOC1_0A of GPT	J51-28	SW7-1: OFF
		SD1_CLK	CLK of SDHI ch1 (microSD)	J27-5	SW7-1: ON
N3	P04_0/IRQ04_0/GTIOC1_1B/TXD0/SDA0/MOSI0/SCKE1/IIC_SDA0/SD1_DATA0/MCLK00/MCLK30/ENCIFCK1/SI4#/HDLS1_SEL1	GTIOC1_1B	Input/output GTIOC1_1B of GPT	J51-31	SW7-1: OFF
		SD1_DATA0	Data DATA0 of SDHI ch1 (microSD)	J27-7	SW7-1: ON
N4	P04_2/IRQ04_2/GTIOC1_2A/CTS0#/TXDE2/SD1_DATA2/MCLK01/MCLK31/ENCIFDO2/TST_OUT5/HDLS1_MOSI1	GTIOC1_2A	Input/output GTIOC1_2A of GPT	J51-32	SW7-1: OFF
		SD1_DATA2	Data DATA2 of SDHI ch1 (microSD)	J27-1	SW7-1: ON
N5	VCC1833_6				
N6	VCC1833_6				
N7	—				
N8	—				
N9	VDD				
N10	VSS				
N11	VSS				
N12	VSS				
N13	VSS				
N14	VSS				
N15	VSS				
N16	VDD				
N17	VCC18_PLL2				
N18	—				
N19	—				
N20	VSS				
N21	DDR_DQA2	DDR_DQA2	Data DQ[6] of LPDDR4		
N22	VSS				
N23	DDR_DQA5	DDR_DQA5	Data DQ[2] of LPDDR4		
N24	DDR_DQA4	DDR_DQA4	Data DQ[1] of LPDDR4		
N25	VSS				

Table 5-14 List of RZ/T2N Pin Function Selections (14)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
P1	P04_5/IRQ04_5/GTIOC5_1B/CMTW0_TOC0/RXD1/SCL1/MISO1/ESC_LINKA CT0/CANRX0/SPI_MISO1/SD0_CMD/NAND_RE#/HSPI_CS#/TST_OUT6/HD SL1_MISO2	SD0_CMD	Command CMD of SDHI ch0 (eMMC)		SW7-7: ON, SW7-8: ON
		NAND_RE#	RE# of NANDC		SW7-7: OFF, SW7-8: ON
		HSPI_CS#	CS# of SHOSTIF	J45-4	SW7-7: OFF, SW7-8: OFF
P2	P04_4/IRQ04_4/GTIOC5_1A/CMTW0_TIC0/SCK1/GMAC0_PTPTRG0/ESC_LATCH0/SPI_RSPCK1/SD0_CLK/NAND_WE#/HSPI_INT#/DUEI6/HD SL1_SEL2	SD0_CLK	Clock CLK of SDHI ch0 (eMMC)		SW7-7: ON, SW7-8: ON
		NAND_WE#	WE# of NANDC		SW7-7: OFF, SW7-8: ON
		HSPI_INT#	INT# of SHOSTIF	J45-2	SW7-7: OFF, SW7-8: OFF
P3	P04_3/IRQ04_3/GTIOC1_2B/DE0/RXD E2/SD1_DATA3/MDAT01/MDAT31/ENCIFDI2/SI5#/HD SL1_CLK2	GTIOC1_2B	Input/output GTIOC1_2B of GPT	J51-33	SW7-1: OFF
		SD1_DATA3	Data DATA3 of SDHI ch1 (microSD)	J27-2	SW7-1: ON
P4	P04_6/IRQ04_6/GTIOC2_4A/GTIOC5_2A/CMTW0_TIC1/TXD1/SDA1/MOSI1/ESC_LINKACT1/CANTX0/SPI_MOSI1/SD0_DATA0/NAND_IO0/HSPI_IO0/SI6#/HD SL1_MOSI2	SD0_DATA0	Data DATA0 of SDHI ch0 (eMMC)		SW7-7: ON, SW7-8: ON
		NAND_IO0	Data IO0 of NANDC		SW7-7: OFF, SW7-8: ON
		HSPI_IO0	Data IO0 of SHOSTIF	J45-12	SW7-7: OFF, SW7-8: OFF
P5	VSS				
P6	VSS				
P7	—				
P8	—				
P9	VSS				
P10	VDD				
P11	VSS				
P12	VSS				
P13	VSS				
P14	VSS				
P15	VSS				
P16	VSS				
P17	VSS				
P18	—				
P19	—				
P20	DDR_VDDQ				
P21	VSS				
P22	DDR_DQA0	DDR_DQA0	Data DQ[4] of LPDDR4		
P23	VSS				
P24	DDR_DQA6	DDR_DQA6	Data DQ[3] of LPDDR4		
P25	VSS				

Table 5-15 List of RZ/T2N Pin Function Selections (15)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
R1	P05_2/IRQ05_2/GTIOC1_3B/GTIOC5_0A/CMTW1_TIC1/SCK2/TXDE5/ESC_LED RUN/SPI_RSPCK2/SD0_DATA4/NAND_IO4/HSPI_CK/ENCIFDO5/HDSL2_CLK1	SD0_DATA4	Data DATA4 of SDHI ch0 (eMMC)		SW7-7: ON, SW7-8: ON
		NAND_IO4	Data IO4 of NANDC		SW7-7: OFF, SW7-8: ON
		HSPI_CK	CK of SHOSTIF	J45-3	SW7-7: OFF, SW7-8: OFF, R188: DNF
		ENCIFDO5	Data output ENCIFDO5 of ENCIF	J51-48	SW7-7: OFF, SW7-8: OFF, R188: Fit
R2	P05_0/IRQ05_0/GTIOC3_4A/GTIOC5_3A/CMTW1_TIC0/CTS1#/SCKE5/ESC_LEDERR/CANTXDP0/SPI_SSL11/SD0_DATA2/NAND_IO2/HSPI_IO2/ENCIFCK5/TST_OUT7/HDSL2_SMPL	SD0_DATA2	Data DATA2 of SDHI ch0 (eMMC)		SW7-7: ON, SW7-8: ON
		NAND_IO2	Data IO2 of NANDC		SW7-7: OFF, SW7-8: ON
		HSPI_IO2	Data IO2 of SHOSTIF	J45-10	SW7-7: OFF, SW7-8: OFF
		ENCIFCK5	Clock ENCIFCK5 of ENCIF	J51-46	
R3	P04_7/IRQ04_7/GTIOC2_4B/GTIOC5_2B/CMTW0_TOC1/SS1#/CTS1#/RTS1#/ESC_RESETOUT#/CANRXDP0/SPI_DDL10/SD0_DATA1/NAND_IO1/HSPI_IO1/DUEI7/HDSL2_LINK	SD0_DATA1	Data DATA1 of SDHI ch0 (eMMC)		SW7-7: ON, SW7-8: ON
		NAND_IO1	Data IO1 of NANDC		SW7-7: OFF, SW7-8: ON
		HSPI_IO1	Data IO1 of SHOSTIF	J45-11	SW7-7: OFF, SW7-8: OFF
R4	P05_1/IRQ05_1/GTIOC4_4B/GTIOC5_3B/CMTW1_TOC0/DE1/DEE5/ETHSW_PTPOUT0/ESC_SYNC0/SPI_SSL12/SPI_RSPCK0/SD0_DATA3/NAND_IO3/HSPI_IO3/ENCIFOE5/SI7#	SD0_DATA3	Data DATA3 of SDHI ch0 (eMMC)		SW7-7: ON, SW7-8: ON
		NAND_IO3	Data IO3 of NANDC		SW7-7: OFF, SW7-8: ON
		HSPI_IO3	Data IO3 of SHOSTIF	J45-9	SW7-7: OFF, SW7-8: OFF
		P05_1	RST of PMOD2	J35-8	
		ENCIFOE5	Output enable ENCIFOE5 of ENCIF	J51-47	
R5	VCC1833_5				
R6	VCC1833_5				
R7	—				
R8	—				
R9	VCC18_PLL0				
R10	VSS				
R11	VSS				
R12	VSS				
R13	VSS				
R14	VSS				
R15	VSS				
R16	VDD				
R17	VDD				
R18	—				

R19	—				
R20	VSS				
R21	DDR_CSA0	DDR_CSA0	CS1 of LPDDR4		Unused
R22	DDR_CAA0	DDR_CAA0	CA[3] of LPDDR4		
R23	VSS				
R24	DDR_CKA_C	DDR_CKA_C	CK_C of LPDDR4		
R25	DDR_CKA_T	DDR_CKA_T	CK_T of LPDDR4		

Table 5-16 List of RZ/T2N Pin Function Selections (16)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
T1	VSS				
T2	P05_5/IRQ05_5/GTIOC2_3B/SS2#/CT S2#/RTS2#/RXD2/SCL2/MISO2/ETH0 _CRS/SPI_SSL20/SD0_DATA7/NAND _IO7/MDAT00/HSPI_IO6/HDSL2_MOS I1	SD0_DATA7	Data DATA7 of SDHI ch0 (eMMC)		SW7-7: ON, SW7-8: ON
		NAND_IO7	Data IO7 of NANDC		SW7-7: OFF, SW7-8: ON
		HSPI_IO6	Data IO6 of SHOSTIF	J45-6	SW7-7: OFF, SW7-8: OFF
		IRQ05_5	IRQ of PMOD2	J35-7	
T3	P05_3/IRQ05_3/GTIOC5_0B/CMTW1_ TOC1/RXD2/SCL2/MISO2/RXDE5/IIC_ SCL2/ETH0_TXER/ETH1_RXER/SPI_ MISO2/SD0_DATA5/NAND_IO5/HSPI_ IO4/ENCIFDI5/HDSL2_SEL1	SD0_DATA5	Data DATA5 of SDHI ch0 (eMMC)		SW7-7: ON, SW7-8: ON
		NAND_IO5	Data IO5 of NANDC		SW7-7: OFF, SW7-8: ON
		HSPI_IO4	Data IO4 of SHOSTIF	J45-8	SW7-7: OFF, SW7-8: OFF
		RXD2	RXD2 of PMOD2	J35-3	
		ENCIFDI5	Data input ENCIFDI5 of ENCIF	J51-49	
T4	P05_4/IRQ05_4/GTIOC2_3A/TXD2/SD A2/MOSI2/IIC_SDA2/ETH0_RXER/SPI_ MOSI2/SD0_DATA6/NAND_IO6/MCL K00/HSPI_IO5/HDSL2_MISO1	SD0_DATA6	Data DATA6 of SDHI ch0 (eMMC)		SW7-7: ON, SW7-8: ON
		NAND_IO6	Data IO6 of NANDC		SW7-7: OFF, SW7-8: ON
		HSPI_IO5	Data IO5 of SHOSTIF	J45-7	SW7-7: OFF, SW7-8: OFF
		TXD2	TXD2 of PMOD2	J35-2	
T5	VSS				
T6	VSS				
T7	—				
T8	—				
T9	VSS				
T10	VSS				
T11	VDD				
T12	VDD				
T13	VDD				
T14	VDD				
T15	VSS				
T16	VSS				
T17	VSS				
T18	—				
T19	—				
T20	DDR_VDDQ				
T21	VSS				
T22	DDR_CAA2	DDR_CAA2	CA[1] of LPDDR4		
T23	DDR_CAA1	DDR_CAA1	CA[0] of LPDDR4		
T24	DDR_CKEA0	DDR_CKEA0	CKE0 of LPDDR4		
T25	VSS				

Table 5-17 List of RZ/T2N Pin Function Selections (17)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
U1	P06_0/IRQ06_0/CS3#/GTIOC1_0A/SS3#/CTS3#/RTS3#/ETH1_RXER/ESC_LEDSTER/CANRXDP1/SPI_SSL00/TST_OUT4/HDSL2_MISO2	IRQ06_0	MDINT of Ethernet port 3		
U2	P05_7/IRQ05_7/CS2#/GTIOC1_3A/SCK3/SCKE5/ETH1_TXER/ESC_RESETOUT#/SPI_RSPCK0/MCLK00/ENCIFCK5/DUEI4/HDSL2_SEL2	ESC_RESETOUT#	RESETOUT# of Ethernet port 0		SW12-3: OFF
			RESETOUT# of Ethernet port 2		SW12-4: OFF
U3	P05_6/IRQ05_6/CTS2#/TXD2/SDA2/MOSI2/ETH2_COL/SPI_SSL21/SD0_RST#/NAND_WP#/MCLK01/HSPI_IO7/HDSL2_CLK2	SD0_RST#	Reset RST# of SDHI ch0 (eMMC)		SW7-7: ON, SW7-8: ON
		NAND_WP#	WP# of NANDC		SW7-7: OFF, SW7-8: ON
		HSPI_IO7	Data IO7 of SHOSTIF	J45-5	SW7-7: OFF, SW7-8: OFF
U4	P06_3/IRQ06_3/D29/GTIOC1_1B/GTIOC2_0B/CTS3#/GMAC1_PTPTRG0/ESC_LEDERR/CANTXDP1/SPI_SSL01/HD29/TST_OUT5/HDSL3_SMPL	ESC_LEDERR	ERR control of LED4		
U5	P06_1/IRQ06_1/CS5#/GTIOC1_3B/DEE5/TXD3/SDA3/MOSI3/ETH1_CRS/CANTX1/SPI_MOSI0/MDAT00/ENCIFOE5/SI4#/HDSL2_MOSI2	MDAT00	Data MDAT00 of DSMIF	J49-22	
U6	VCC33				
U7	—				
U8	—				
U9	VDD				
U10	VDD				
U11	VSS				
U12	VCC18_PLL3				
U13	VCC18_PLL4				
U14	VSS				
U15	VDD				
U16	VCC33				
U17	VDD				
U18	—				
U19	—				
U20	VSS				
U21	DDR_CAA4	DDR_CAA4	CA[2] of LPDDR4		
U22	DDR_CAA3	DDR_CAA3	CA[4] of LPDDR4		
U23	VSS				
U24	DDR_CSA1	DDR_CSA1	CS0 of LPDDR4		
U25	DDR_CKEA1	DDR_CKEA1	CKE1 of LPDDR4		Unused

Table 5-18 List of RZ/T2N Pin Function Selections (18)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
V1	P06_5/IRQ06_5/D31/MTIOC2B/GTIOC1_2A/GTIOC2_1B/SCK4/SPI_SSL03/MCLK30/HD31/DUIE6/HD31_SEL1	P06_5	WAKE# signal of PCIe	J6-B11	
V2	P06_4/IRQ06_4/D30/GTIOC1_1A/GTIOC2_1A/DE3/GMAC1_PTPTRG1/SPI_SSL02/MDAT01/HD30/SI5#/HD31_CLK1	P06_4	CLKREQ output when the PCIe is an endpoint	J6-B12	SW12-6: OFF
		IRQ06_4	PRSNT2 input when the PCIe is a root complex	J6-B17	SW12-6: ON
V3	P06_2/IRQ06_2/D28/GTIOC1_0B/GTIOC2_0A/RXD3/SCL3/MISO3/ETH1_COL/CANRX1/SPI_MISO0/MCLK01/HD28/DUEI5/HD31_LINK	MCLK01	Clock MCLK01 of DSMIF	J49-23	
V4	P06_7/IRQ06_7/GTIOC1_4B/GTIOC2_2B/TXD4/SDA4/MOSI4/RXDE5/CANTX0/SD1_IOVS/MDAT02/ENCIFDI5/SI6#/HD31_MOSI1	TXD4	TXD4 of SCI (RMW)	J40-3	
V5	P07_1/IRQ07_1/POE4#/CTS4#/DEE1/ETH4_RXER/ETHSW_TDMAOUT1/ESC_LEDERR/CANRXDP0/SPI_SSL22/MCLK31/ADTRG0#/ENCIFOE1/TST_OUT7/HD31_SEL2	ETH4_RXER	RXER of Ethernet port 4		R331: DNF, R333: Fit
V6	VCC33				
V7	—				
V8	—				
V9	—				
V10	—				
V11	—				
V12	—				
V13	—				
V14	—				
V15	—				
V16	—				
V17	—				
V18	—				
V19	—				
V20	DDR_VDDQ				
V21	DDR_CALIBRATION	DDR_CALIBRATION	Connected to VDDQ1V1 via a 240-Ω resistor		
V22	DDR_RETENTION	DDR_RETENTION	Connected to VDDQ1V1		
V23	DDR_RESET#	DDR_RESET#	RESET# of LPDDR4		
V24	DDR_CAA5	DDR_CAA5	CA[5] of LPDDR4		
V25	VSS				

Table 5-19 List of RZ/T2N Pin Function Selections (19)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
W1	VSS				
W2	P07_0/IRQ07_0/POE0#/GTIOC1_2B/S4#/CTS4#/RTS4#/IIC_SDA1/ETH4_TXER/ESC_RESETOUT#/SPI_SSL13/MDAT30/ADTRG2#/DUEI7/HDSL3_CLK2/POUTA	ESC_RESETOUT#	RESETOUT# of Ethernet port 0		SW12-3: ON
			RESETOUT# of Ethernet port 1		
			RESETOUT# of Ethernet port 2		SW12-4: ON
W3	P06_6/IRQ06_6/GTIOC1_4A/GTIOC2_2A/RXD4/SCL4/MISO4/TXDE5/CANRX0/SD1_PWEN/MCLK02/ENCIFDO5/ST_OUT6/HDSL3_MISO1	RXD4	RXD4 of SCI (RMW)	J40-2	
W4	P07_4/IRQ07_4/A16/POE11#/GTIOC1_1B/SCKE1/GMAC2_PTPTRG0/ETHSW_TDMAOUT0/ESC_LED RUN/MDAT22/ENCIFCK1/HDSL3_MOSI2	P07_4	User DIP switch SW6-3		
W5	P07_2/IRQ07_2/POE8#/DE4/TXDE1/ETH4_CRS/ETHSW_PTPOUT2/ESC_SYNC0/CANTXDP0/SPI_SSL23/MDAT31/ADTRG1#/ENCIFDO1/SI7#/POUTB	P07_2	User DIP switch SW6-1		
W6	VSS				
W7	—				
W8	—				
W9	—				
W10	—				
W11	—				
W12	—				
W13	—				
W14	—				
W15	—				
W16	—				
W17	—				
W18	—				
W19	—				
W20	VSS				
W21	VSS				
W22	VSS				
W23	VSS				
W24	VSS				
W25	VSS				

Table 5-20 List of RZ/T2N Pin Function Selections (20)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
Y1	P07_5/IRQ07_5/MTCLKC/MTIOC0C/GTETRG/TXDE6/IIC_SDA0/ETH0_TXER/CANTX0/SPI_MOSI3/MCLK21/ENCIFDO6/DUEI0/HDLSL6_LINK	P07_5	User DIP switch SW6-4		
Y2	P07_6/IRQ07_6/A23/GTETRGA/ETH0_RXER/CANRXDP0/SPI_SSL30/TST_OUT0/HDLSL6_SMPL	IRQ07_6	MDINT of Ethernet port 2		
Y3	P07_3/IRQ07_3/POE10#/GTIOC1_0A/RXDE1/IIC_SCL1/ETH4_COL/GMAC2_PTPTRG1/ETHSW_PTPOUT3/ESC_SYNC1/MCLK22/ENCIFDI1/HDLSL3_MISO2/POUTZ	P07_3	User DIP switch SW6-2		
Y4	P07_7/IRQ07_7/A22/MTCLKD/MTIOC0D/GTIOC0_1B/GTIOC4_0B/GTETRG_C/SCK5/DEE6/IIC_SCL0/ETH0_CRS/CANRX0/SPI_MISO3/MCLK32/ENCIFOE6	GTETRGC	Trigger input C of GPT/POEG	J51-35	
Y5	P08_3/IRQ08_3/A18/TXD5/SDA5/MOSI5/ETH1_CRS/ETHSW_TDMAOUT2/ESC_LINKACT0/CANRXDP1/SPI_SSL33/SIO#0/HDLSL6_CLK2	ESC_LINKACT0	LINKACT0 control of LED5		
Y6	VSS				
Y7	VCC33				
Y8	VCC33				
Y9	VSS				
Y10	VDD18ABG				
Y11	NCPOUT	NCPOUT	A 1-μF capacitor is inserted between the analog input-output pin and GND.		
Y12	VSS_USB				
Y13	VSS				
Y14	PCIE_VDDA_RX				
Y15	PCIE_VDDA_TX				
Y16	VSS				
Y17	PCIE_VCC18A_CMN				
Y18	VSS				
Y19	VSS				
Y20	VCC18_ADC1				
Y21	VCC18_ADC2				
Y22	VCC18_OTP				
Y23	AVCC18_TSU				
Y24	VSS				
Y25	VSS				

Table 5-21 List of RZ/T2N Pin Function Selections (21)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
AA1	P08_0/IRQ08_0/A21/MTIOC0A/MTIOC6A/GTIOC4_1A/GTETRGD/SS5#/CTS5#/RTS5#/SCKE6/ETH0_COL/CANRX1/SPI_RSPCK3/MDAT32/ENCIFCK6/DUEI1/HDSL6_SEL1	CANRX1	RX of CAN interface		
AA2	P08_2/IRQ08_2/A19/MTIOC0B/MTIOC6C/GTETRGSB/DE5/RXDE6/GMAC0_PTPTRG1/ESC_LATCH1/CAN_TX1/SPI_SSL32/SD0_WP/MDAT21/ENCIFDI6	CANTX1	TX of CAN interface		
AA3	P08_1/IRQ08_1/A20/GTETRGSB/CT55#/GMAC0_PTPTRG0/ESC_LATC_H0/CANTXDP0/SPI_SSL31/SD0_CD/TST_OUT1/HDSL6_MISO1	IRQ08_1	User push switch SW3		
AA4	P08_5/MDW0/IRQ08_5/A6/SCKE3/SD1_PWEN/NAND_ALE/HA6/ENCIFCK3/DUIE0	MDW0	Input of MDW0 setting		
		IRQ08_5	IRQ of SPI expansion connector	J26-2	SW9-3: OFF
		A6	Address A6 of external bus	J46-15	
		NAND_ALE	ALE of NANDC		SW9-3: ON
AA5	P09_0/MDV0/IRQ09_0/WE0#/TXDE7/ETHSW_PTPOUT1/ESC_SYNC1/SD0_IOVS/HWR0#/ENCIFDO7/DUEI1	MDV0	Input of MDV0 setting		
		WE0#	WE0# of external bus	J47-36	
		ENCIFDO7	Data output ENCIFDO7 of ENCIF	J52-48	
AA6	P09_3/IRQ09_3/CS0#/MTIOC2A/GTIOC4_3A/SS0#/CTS0#/RST0#/RXDE6/SCKE4/ETHSW_LPI0/ESWM_MPI_NTO/SD0_CD/NAND_RY_BY0#/MCLK31/HCS0#/ENCIFCK4/ENCIFDI6/HDSL6_MOSI1	CS0#	CS0# of external bus	J46-32	SW9-3: OFF
		MCLK31	Clock MCLK31 of DSMIF	J52-23	
		NAND_RY_BY0#	Ready/Busy RY_BY0# of NANDC		SW9-3: ON
AA7	VSS				
AA8	VSS				
AA9	VSS				
AA10	VSS				
AA11	VCC33_USB				
AA12	AVCC18_USB				
AA13	VSS				
AA14	PCIE_VDDA_RX				
AA15	PCIE_VDDA_TX				
AA16	VSS				
AA17	VSS				
AA18	VREFH0				
AA19	VCC18_ADC0				
AA20	VREFH1				
AA21	VREFH2				
AA22	VSS				
AA23	VSS				
AA24	VSS				
AA25	VSS				

Table 5-22 List of RZ/T2N Pin Function Selections (22)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
AB1	VSS				
AB2	P08_4/IRQ08_4/A17/RXD5/SCL5/MISO5/ETH1_COL/ETHSW_TDMAOUT3/ESC_LINKACT1/CANTXDP1/SI1#/HDSL6_SEL2	ESC_LINKACT1	LINKACT1 control of LED6		
AB3	P08_7/MDD/IRQ08_7/A8/DEE7/SD0_PWEN/NAND_CE0#/HA8/ENCIFOE7/SIO#	MDD	Input of MDD setting		
		A8	Address A8 of external bus	J46-19	SW9-3: OFF
		ENCIFOE7	Output enable ENCIFOE7 of ENCIF	J52-47	
		NAND_CE0#	CE0# of NANDC		SW9-3: ON
AB4	P09_5/MDV2/IRQ09_5/A1/TXDE3/TXDE4/ETHSW_LPI2/HA1/ENCIFDO3/ENCIFDO4/DUEI2	MDV2	Input of MDV2 setting		
		A1	Address A1 of external bus	J46-3	
		ENCIFDO4	Data output ENCIFDO4 of ENCIF	J49-48	
AB5	P10_3/IRQ10_3/MTIOC6D/GTIOC3_0B/RXD2/SCL2/MISO2/MDAT22/TST_OUT2	P10_3	Control of user LED3 (LED11)		
AB6	P10_6/IRQ10_6/MTIOC7B/GTIOC3_2A/CMTW0_TIC1/CTS2#/SCKE2/ENCIFCK2/TST_OUT3	P10_6	GPIO connector	J55-6	
AB7	P11_2/IRQ11_2/GTIOC0_3B/TXD1/SDA1/MOSI1/IIC_SDA0/ESC_I2CDA/TA/USB_EXICEN	TXD1	TXD1 of USB-to-serial conversion		
AB8	P11_3/IRQ11_3/POE4#/GTETRGD/RXD0/SCL0/MISO0/IIC_SCL1	RXD0	RXD0 of USB-to-serial conversion		
AB9	TRST#	TRST#	Test reset input		
AB10	VSS				
AB11	VSS_USB				
AB12	USB_RREF				
AB13	VSS				
AB14	PCIE_VCC18A				
AB15	PCIE_REFCLKN	PCIE_REFCLKN	Reference clock N of PCIe		
AB16	VSS				
AB17	RES#	RES#	Reset input		
AB18	VSS				
AB19	VSS				
AB20	VSS				
AB21	VSS				
AB22	AN204	AN204	Input to A/D converter (AN204)	J49-9	
AB23	VSS				
AB24	VSS				
AB25	VSS				

Table 5-23 List of RZ/T2N Pin Function Selections (23)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
AC1	P08_6/MDW1/IRQ08_6/A7/DEE3/SD1_IOVS/NAND_CLE/HA7/ENCIFOE3/TST_OUT0	MDW1	Input of MDW1 setting		
		A7	Address A7 of external bus	J46-17	SW9-3: OFF
		NAND_CLE	CLE of NANDC		SW9-3: ON
AC2	P09_1/MDV1/IRQ09_1/WE1#/SCKE7/NAND_CE1#/HWR1#/ENCIFCK7/TST_OUT1	MDV1	Input of MDV1 setting		
		WE1#	WE1# of external bus	J47-38	
		ENCIFCK7	Clock ENCIFCK7 of ENCIF	J52-46	
AC3	P09_7/MDV4/IRQ09_7/A3/SCKE6/ETHSW_TDMAOUT1/ESC_LINKACT1/ESC_LINKACT2/HA3/ENCIFCK6/SI2#/POUTA	MDV4	Input of MDV4 setting		
		A3	Address A3 of external bus	J46-7	
		ESC_LINKACT2	LINKACT2 control of LED7		R555: Fit
		ENCIFCK6	Clock ENCIFCK6 of ENCIF	J50-46	R555: DNF
AC4	P10_5/IRQ10_5/MTIOC7C/GTIOC3_1A/GTIOC4_2B/CMTW0_TOC0/SS2#/CTS2#/RTS2#/IIC_SDA2/DUEI3	P10_5	GPIO connector	J55-5	
AC5	P10_4/IRQ10_4/MTIOC7A/GTIOC3_1B/GTIOC4_2A/CMTW0_TIC0/TXD2/SDA2/MOSI2/SI2#	IRQ10_4	User push switch SW2		
AC6	P10_7/IRQ10_7/MTIOC7D/GTIOC3_2B/CMTW0_TOC1/DE2/DEE2/ENCIFOE2/SI3#	P10_7	GPIO connector	J55-7	
AC7	P12_0/TMS/IRQ12_0	TMS	TMS of debugging interface	J31-2	
AC8	P11_7/IRQ11_7/POE11#/GTIOC5_2A/GTETRGB/RTCAT1HZ/USB_OTG_ID/MBX_HINT#	GTETRGB	Trigger input B of GPT/POEG	J50-35	SW11-3: OFF, SW11-4: ON
		MBX_HINT#	HINT# of SHOSTIF	J45-13	
		USB_OTG_ID	ID of USB OTG interface		SW11-3: ON, SW11-4: OFF
AC9	P12_4/IRQ12_4/USB_VBUSIN	IRQ12_4	User push switch SW4		SW11-5: OFF, SW11-6: OFF, SW11-7: ON
		USB_VBUSIN	VBUSIN (USB function interface)		SW11-5: ON, SW11-6: OFF, SW11-7: OFF
			VBUSIN (USB OTG interface)		SW11-5: OFF, SW11-6: ON, SW11-7: OFF
AC10	VSS				
AC11	VSS_USB				
AC12	VCC18_USB				
AC13	VSS_USB				
AC14	VSS				
AC15	VSS				
AC16	PCIE_REFCLKP	PCIE_REFCLKP	Reference clock P of PCIe		
AC17	MDX	MDX	Input of MDX setting		
AC18	EXTCLKIN	EXTCLKIN	External clock input that is connected to a crystal oscillator		

AC19	VSS				
AC20	AN002	AN002	Input to A/D converter (AN002)	J56-11	
AC21	AN100	AN100	Input to A/D converter (AN100)	J56-9	
AC22	AN102	AN102	Input to A/D converter (AN102)	J56-7	
AC23	AN202	AN202	Input to A/D converter (AN202)	J56-3	
AC24	AN203	AN203	Input to A/D converter (AN203)	J56-2	
AC25	AN207	AN207	Input to A/D converter (AN207)	J52-9	

Table 5-24 List of RZ/T2N Pin Function Selections (24)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
AD1	P09_2/IRQ09_2/WAIT#/SCK0/RXDE3/RXDE4/NAND_RY_BY1#/HWAIT#/ENCIFDI3/ENCIFDI4/SI1#/HDCL6_CLK1	ENCIFDI4	Data input ENCIFDI4 of ENCIF	J49-49	
		WAIT#	WAIT# of external bus	J47-34	
AD2	P09_4/IRQ09_4/RD#/MTIOC2B/GTIOC4_3B/CTS0#/RXDE7/DEE4/ETHSW_LPI1/ESWM_MPINT1/SD0_WP/NAND_RY_BY2#/MDAT31/HRD#/ENCIFOE4/ENCIFDI7	NAND_RY_BY2#	Ready/Busy RY_BY2# of NANDC (unused)		SW7-7: OFF, SW7-8: ON
		MDAT31	Data MDAT31 of DSMIF	J52-24	Other than SW7-7: OFF, SW7-8: ON
		RD#	RD# of external bus	J46-39	
AD3	P09_6/MDV3/IRQ09_6/A2/DE0/TXD E6/ETHSW_TDMAOUT0/NAND_CE2#/HA2/ENCIFDO6/TST_OUT2	MDV3	Input of MDV3 setting		
		NAND_CE2#	CE2# of NANDC (unused)		SW7-7: OFF, SW7-8: ON
		A2	Address A2 of external bus	J46-5	Other than SW7-7: OFF, SW7-8: ON
		ENCIFDO6	Data output ENCIFDO6 of ENCIF	J50-48	
AD4	P10_2/IRQ10_2/MTIOC1B/MTIOC6B/GTIOC3_0A/GTIOC4_1B/SCK2/IIC_SCL2/MCLK22/DUEI2	P10_2	Control of user LED2 (LED10)		
AD5	P11_0/IRQ11_0/TXDE2/USB_VBUS EN/ENCIFDO2	USB_VBUSEN	VBUS control (USB host interface)		SW11-1: ON, SW11-2: OFF
			VBUS control (USB OTG interface)		SW11-1: OFF, SW11-2: ON
AD6	P11_1/IRQ11_1/GTIOC0_3A/RXD1/SCL1/MISO1/RXDE2/IIC_SCL0/ESC_I2CCLK/USB_OVRCUR/ENCIFDI2	RXD1	RXD1 of USB-to-serial conversion		
AD7	P11_5/CKIO/IRQ11_5/POE0#/GTIOC5_0A/GTETRGA/SCIEXTCLK/IIC_SCL2/NAND_RY_BY3#/HCKIO	CKIO	Clock CKIO of external bus	J47-2	E12: Open-circuit
		GTETRGA	Trigger input A of GPT/POEG	J49-35	E12: Short-circuit
AD8	P12_1/TDI/IRQ12_1	TDI	TDI of debugging interface	J31-8	
AD9	P12_3/TDO/IRQ12_3	TDO	TDO of debugging interface	J31-6	
AD10	VSS				
AD11	USB_DP	USB_DP	DP input/output of USB host or USB function interface	J2-3, J3-3	
			DP input/output of USB OTG interface	J4-3	E2: Short-circuit
AD12	VSS_USB				
AD13	VSS				
AD14	PCIE_RXDP	PCIE_RXDP	Receive data RXDP of PCIe	J6-A16	
AD15	VSS				
AD16	PCIE_TXDP	PCIE_TXDP	Transmit data TXDP of PCIe	J6-B14	
AD17	VSS				
AD18	XTAL	XTAL	Connected to a crystal resonator		Unused
AD19	VSS				
AD20	AN001	AN001	Input to A/D converter (AN001)	J56-12	

AD21	AN101	AN101	Input to A/D converter (AN101)	J56-8	
AD22	AN103	AN103	Input to A/D converter (AN103)	J56-6	
AD23	AN200	AN200	Input to A/D converter (AN200)	J56-5	
AD24	AN201	AN201	Input to A/D converter (AN201)	J56-4	
AD25	AN205	AN205	Input to A/D converter (AN205)	J50-9	

Table 5-25 List of RZ/T2N Pin Function Selections (25)

Pin	Pin Name	Pin Function	Description	Connector	Remarks
AE1	VSS				
AE2	P10_0/MDV5/IRQ10_0/A4/DEE6/ET HSW_TDMAOUT2/ESC_IRQ/NAND _CE3#/HA4/ENCIFOE6/POUTB	MDV5	Input of MDV5 setting		
		IRQ10_0	IRQ of SPI expansion connector	J26-13	
		A4	Address A4 of external bus	J46-9	
		ENCIFOE6	Output enable ENCIFOE6 of ENCIF	J50-47	
AE3	P10_1/MDB/IRQ10_1/A5/ETHSW_T DMAOUT3/ESC_RESETOUT#/ESC _LED3/HA5/POUTZ	MDB	Input of MDB setting		
		A5	Address A5 of external bus	J46-13	
		ESC_LED3	RUN control of LED3		
AE4	VSS				
AE5	P11_4/RSTOUT#/IRQ11_4/GTETR GSA/TXD0/SDA0/MOSI0/IIC_SDA1	TXD0	TXD0 of USB-to-serial conversion		
AE6	P11_6/IRQ11_6/IIC_SDA2/USB_OV RCUR	USB_OVRCUR	OVRCUR input of USB host interface		
AE7	VSS				
AE8	P12_2/TCK/IRQ12_2	TCK	TCK of debugging interface	J31-4	
AE9	BSCANP	BSCANP	Enabling of boundary scan		
AE10	VSS				
AE11	USB_DM	USB_DM	DM input/output of USB host or USB function interface	J2-2, J3-2	
			DM input/output of USB OTG interface	J4-2	E1: Short- circuit
AE12	VSS_USB				
AE13	VSS				
AE14	PCIE_RXDN	PCIE_RXDN	Receive data RXDN of PCIe	J6-A17	
AE15	VSS				
AE16	PCIE_TXDN	PCIE_TXDN	Transmit data TXDN of PCIe	J6-B15	
AE17	VSS				
AE18	EXTAL	EXTAL	Connected to a crystal resonator		Unused
AE19	VSS				
AE20	AN000	AN000	Input to potentiometer		SW14-1: ON, SW14-2: OFF
			Input to A/D converter (AN000)	J56-13	SW14-1: OFF, SW14-2: ON
AE21	AN003	AN003	Input to A/D converter (AN003)	J56-10	
AE22	VSS				
AE23	VSS				
AE24	AN206	AN206	Input to A/D converter (AN206)	J51-9	
AE25	VSS				

6. Circuitry for Configuration

6.1 Types of Configuration Circuits

Since multiple functions are assigned to single pins and each function has to be selected for use in the RZ/T2N, the functions to be used should be selected through the following methods on this board.

(1) Switches

DIP switches SW7 to SW14 are mounted for selecting functions.

(2) Jumper blocks

J1, J11 to J20, J22 to J25, J29, J39, J41, and J48 are mounted for selecting functions.

(3) Option links

The option links are as follows:

— Solder bridges and trace cuts

A solder bridge consists of two pads, which are insulated from each other at the time of shipment.

Conduction can be set up for such pads by connecting them with solder or the like. A trace cut is a thin copper trace that connects two pads and sets up conduction between them. Such pads can be insulated from each other by cutting the trace between the pads.

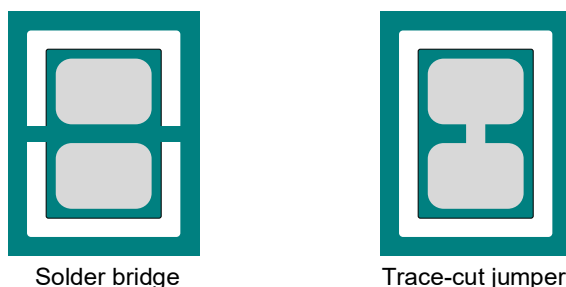


Figure 6-1 Solder Bridge and Trace Cut

— 0-Ω resistors

The functions to be used can be selected by changing the factory states of 0-Ω resistors to Fit or DNF.

The subsequent sections describe which peripheral functions of the multi-functional RZ/T2N signals are enabled or disabled through the settings of switches, jumper blocks, and option links. The connection information for ICs and headers other than the RZ/T2N will also be shown. **Text in bold blue type** in the tables indicates the initial state of the configuration on the board as shipped. For the positions of switches, jumper blocks, and option links, refer to "3.3 Arrangement of Components".

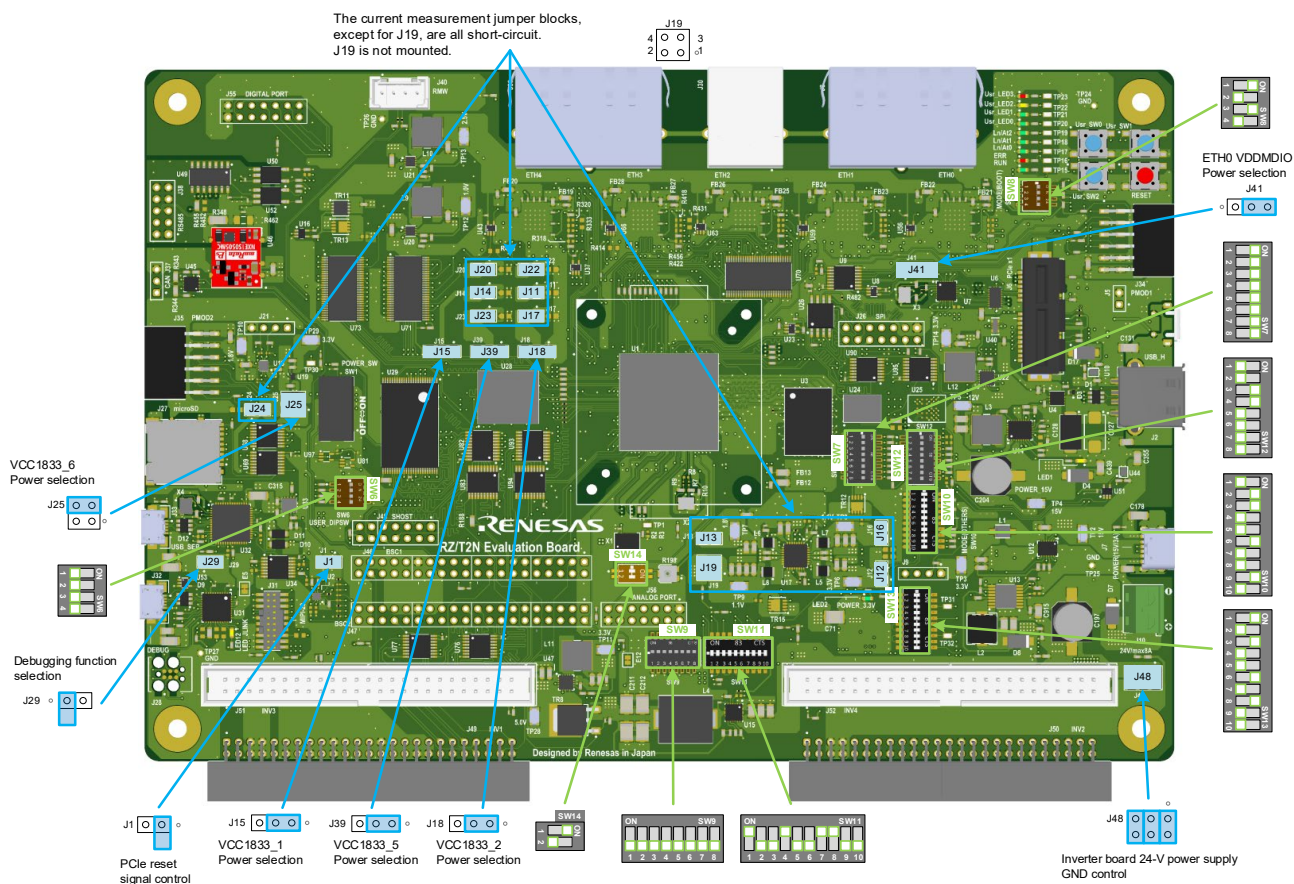
The settings of switches or jumper blocks should only be changed while the power is turned off.

When removing soldered components, do not apply a soldering iron to the board for more than 5 seconds. This time restriction is to avoid any damage to components mounted nearby on the board.

When modifying an option link, always check the related option links to ensure that no signal contention or short-circuit has occurred. Most of the RZ/T2N pins have multiplexed functions and some of the peripheral functions must be used exclusively of each other. Refer to the RZ/T2N Group Hardware Manual and this board's schematics for further information.

6.2 Configuration at Shipment

Figure 6-2 shows the state of switch settings and jumper block settings for the configuration at the time of shipment.



6.3 Configuration by Switches

This board is equipped with DIP switches SW7 to SW14 for selecting functions. The functions set by individual switches are explained below.

6.3.1 Mode Setting Switches SW8 and SW10

SW8 and SW10 are used to set the mode pins of the RZ/T2N. Table 6-1 lists the settings of SW8 and Table 6-2 lists the settings of SW10.

Table 6-1 Functions of Mode Setting Switch SW8

No.	Setting		Function																		
SW8-1 MD0	OFF	MD0 = H	The operating mode of the RZ/T2N is selected with the combination of SW8-1, SW8-2, and SW8-3 (MD0, MD1, and MD2).																		
	ON	MD0 = L																			
SW8-2 MD1	OFF	MD1 = H	<table><tr><td>SW8-1, SW8-2, SW8-3</td><td>Operating Mode</td></tr><tr><td>ON, ON, ON</td><td>xSPI0 boot mode (x1 boot serial flash)</td></tr><tr><td>OFF, ON, ON</td><td>xSPI0 boot mode (x8 boot serial flash)*</td></tr><tr><td>ON, OFF, ON</td><td>xSPI1 boot mode (x1 boot serial flash)</td></tr><tr><td>OFF, OFF, ON</td><td>eSD boot mode</td></tr><tr><td>ON, ON, OFF</td><td>eMMC boot mode</td></tr><tr><td>OFF, ON, OFF</td><td>SCI (UART) boot mode</td></tr><tr><td>ON, OFF, OFF</td><td>USB boot mode</td></tr><tr><td>OFF, OFF, OFF</td><td>Reserved (setting prohibited)</td></tr></table>	SW8-1, SW8-2, SW8-3	Operating Mode	ON, ON, ON	xSPI0 boot mode (x1 boot serial flash)	OFF, ON, ON	xSPI0 boot mode (x8 boot serial flash)*	ON, OFF, ON	xSPI1 boot mode (x1 boot serial flash)	OFF, OFF, ON	eSD boot mode	ON, ON, OFF	eMMC boot mode	OFF, ON, OFF	SCI (UART) boot mode	ON, OFF, OFF	USB boot mode	OFF, OFF, OFF	Reserved (setting prohibited)
	SW8-1, SW8-2, SW8-3	Operating Mode																			
ON, ON, ON	xSPI0 boot mode (x1 boot serial flash)																				
OFF, ON, ON	xSPI0 boot mode (x8 boot serial flash)*																				
ON, OFF, ON	xSPI1 boot mode (x1 boot serial flash)																				
OFF, OFF, ON	eSD boot mode																				
ON, ON, OFF	eMMC boot mode																				
OFF, ON, OFF	SCI (UART) boot mode																				
ON, OFF, OFF	USB boot mode																				
OFF, OFF, OFF	Reserved (setting prohibited)																				
MD1	ON	MD1 = L																			
SW8-3 MD2	OFF	MD2 = H																			
	ON	MD2 = L																			
SW8-4	Unused		— (At the time of shipment = OFF)																		

Note: This setting is prohibited because OctaFlash is mounted.

Table 6-2 Functions of Mode Setting Switch SW10

No.	Setting		Function
SW10-1	Unused		— (At the time of shipment = OFF)
SW10-2 MDV1	OFF	MDV1 = H	VCC1833_1 = 3.3-V (J15: 2-3 are short-circuit)
	ON	MDV1 = L	VCC1833_1 = 1.8-V (J15: 1-2 are short-circuit)
SW10-3 MDV2	OFF	MDV2 = H	VCC1833_2 = 3.3-V (J18: 2-3 are short-circuit)
	ON	MDV2 = L	VCC1833_2 = 1.8-V (J18: 1-2 are short-circuit)
SW10-4	Unused		— (At the time of shipment = OFF)
SW10-5	Unused		— (At the time of shipment = OFF)
SW10-6 MDV5	OFF	MDV5 = H	VCC1833_5 = 3.3-V (J39: 2-3 are short-circuit)
	ON	MDV5 = L	VCC1833_5 = 1.8-V (J39: 1-2 are short-circuit)
SW10-7 MDW0	OFF	MDW0 = H	The number of ATCM wait cycles of CPU0 in the Cortex-R52 is 1 wait cycle.
	ON	MDW0 = L	The number of ATCM wait cycles of CPU0 in the Cortex-R52 is 0 wait cycles.
SW10-8 MDW1	OFF	MDW1 = H	The number of ATCM wait cycles of CPU1 in the Cortex-R52 is 1 wait cycle.
	ON	MDW1 = L	The number of ATCM wait cycles of CPU1 in the Cortex-R52 is 0 wait cycles.
SW10-9 MDD	OFF	MDD = H	JTAG mode = JTAG authentication in hash mode
	ON	MDD = L	JTAG mode = Normal mode
SW10-10 MDB	OFF	MDB = H	Second boot CPU = Core 0 in the Cortex-A55
	ON	MDB = L	Second boot CPU = CPU0 in the Cortex-R52

6.3.2 Signal Function Selection Switches SW7, SW9, and SW11 to SW14

SW7, SW9, and SW11 to SW14 are used to select the functions of the signal lines. Table 6-3 to Table 6-8 list the settings of SW7, SW9, and SW11 to SW14.

Table 6-3 Signal Function Selection Switch SW7

No.	Setting		Function
SW7-1	OFF		P03_6, P03_7, P04_0 to P04_3, and P15_0 are used as control signals for inverter board INV3. (P15_0 is also used as a control signal for BSC2.)
	ON		P03_6, P03_7, P04_0 to P04_3, and P15_0 are used as control signals for the microSD card.
SW7-2	OFF		P23_1, P23_2, P23_4 to P23_7, P24_0 to P24_4, and P25_0 are used as control signals for inverter boards INV2, INV3, and INV4, BSC1, and the GPIO connector.
	ON		P23_1, P23_2, P23_4 to P23_7, P24_0 to P24_4, and P25_0 are used as control signals for Ethernet port 2.
SW7-3	OFF		P00_0 to P00_7, P01_0 to P01_5, P16_1, and P16_7 are used as control signals for inverter boards INV1 and INV4, BSC1, the SPI expansion connector, and PMOD1.
	ON		P00_0 to P00_7, P01_0 to P01_5, P16_1, and P16_7 are used as control signals for Ethernet port 3.
SW7-4	OFF		P01_6, P01_7, P02_0 to P02_7, P03_0, P03_1, P03_4, P03_5, and P15_1 are used as control signals for inverter boards INV1, INV2, INV3, and INV4, BSC1, BSC2, PMOD1, and PMOD2.
	ON		P01_6, P01_7, P02_0 to P02_7, P03_0, P03_1, P03_4, P03_5, and P15_1 are used as control signals for Ethernet port 4.
SW7-5	OFF		P15_7 and P16_2 to P16_5 are used as control signals for inverter boards INV2 and INV4 and PMOD1.
	ON		P15_7 and P16_2 to P16_5 are used as control signals for the QSPI flash memory and SPI expansion connector.
SW7-6	OFF		P17_5 and P18_3 to P18_6 are used as control signals for inverter boards INV1, INV3, and INV4.
	ON		P17_5 and P18_3 to P18_6 are used as control signals for OctaFlash.
SW7-7, SW7-8	-7	-8	
	OFF	OFF	P04_4 to P04_7 and P05_0 to P05_6 are used as control signals for the HSPI, inverter board INV3, and PMOD2.
	OFF	ON	Unused
	ON	OFF	P04_4 to P04_7, P05_0 to P05_6, P09_4, and P09_6 are used as control signals for the NAND flash memory. (When using P09_4 and P09_6 as control signals for BSC1 or inverter boards INV2 and INV4, make a setting other than SW7-7, SW7-8 = ON, OFF.)
	ON	ON	P04_4 to P04_7 and P05_0 to P05_6 are used as control signals for eMMC.

Table 6-4 Signal Function Selection Switch SW9

No.	Setting	Function
SW9-1	Unused	— (At the time of shipment = OFF)
SW9-2	Unused	— (At the time of shipment = OFF)
SW9-3	OFF	P08_5 to P08_7 and P09_3 are used as control signals for inverter board INV4, BSC1, and the SPI expansion connector.
	ON	P08_5 to P08_7 and P09_3 are used as control signals for the NAND flash memory.
SW9-4	Unused	— (At the time of shipment = OFF)
SW9-5	OFF	P00_6, P00_7, and P01_0 are used as ENCIF signals for inverter board INV1 when SW7-3 = OFF.
	ON	P00_6, P00_7, and P01_0 are used as GPT signals for inverter board INV1 when SW7-3 = OFF.
SW9-6	OFF	P02_4 to P02_6 are used as ENCIF signals for inverter board INV2 when SW7-4 = OFF.
	ON	P02_4 to P02_6 are used as GPT signals for inverter board INV2 when SW7-4 = OFF.
SW9-7	OFF	P15_2, and P15_0 and P15_1 when SW7-1, SW7-4 = OFF, OFF are used as ENCIF signals for inverter board INV3.
	ON	P15_2, and P15_0 and P15_1 when SW7-1, SW7-4 = OFF, OFF are used as GPT signals for inverter board INV3.
SW9-8	OFF	P16_6, P16_7 when SW7-3 = OFF, and P17_0 when SW13-1 = ON are used as ENCIF signals for inverter board INV4 when SW12-5 = ON.
	ON	P16_6, P16_7 when SW7-3 = OFF, and P17_0 when SW13-1 = ON are used as GPT signals for inverter board INV4 when SW12-5 = ON.

Table 6-5 Signal Function Selection Switch SW11

No.	Setting			Function
SW11-1, SW11-2	-1	-2		
	ON	OFF		P11_0 is used as VBUSEN for the USB host interface.
	OFF	ON		P11_0 is used as VBUSEN for the USB OTG interface.
SW11-3, SW11-4	-3	-4		
	ON	OFF		P11_7 is used as USB_OTG_ID.
	OFF	ON		P11_7 is used as a control signal for inverter board INV2 or SHOST.
SW11-5 to SW11-7	-5	-6	-7	
	ON	OFF	OFF	P12_4 is used as VBUSIN for the USB function interface.
	OFF	ON	OFF	P12_4 is used as VBUSIN for the USB OTG interface.
	OFF	OFF	ON	P12_4 is used as the user push switch SW4 input.
SW11-8, SW11-9	-8	-9		
	ON	OFF		P14_3 is used as EXICEN for the USB OTG interface.
	OFF	ON		P14_3 is used as D2 for BSC2.
SW11-10	Unused			— (At the time of shipment = OFF)

Table 6-6 Signal Function Selection Switch SW12

No.	Setting	Function
SW12-1	Unused	— (At the time of shipment = OFF)
SW12-2	Unused	— (At the time of shipment = OFF)
SW12-3	OFF	P24_6, P24_7, and P05_7 are used as MDC, MDIO, and NRESET for Ethernet port 0.
	ON	P20_4, P20_5, and P07_0 are used as MDC, MDIO, and NRESET for Ethernet port 0.
SW12-4	OFF	P24_6, P24_7, and P05_7 are used as MDC, MDIO, and NRESET for Ethernet port 2.
	ON	P20_4, P20_5, and P07_0 are used as MDC, MDIO, and NRESET for Ethernet port 2.
SW12-5	OFF	P16_6, P16_7 when SW7-3 = OFF, and P17_0 when SW13-1 = ON are used as control signals for the SPI expansion connector and PMOD1.
	ON	P16_6, P16_7 when SW7-3 = OFF, and P17_0 when SW13-1 = ON are used as control signals for inverter board INV4.
SW12-6	OFF	PCIe is used as an endpoint.
	ON	PCIe is used as a root complex.
SW12-7	OFF	The 12-V power supply of the PCIe connector J6 is OFF.
	ON	The 12-V power supply of the PCIe connector J6 is ON (when used as the root complex).
SW12-8	OFF	The 3.3-V power supply of the PCIe connector J6 is OFF.
	ON	The 3.3-V power supply of the PCIe connector J6 is ON (when used as the root complex).

Table 6-7 Signal Function Selection Switch SW13

No.	Setting			Function
SW13-1, SW13-2	-1	-2		
	ON	OFF		P17_0 is used as a control signal for the SPI expansion connector and inverter board INV4.
	OFF	ON		P17_0 is used as SCL for PMOD1 and the PCIe clock generator (U7).
SW13-3 to SW13-5	-3	-4	-5	
	ON	OFF	OFF	P15_4 is used as SCL for EEPROM.
	OFF	ON	OFF	P15_4 is used as a control signal for BSC2 and PMOD2.
	OFF	OFF	ON	P15_4 is used as USB_OTG_STATUS1.
SW13-6, SW13-7	-6		-7	
	ON		OFF	P17_1 is used as a control signal for the SPI expansion connector and inverter board INV4.
	OFF		ON	P17_1 is used as SDA for PMOD1 and the PCIe clock generator (U7).
SW13-8 to SW13-10	-8	-9	-10	
	ON	OFF	OFF	P15_5 is used as SDA for EEPROM.
	OFF	ON	OFF	P15_5 is used as a control signal for BSC2 and PMOD2.
	OFF	OFF	ON	P15_5 is used as USB_OTG_STATUS2.

Table 6-8 Signal Function Selection Switch SW14

No.	Setting		Function
SW14-1, SW14-2	-1	-2	
	ON	OFF	AN000 is connected to the potentiometer.
	OFF	ON	AN000 is connected to the ADC connector (J56).

6.4 Configuration by Jumper Blocks

This board is equipped with jumper blocks J1, J11 to J20, J22 to J25, J29, J39, J41, and J48 for selecting functions. The functions set by individual jumper blocks are explained below.

6.4.1 I/O Power Selection Jumper Blocks J15, J18, J25, J39, and J41

J15, J18, J25, J39, and J41 are used to select the power supply to the I/O power domain of the RZ/T2N and Ethernet PHY. The supply of voltage to each power supply selected by J15, J18, J25, J39, or J41 must comply with the standards or usage methods of the I/O devices connected to that power domain. Otherwise, malfunctions of the device may occur or permanent damages may be caused.

Table 6-9 I/O Power Selection Jumper Blocks J15, J18, J25, J39, and J41

No.	Setting	Function
J15	1-2 are short-circuit	1.8-V power is supplied to VCC1833_1. This setting is for using the domain signals of VCC1833_1 for Ethernet port 2 (SW7-2 = ON). At this time, set SW10-2 = ON.
	2-3 are short-circuit	3.3-V power is supplied to VCC1833_1. This setting is for using the domain signals of VCC1833_1 for other functions (SW7-2 = OFF). At this time, set SW10-2 = OFF.
J18	1-2 are short-circuit	1.8-V power is supplied to VCC1833_2. This setting is for using the domain signals of VCC1833_2 for Ethernet ports 3 and 4 (SW7-3, SW7-4 = ON, ON) while Ethernet ports 3 and 4 are set to the RGMII mode. At this time, set SW10-3 = ON.
	2-3 are short-circuit	3.3-V power is supplied to VCC1833_2. This setting is for using the domain signals of VCC1833_2 for Ethernet ports 3 and 4 (SW7-3, SW7-4 = ON, ON) while Ethernet ports 3 and 4 are set to the RMII mode or for using the domain signals for other functions (SW7-3, SW7-4 = OFF, OFF). At this time, set SW10-3 = OFF.
J25	1-2 are short-circuit	3.3-V power is supplied to VCC1833_6. This setting is for using the domain signals of VCC1833_6 for other functions (SW7-1 = OFF).
	3-4 are short-circuit	The output from the power-supply control IC for SD1 is supplied to VCC1833_6. This setting is for using the domain signals of VCC1833_6 for the microSD card (SW7-1 = ON).
J39	1-2 are short-circuit	1.8-V power is supplied to VCC1833_5. This setting is for using the domain signals of VCC1833_5 for eMMC (SW7-7, SW7-8 = ON, ON). At this time, set SW10-6 = ON.
	2-3 are short-circuit	3.3-V power is supplied to VCC1833_5. This setting is for using the domain signals of VCC1833_5 for other functions (SW7-7, SW7-8 = OFF, ON or OFF, OFF). At this time, set SW10-6 = OFF.
J41	1-2 are short-circuit	VCC1833_1 is supplied to VDDMDIO of PHY (U54) for Ethernet port 0. This setting is for using P24_6, P24_7, and P05_7 as MDC, MDIO, and NRESET for Ethernet port 0 (SW12-3 = OFF).
	2-3 are short-circuit	1.8-V power is supplied to VDDMDIO of PHY (U54) for Ethernet port 0. This setting is for using P20_4, P20_5, and P07_0 as MDC, MDIO, and NRESET for Ethernet port 0 (SW12-3 = ON).

6.4.2 Debugging Function Selection Jumper Block J29

J29 is used to enable or disable the on-board debugging function J-Link™ OB.

Table 6-10 Debugging Function Selection Jumper Block J29

No.	Setting	Function
J29	Open-circuit	The on-board debugging function J-Link™ OB is enabled.
	Short-circuit	The on-board debugging function J-Link™ OB is disabled. Connect an external emulator to J31 at debugging.

6.4.3 PCIe Reset Signal Control Jumper Block J1

J1 is used to select whether the reset signal of the PCIe is included in the system reset factors.

Table 6-11 PCIe Reset Signal Control Jumper Block J1

No.	Setting	Function
J1	Open-circuit	A PCIe reset is not included in the system reset factors.
	Short-circuit	A PCIe reset is included in the system reset factors.

6.4.4 Current Measurement Jumper Blocks J11 to J14, J16, J17, J19, J20, and J22 to J24

J11 to J14, J16, J17, J19, J20, and J22 to J24 are jumper blocks for measuring the current drawn by the target device (RZ/T2N). When the current is to be measured, insert an ammeter between pins of the corresponding jumper block.

Table 6-12 Current Measurement Jumper Blocks J11 to J14, J16, J17, J19, J20, and J22 to J24

No.	Function	Function
J19	Current of CPU1V1 is measured.	This is a 4-pin jumper block and is not mounted at the time of shipment. When the current is to be measured, remove R75 and insert an ammeter between pins 1-3 side and pins 2-4 side.
J13	Current of CPU1V8 is measured.	
J12	Current of CPU3V3 is measured.	The jumper blocks are short-circuit at the time of shipment. When the current is to be measured, make the relevant jumper block open-circuit and insert an ammeter between pins 1-2.
J16	Current of VDDQ1V1 is measured.	
J11	Current of CPU_VCC1833_0 is measured.	
J14	Current of CPU_VCC1833_1 is measured.	
J17	Current of CPU_VCC1833_2 is measured.	
J20	Current of CPU_VCC1833_3 is measured.	
J22	Current of CPU_VCC1833_4 is measured.	
J23	Current of CPU_VCC1833_5 is measured.	
J24	Current of CPU_VCC1833_6 is measured.	

6.4.5 Inverter Board 24-V Power-Supply GND Connection Jumper Block J48

J48 is used to select connection or disconnection to GND for the 24-V power supply of inverter boards.

Table 6-13 Inverter Board 24-V Power-Supply GND Connection Jumper Block J48

No.	Setting	Function
J48	Open-circuit	The 24-V power supply GND for inverter boards (GND_24V) is not connected to GND. This setting is for supplying 15-V to this board through J7 and for supplying 24-V directly to inverter boards.
	Short-circuit	The 24-V power supply GND for inverter boards (GND_24V) is connected to GND. Connect pins 1-2, 3-4, and 5-6 respectively. This setting is for supplying 24-V to this board through J10 and for supplying 24-V to inverter boards from this board.

6.5 Configuration by Option Links

6.5.1 Settings by Solder Bridges and Trace Cuts

This board is equipped with solder bridges E10 and E11, and trace cuts E1, E2, E5, E8, E9, and E12 for selecting functions. Table 6-14 lists the settings of each solder bridge and trace cut.

Table 6-14 Settings of Solder Bridges and Trace Cuts

No.	Setting	Function
E1	Open-circuit	USB_DM is not connected to USB_OTG_DM.
	Short-circuit	USB_DM is connected to USB_OTG_DM.
E2	Open-circuit	USB_DP is not connected to USB_OTG_DP.
	Short-circuit	USB_DP is connected to USB_OTG_DP.
E5	Open-circuit	Setting prohibited
	Short-circuit	3.3-V power is supplied to the J-Link™ OB circuit.
E8	Open-circuit	PMOD1 (J34) is used in accordance with Type6A (expanded I ² C).
	Short-circuit	PMOD1 (J34) is used in accordance with Type2A (expanded SPI). (In this case, E10 should be left open-circuit.)
E9	Open-circuit	PMOD1 (J34) is used in accordance with Type6A (expanded I ² C).
	Short-circuit	PMOD1 (J34) is used in accordance with Type2A (expanded SPI). (In this case, E11 should be left open-circuit.)
E10	Open-circuit	PMOD1 (J34) is used in accordance with Type2A (expanded SPI).
	Short-circuit	PMOD1 (J34) is used in accordance with Type6A (expanded I ² C). (In this case, E8 should be left open-circuit.)
E11	Open-circuit	PMOD1 (J34) is used in accordance with Type2A (expanded SPI).
	Short-circuit	PMOD1 (J34) is used in accordance with Type6A (expanded I ² C). (In this case, E9 should be left open-circuit.)
E12	Open-circuit	P11_5 is not connected to INV1 (J49). Using P11_5 as BSC_CKIO of the BSC2 connector (J47) instead of as the GPT signal improves the waveform quality.
	Short-circuit	P11_5 is connected to INV1 (J49) (used as the GPT signal).

6.5.2 Settings by 0-Ω Resistors

The following 0-Ω resistors are or can be placed on this board, and the function to be used can be selected by changing the state as shipped to Fit or DNF. Table 6-15 lists the settings of the 0-Ω resistors.

Table 6-15 Settings by 0-Ω Resistors

No.	Setting	Function
R75	Fit	The 1.1-V power supply p1v1 is connected to CPU1V1.
	DNF	The 1.1-V power supply p1v1 is not connected to CPU1V1 (when measuring the CPU1V1 current using J19).
R188	Fit	P05_2 is used as ENCIFDO5 for inverter board INV3 when SW7-7, SW7-8 = OFF, OFF.
	DNF	P05_2 is not used as ENCIFDO5 for inverter board INV3 when SW7-7, SW7-8 = OFF, OFF. Using P05_2 as HSPI_CK of the SHOST connector (J45) improves the waveform quality.
R343, R344	Fit	The terminating resistor for the CAN signal is enabled (connected).
	DNF	The terminating resistor for the CAN signal is disabled (not connected).
R352	Fit	The 130-Ω terminating resistor for RS485 A-B is enabled (connected). To change the value of the terminating resistor, change the value of R353 as desired.
	DNF	The 130-Ω terminating resistor for RS485 A-B is disabled (not connected).
R357	Fit	The DE signal is used in the RE control of the RS485.
	DNF	The DE signal is not used in the RE control of the RS485. In this case, install R358 (10-kΩ) and fix the RE signal to the low level.
R452, R454	Fit	The communications mode of the RS485 interface is full-duplex.
	DNF	The communications mode of the RS485 interface is half-duplex. In this case, set R453 and R455 to the Fit state.
R453, R455	Fit	The communications mode of the RS485 interface is half-duplex.
	DNF	The communications mode of the RS485 interface is full-duplex. In this case, set R452 and R454 to the Fit state.
R262, R338, R414, R431	Fit	RMII is used for the MAC-PHY interface of Ethernet port 3. In this case, also install R418 (10-kΩ) and R456 (10-kΩ).
	DNF	RGMII is used for the MAC-PHY interface of Ethernet port 3.
R396, R423, R429	Fit	RGMII is used for the MAC-PHY interface of Ethernet port 3. In this case, set R418 (10-kΩ) and R456 (10-kΩ) to the DNF state.
	DNF	RMII is used for the MAC-PHY interface of Ethernet port 3.
R325, R331, R464	Fit	RGMII is used for the MAC-PHY interface of Ethernet port 4. In this case, set R318 (10-kΩ) and R320 (10-kΩ) to the DNF state.
	DNF	RMII is used for the MAC-PHY interface of Ethernet port 4.
R333, R436, R463, R465	Fit	RMII is used for the MAC-PHY interface of Ethernet port 4. In this case, also install R318 (10-kΩ) and R320 (10-kΩ).
	DNF	RGMII is used for the MAC-PHY interface of Ethernet port 4.
R482	Fit	P15_6 is used as CKP for the SPI expansion connector.
	DNF	P15_6 is not used as CKP for the SPI expansion connector.
R555	Fit	P09_7 is used as LINKACT2 for an EtherCAT LED.
	DNF	P09_7 is not used as LINKACT2 for an EtherCAT LED.

7. User Circuits

This chapter describes the circuits on the board for each of its functions.

The initial state of this board at the time of shipment is indicated by the **text in bold blue type** in the "Settings of Configuration Circuits" column of each of the signal connection tables. Refer to the details on the configuration circuits in chapter 6.

7.1 Reset Circuit

A reset signal can be generated by the power-on reset IC and reset switch on the board. Figure 7-1 shows the configuration of the reset circuit.

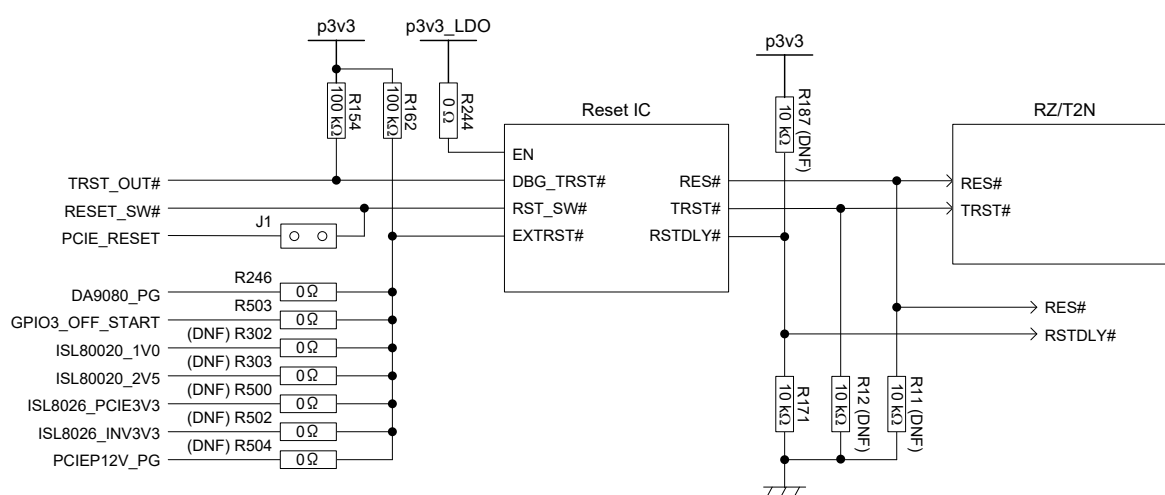


Figure 7-1 Configuration of the Reset Circuit

7.2 Clock Circuit

Figure 7-2 shows the clock circuit for the RZ/T2N on this board. Table 7-1 lists the resonators.

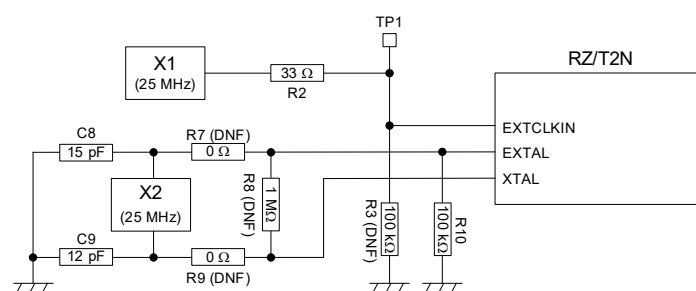


Figure 7-2 Configuration of the Clock Circuit

Table 7-1 List of Resonators

Resonator	Function or Intended Use	State as Shipped	Frequency
X1	Clock for the RZ/T2N (oscillator)	Mounted	25 MHz
X2	Clock for the RZ/T2N	Mounted (disabled state)	25 MHz
X3	Clock for the PCIe	Mounted	25 MHz
X4	Clock for the USB-to-serial conversion IC	Mounted	12 MHz

7.3 Switches

This board is equipped with four push switches and nine DIP switches in addition to the power switch described in section 2.2. Table 7-2 lists the functions and signal connections of the four push switches. Table 7-3 lists the functions and signal connections of user DIP switch SW6.

Among the DIP switches, SW8 and SW10 are used for setting the mode of the RZ/T2N, and SW7, SW9, and SW11 to SW14 are used for selecting the functions of the signal lines. Refer to section 6.3 in which the switches are explained as part of the configuration circuitry of this board.

Table 7-2 Signal Connections of the Push Switches

Switch	Function or Intended Use	MPU Port	Settings of Configuration Circuits
SW2	User switch (Usr_SW0), connected to IRQ10.	P10_4	—
SW3	User switch (Usr_SW1), connected to IRQ8.	P08_1	—
SW4	User switch (Usr_SW2), connected to IRQ12.	P12_4* ¹	SW11-5: OFF, SW11-6: OFF, SW11-7: ON
SW5 (RES)	Reset switch	RES#* ²	—

Notes: 1. Connected via DIP switches. If the factory settings are used, this can be used as an SW4 input.

2. Connected via the reset circuit.

Table 7-3 Signal Connections of User DIP Switch SW6

Switch	Function or Intended Use	MPU Port	Settings of Configuration Circuits
SW6-1	Connected to P07_2 for user control.	P07_2	—
SW6-2	Connected to P07_3 for user control.	P07_3	—
SW6-3	Connected to P07_4 for user control.	P07_4	—
SW6-4	Connected to P07_5 for user control.	P07_5	—

7.4 LEDs

This board is equipped with 22 LEDs. Table 7-4 lists the functions, colors, and signal connections of the LEDs.

Table 7-4 Signal Connections of the LEDs

LED	Color	Function or Intended Use	MPU Port	Settings of Configuration Circuits
LED1 (P15V)	Yellow	Indicator of the 15-V power-supply line	—	—
LED2 (P3V3)	Green	Indicator of the 3.3-V power-supply line	—	—
LED3_ESC_RUN	Green	ESC_LED RUN (User LED)	P10_1	—
LED4_ESC_ERR	Red	ESC_LED ERR (User LED)	P06_3	—
LED5_ESC_L/A0	Green	ESC_LINKACT0 (User LED)	P08_3	—
LED6_ESC_L/A1	Green	ESC_LINKACT1 (User LED)	P08_4	—
LED7_ESC_L/A2	Green	ESC_LINKACT2 (User LED)	P09_7	R555: Fit
LED8	Green	User LED0	P13_3	—
LED9	Green	User LED1	P13_5	—
LED10	Yellow	User LED2	P10_2	—
LED11	Red	User LED3	P10_3	—
LED12	Yellow	Indicator of J-Link™ OB	—	—
LED built in J8A	Green	Ethernet port 0 LED (Link)	—	—
LED built in J8A	Yellow	Ethernet port 0 LED (Activity)	—	—
LED built in J8B	Green	Ethernet port 1 LED (Link)	—	—
LED built in J8B	Yellow	Ethernet port 1 LED (Activity)	—	—
LED built in J30	Green	Ethernet port 2 LED (Link)	—	—
LED built in J30	Yellow	Ethernet port 2 LED (Activity)	—	—
LED built in J36A	Green	Ethernet port 3 LED (Link)	—	—
LED built in J36A	Yellow	Ethernet port 3 LED (Activity)	—	—
LED built in J36B	Green	Ethernet port 4 LED (Link)	—	—
LED built in J36B	Yellow	Ethernet port 4 LED (Activity)	—	—

7.5 Potentiometer

On this board, a 10-k Ω single-rotation potentiometer for evaluating the A/D converter is connected to AN000 of the RZ/T2N. Figure 7-3 shows the configuration of the potentiometer circuit.

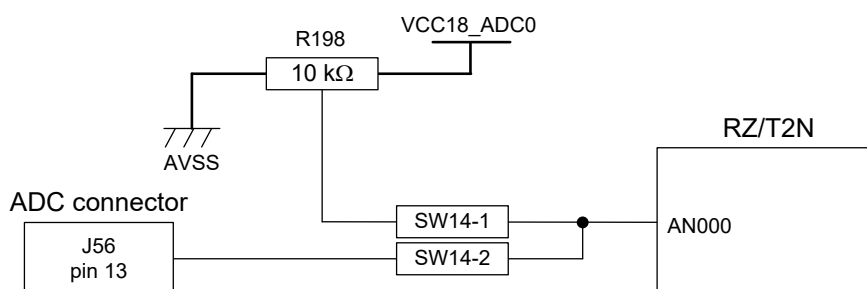


Figure 7-3 Configuration of the Potentiometer Circuit

A potentiometer is installed to provide an easy way of supplying a variable analog input to the microprocessor. Note in advance that it will not guarantee the accuracy of the A/D converter.

7.6 Pmod™

This board is equipped with two connectors for Digilent Pmod™ interfaces so that compatible Pmod™ modules can be connected and evaluated. PMOD1 (J34) supports the Type2A, 6A Pmod™ interfaces and PMOD2 (J35) supports Type3A. Figure 7-4 shows the configuration of the Pmod™ interface circuits. Table 7-5 and Table 7-6 list the signal connections. Figure 7-5 shows the switch settings when using PMOD1 and PMOD2.

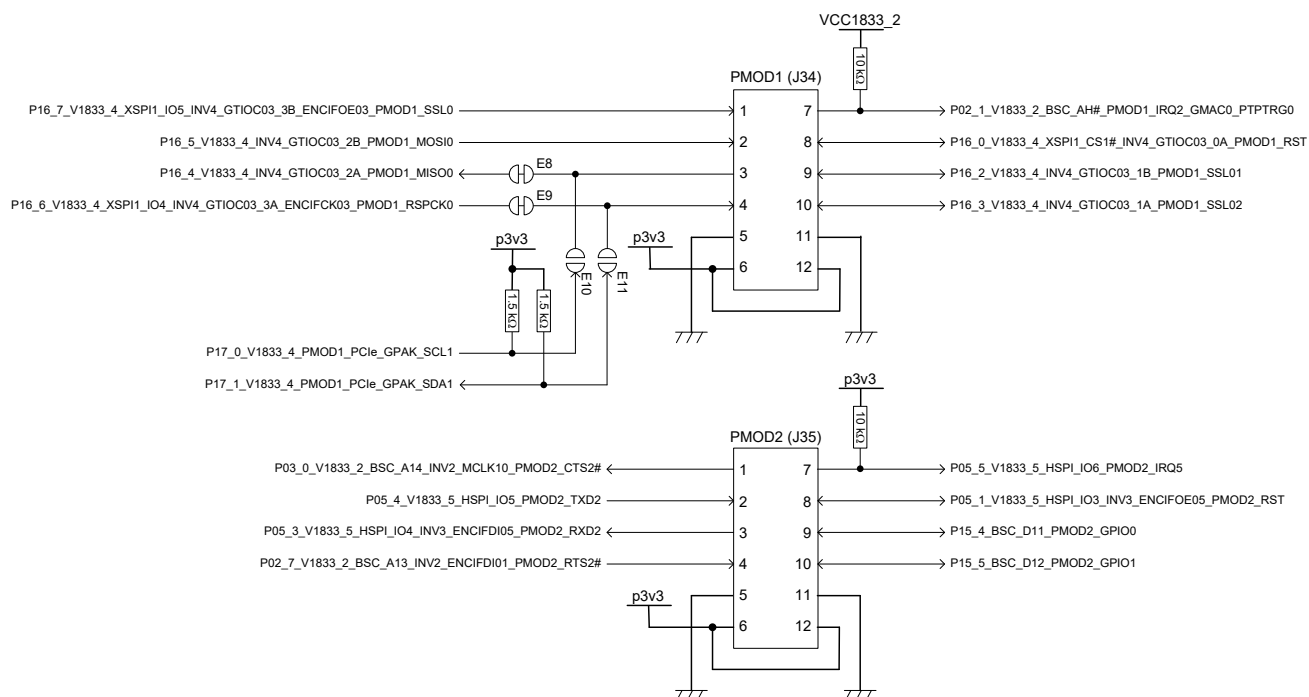


Figure 7-4 Configuration of the Pmod™ Interface Circuits

Table 7-5 Signal Connections of the PMOD1 Connector (J34)

Pin	Signal Name	MPU Port	Settings of Configuration Circuits
1	P16_7_V1833_4_XSPI1_IO5_INV4_GTIOC03_3B_ENCIFOE03_PMOD1_SSL0	P16_7*1	SW7-3 : OFF, SW12-5 : OFF
2	P16_5_V1833_4_INV4_GTIOC03_2B_PMOD1_MOSI0	P16_5*1	SW7-5: OFF
3	P16_4_V1833_4_INV4_GTIOC03_2A_PMOD1_MISO0	P16_4*1	SW7-5: OFF, E8 : Short-circuit, E10 : Open-circuit
	P17_0_V1833_4_PMOD1_PCl_e_GPAK_SCL1	P17_0*2*3	SW12-5 : OFF, SW13-1 : OFF, SW13-2: ON, E8 : Open-circuit, E10: Short-circuit
4	P16_6_V1833_4_XSPI1_IO4_INV4_GTIOC03_3A_ENCIFCK03_PMOD1_RSPCK0	P16_6	SW12-5 : OFF, E9 : Short-circuit, E11 : Open-circuit
	P17_1_V1833_4_PMOD1_PCl_e_GPAK_SDA1	P17_1*2*3	SW13-6: OFF, SW13-7: ON, E9: Open-circuit, E11: Short-circuit
5	GND	—	—
6	p3v3	—	—
7	P02_1_V1833_2_BSC_AH#_PMOD1_IRQ2_GMAC0_PTPTRG0	P02_1*1	SW7-4: OFF
8	P16_0_V1833_4_XSPI1_CS1#_INV4_GTIOC03_0A_PMOD1_RST	P16_0	—
9	P16_2_V1833_4_INV4_GTIOC03_1B_PMOD1_SSL01	P16_2*1	SW7-5: OFF
10	P16_3_V1833_4_INV4_GTIOC03_1A_PMOD1_SSL02	P16_3*1	SW7-5: OFF
11	GND	—	—
12	p3v3	—	—

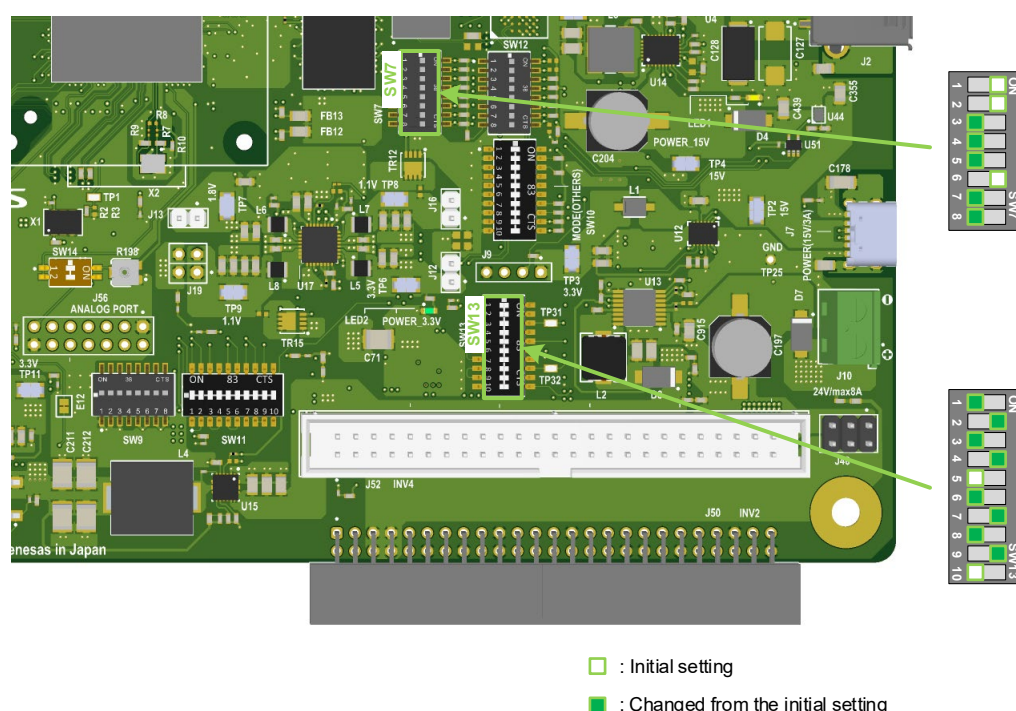
Notes: 1. Connected via the bus switch IC. To use PMOD1, pins 2 and 3 of J18 should be short-circuit and SW10-3 should be turned off.
2. To change the function, the setting of an option link has to be changed.
3. Connected via SW13.

Table 7-6 Signal Connections of the PMOD2 Connector (J35)

Pin	Signal Name	MPU Port	Settings of Configuration Circuits
1	P03_0_V1833_2_BSC_A14_INV2_MCLK10_PMOD2_CTS2#	P03_0*1	SW7-4 : OFF
2	P05_4_V1833_5_HSPI_IO5_PMOD2_TXD2	P05_4*1	SW7-7: OFF, SW7-8: OFF
3	P05_3_V1833_5_HSPI_IO4_INV3_ENCIFDI05_PMOD2_RXD2	P05_3*1	SW7-7: OFF, SW7-8: OFF
4	P02_7_V1833_2_BSC_A13_INV2_ENCIFDI01_PMOD2_RTS2#	P02_7*1	SW7-4: OFF
5	GND	—	—
6	p3v3	—	—
7	P05_5_V1833_5_HSPI_IO6_PMOD2_IRQ5	P05_5*1	SW7-7: OFF, SW7-8: OFF
8	P05_1_V1833_5_HSPI_IO3_INV3_ENCIFOE05_PMOD2_RST	P05_1*1	SW7-7: OFF, SW7-8: OFF
9	P15_4_BSC_D11_PMOD2_GPIO0	P15_4*2	SW13-3 : OFF, SW13-4: ON, SW13-5 : OFF
10	P15_5_BSC_D12_PMOD2_GPIO1	P15_5*2	SW13-8: OFF, SW13-9: ON, SW13-10 : OFF
11	GND	—	—
12	p3v3	—	—

Notes: 1. Connected via the bus switch IC. To use PMOD2, pins 2 and 3 of J18 and J39 should be short-circuit and SW10-3 and SW10-6 should be turned off.

2. Connected via SW13.

**Figure 7-5 Switch Settings When Using PMOD1 and PMOD2**

Note that the pin assignment for a Digilent Pmod™ connector differs in terms of numbering from that for a typical connector. Figure 7-6 shows the pin assignment for a Pmod™ connector. For details, refer to the Digilent Pmod™ Interface Specification.

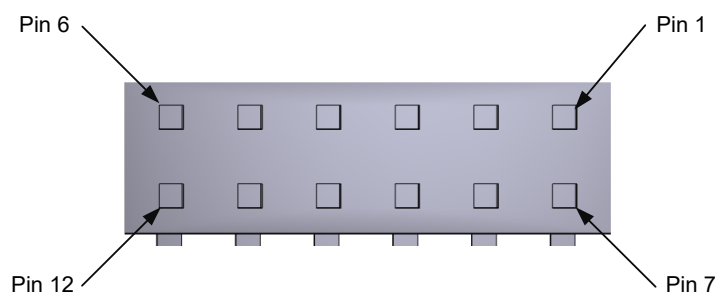


Figure 7-6 Pin Assignment for a Digilent Pmod™ Connector (Viewed from the Direction of Insertion)

7.7 USB-to-Serial Conversion

This board is equipped with a USB connector (J33) for terminal output and an FT2232 for USB-to-serial conversion. Figure 7-7 shows the configuration of the USB-to-serial conversion circuit. Table 7-7 lists the signal connections.

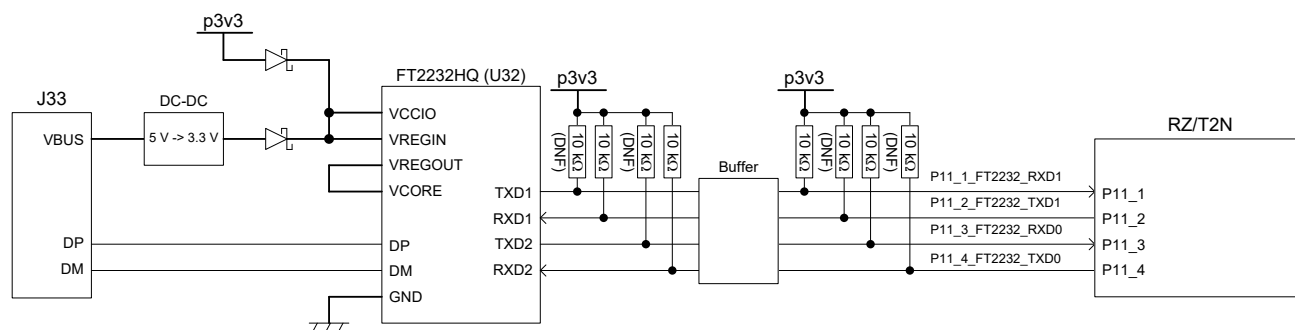


Figure 7-7 Configuration of the USB-to-Serial Conversion Circuit

Table 7-7 Signal Connections of USB-to-Serial Conversion

Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P11_1_FT2232_RXD1	UART data reception 1 for USB-to-serial conversion	P11_1	—
P11_2_FT2232_TXD1	UART data transmission 1 for USB-to-serial conversion	P11_2	—
P11_3_FT2232_RXD0	UART data reception 0 for USB-to-serial conversion	P11_3	—
P11_4_FT2232_TXD0	UART data transmission 0 for USB-to-serial conversion	P11_4	—

When the USB connector (J33) for terminal output is first connected to a PC, the PC will search for a driver. A driver with the standard specification that has been installed on the PC should be used.

7.8 SPI Memory

This board has OctaFlash, Quad SPI flash memory, and EEPROM as SPI memory. An SPI expansion connector (J26) is also connected to SPI1.

Figure 7-8 shows the configuration of the SPI memory circuits, and Table 7-8 lists the SPI memories. Table 7-9 to Table 7-11 list the signal connections for each memory. Table 7-12 lists the signal connections for the SPI expansion connector. Figure 7-9 shows the switch settings when using the SPI expansion connector.

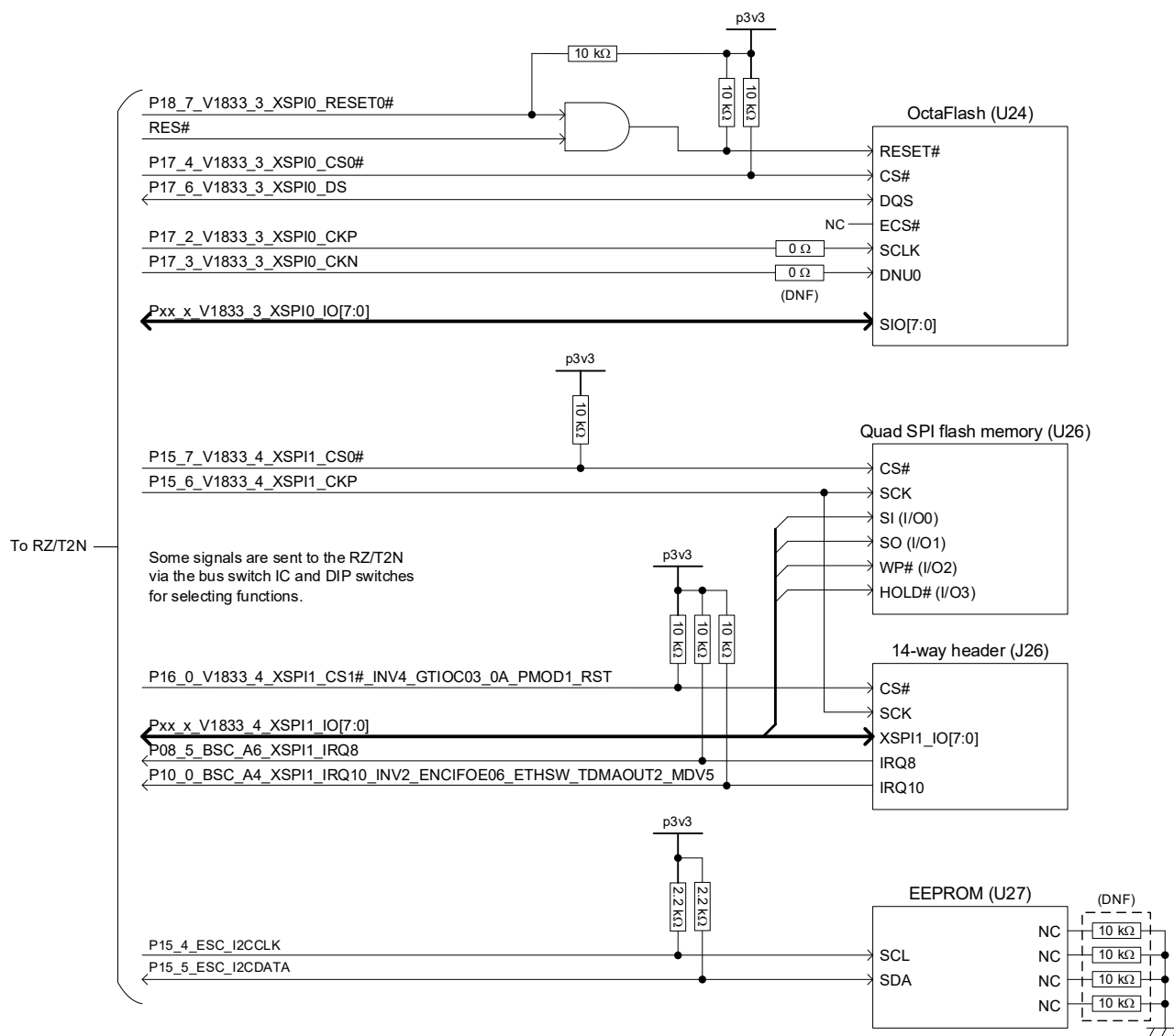


Figure 7-8 Configuration of the SPI Memory Circuits

Table 7-8 List of SPI Memories

SPI Memory	Reference	Controller	Address Space
OctaFlash (512 Mbits)	U24	XSPI0_CS0	40000000h to 43FFFFFFh (64 Mbytes)
Quad SPI flash memory (128 Mbits)	U26	XSPI1_CS0	50000000h to 50FFFFFFh (16 Mbytes)
EEPROM (32 Kbits)	U27	I ² C or EtherCAT	—

Table 7-9 Signal Connections of the OctaFlash

Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P18_7_V1833_3_XSPI0_RESET0#	Reset for XSPI0	P18_7* ¹	—
P17_4_V1833_3_XSPI0_CS0#	CS0#	P17_4	—
P17_6_V1833_3_XSPI0_DS	DS	P17_6	—
P17_2_V1833_3_XSPI0_CKP	CKP	P17_2	—
P18_6_V1833_3_XSPI0_IO7	Data 7	P18_6* ²	SW7-6: ON
P18_5_V1833_3_XSPI0_IO6	Data 6	P18_5* ²	
P18_4_V1833_3_XSPI0_IO5	Data 5	P18_4* ²	
P18_3_V1833_3_XSPI0_IO4	Data 4	P18_3* ²	
P18_2_V1833_3_XSPI0_IO3	Data 3	P18_2	—
P18_1_V1833_3_XSPI0_IO2	Data 2	P18_1	—
P18_0_V1833_3_XSPI0_IO1	Data 1	P18_0	—
P17_7_V1833_3_XSPI0_IO0	Data 0	P17_7	—

Notes: 1. Connected via negative-logic OR with the RES# signal.

2. Connected via the bus switch IC.

Table 7-10 Signal Connections of the Quad SPI Flash Memory

Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P15_7_V1833_4_XSPI1_CS0#	CS0#	P15_7*	SW7-5: ON
P15_6_V1833_4_XSPI1_CKP	CKP	P15_6	—
P16_5_V1833_4_XSPI1_IO3	Data 3	P16_5*	SW7-5: ON
P16_4_V1833_4_XSPI1_IO2	Data 2	P16_4*	
P16_3_V1833_4_XSPI1_IO1	Data 1	P16_3*	
P16_2_V1833_4_XSPI1_IO0	Data 0	P16_2*	

Note: Connected via the bus switch IC.

Table 7-11 Signal Connections of the EEPROM

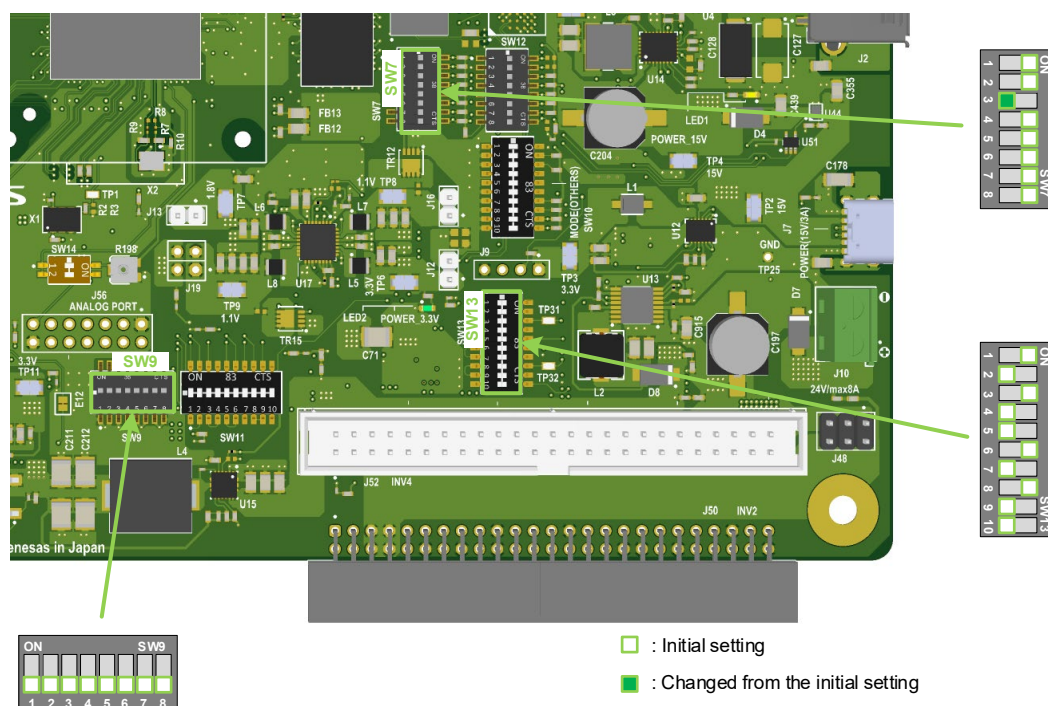
Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P15_4_ESC_I2CCLK	ESC_I2CCLK	P15_4*	SW13-3: ON, SW13-4: OFF, SW13-5: OFF
P15_5_ESC_I2CDATA	ESC_I2CDATA	P15_5*	SW13-8: ON, SW13-9: OFF, SW13-10: OFF

Note: Connected via SW13.

Table 7-12 Signal Connections of the SPI Expansion Connector (J26)

Pin	Signal Name	MPU Port	Settings of Configuration Circuits
1	GND	—	—
2	P08_5_BSC_A6_XSPI1_IRQ8	P08_5*1	SW9-3: OFF
3	P15_6_V1833_4_XSPI1_CKP	P15_6	R482: Fit
4	P16_0_V1833_4_XSPI1_CS1#_INV4_GTIOC03_0A_PMOD1_RST	P16_0	—
5	P17_1_V1833_4_XSPI1_IO7_INV4_ENCIFDI03	P17_1*2	SW13-6: ON, SW13-7: OFF
6	P17_0_V1833_4_XSPI1_IO6_INV4_GTIOC03_4A_ENCIFDO03	P17_0*2	SW12-5: OFF, SW13-1: ON, SW13-2: OFF
7	P16_7_V1833_4_XSPI1_IO5_INV4_GTIOC03_3B_ENCIFOE03_PMOD1_SSL0	P16_7*1	SW7-3: OFF, SW12-5: OFF
8	P16_6_V1833_4_XSPI1_IO4_INV4_GTIOC03_3A_ENCIFCK03_PMOD1_RSPCK0	P16_6	SW12-5: OFF
9	P16_5_V1833_4_XSPI1_IO3	P16_5*1	SW7-5: ON
10	P16_4_V1833_4_XSPI1_IO2	P16_4*1	
11	P16_3_V1833_4_XSPI1_IO1	P16_3*1	
12	P16_2_V1833_4_XSPI1_IO0	P16_2*1	
13	P10_0_BSC_A4_XSPI1_IRQ10_INV2_ENCIFOE06_ETHSW_TDMAOUT2_MDV5	P10_0	—
14	p3v3	—	—

Notes: 1. Connected via the bus switch IC.
2. Connected via SW13.

**Figure 7-9 Switch Settings When Using the SPI Expansion Connector**

7.9 LPDDR4

This board is equipped with LPDDR4. Figure 7-10 shows the configuration of the LPDDR4 circuit.

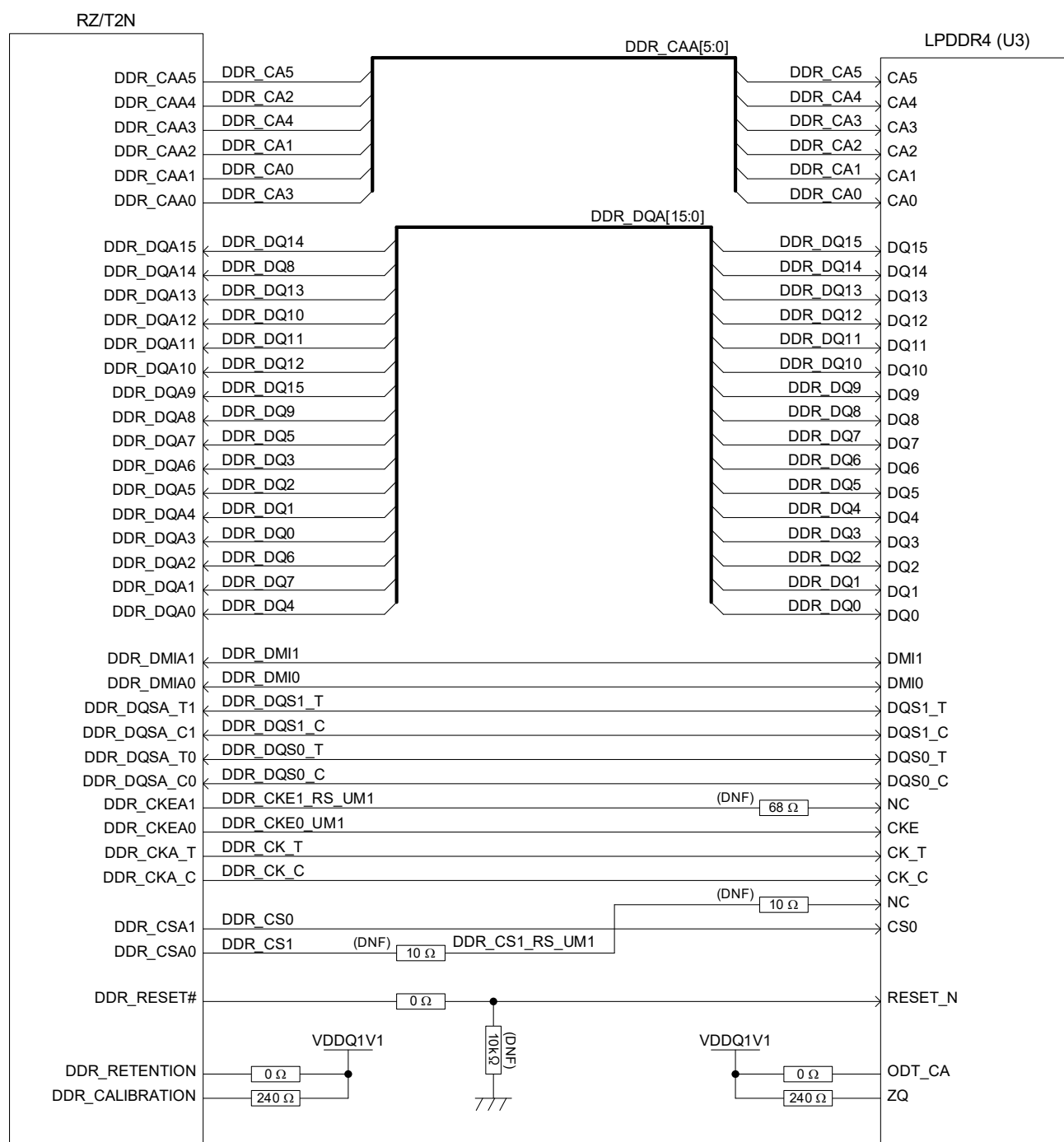


Figure 7-10 Configuration of the LPDDR4 Circuit

7.10 microSD, eMMC, and NAND Flash Memory

This board is equipped with a microSD card slot (J27), eMMC (U28), and NAND flash memory (U29). Figure 7-11 shows the configuration of the microSD, eMMC, and NAND flash memory circuits. Table 7-13 to Table 7-15 list the signal connections. Figure 7-12 shows the switch settings when using the NAND flash memory.

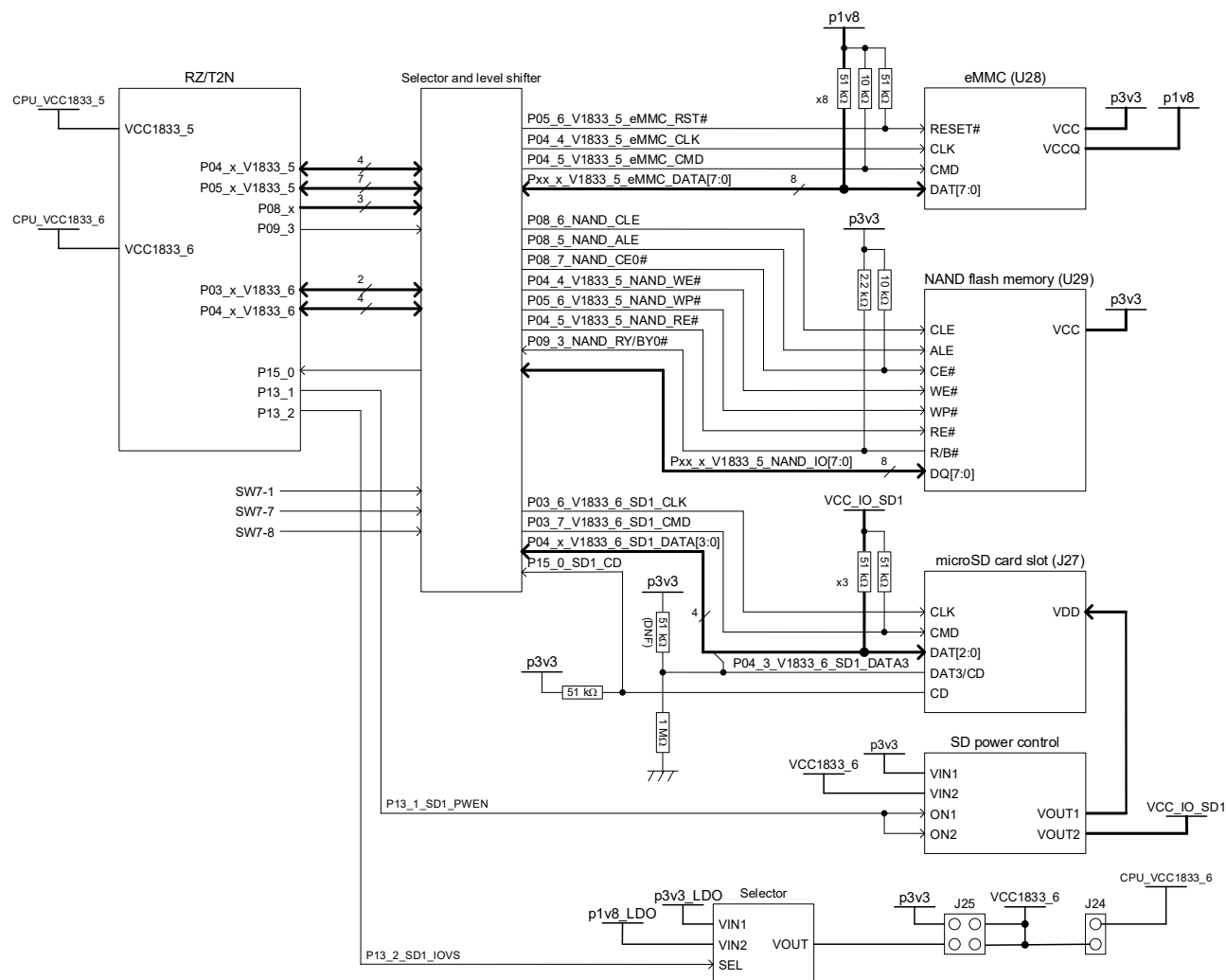


Figure 7-11 Configuration of the microSD, eMMC, and NAND Flash Memory Circuits

Table 7-13 Signal Connections of the eMMC

Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P05_6_V1833_5_eMMC_RST#	Reset	P05_6*	SW7-7: ON, SW7-8: ON
P04_5_V1833_5_eMMC_CMD	Command	P04_5*	
P04_4_V1833_5_eMMC_CLK	Clock	P04_4*	
P04_6_V1833_5_eMMC_DATA0	Data 0	P04_6*	
P04_7_V1833_5_eMMC_DATA1	Data 1	P04_7*	
P05_0_V1833_5_eMMC_DATA2	Data 2	P05_0*	
P05_1_V1833_5_eMMC_DATA3	Data 3	P05_1*	
P05_2_V1833_5_eMMC_DATA4	Data 4	P05_2*	
P05_3_V1833_5_eMMC_DATA5	Data 5	P05_3*	
P05_4_V1833_5_eMMC_DATA6	Data 6	P05_4*	
P05_5_V1833_5_eMMC_DATA7	Data 7	P05_5*	

Note: Connected via the bus switch IC. To use the eMMC, pins 1 and 2 of J39 should be short-circuit and SW10-6 should be turned on.

Table 7-14 Signal Connections of the NAND Flash Memory

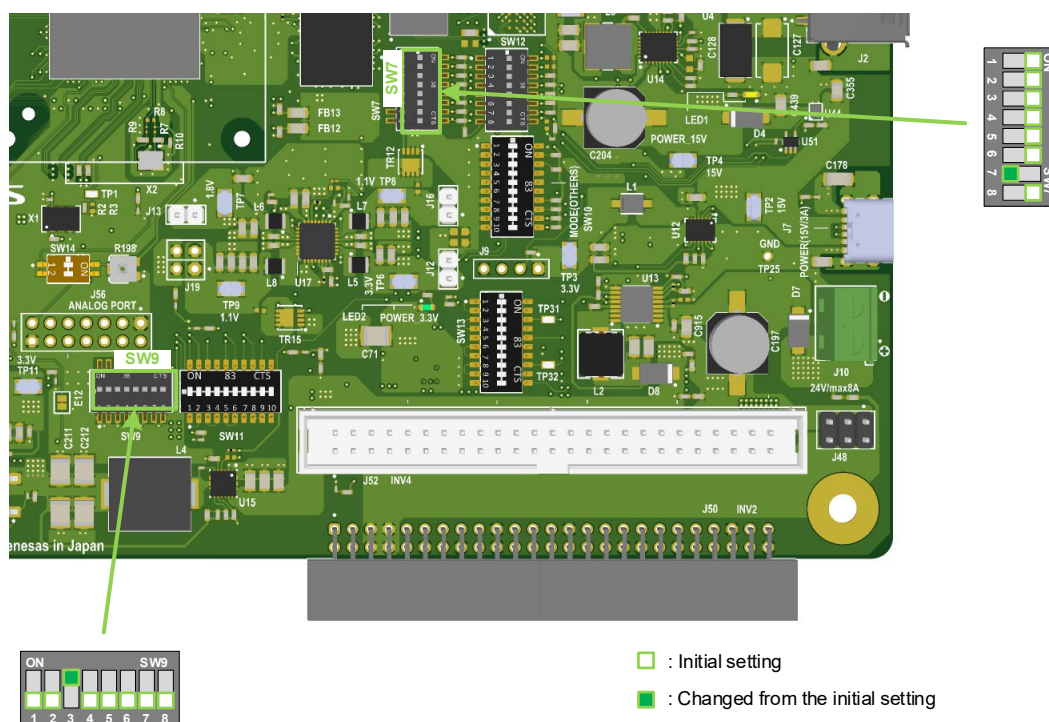
Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P08_5_NAND_ALE	Address latch enable	P08_5*	SW9-3: ON
P08_6_NAND_CLE	Command latch enable	P08_6*	
P08_7_NAND_CE0#	Chip enable	P08_7*	
P09_3_NAND_RY/BY0#	Ready/busy	P09_3*	
P04_4_V1833_5_NAND_WE#	Write enable	P04_4*	SW7-7: OFF, SW7-8: ON
P04_5_V1833_5_NAND_RE#	Read enable	P04_5*	
P05_6_V1833_5_NAND_WP#	Write protect	P05_6*	
P04_6_V1833_5_NAND_IO0	Data 0	P04_6*	
P04_7_V1833_5_NAND_IO1	Data 1	P04_7*	
P05_0_V1833_5_NAND_IO2	Data 2	P05_0*	
P05_1_V1833_5_NAND_IO3	Data 3	P05_1*	
P05_2_V1833_5_NAND_IO4	Data 4	P05_2*	
P05_3_V1833_5_NAND_IO5	Data 5	P05_3*	
P05_4_V1833_5_NAND_IO6	Data 6	P05_4*	
P05_5_V1833_5_NAND_IO7	Data 7	P05_5*	

Note: Connected via the bus switch IC. To use the NAND flash memory, pins 2 and 3 of J39 should be short-circuit and SW10-6 should be turned off.

Table 7-15 Signal Connections of the MicroSD Card Slot

Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P03_6_V1833_6_SD1_CLK	Clock	P03_6*	SW7-1: ON
P03_7_V1833_6_SD1_CMD	Command	P03_7*	
P04_0_V1833_6_SD1_DATA0	Data 0	P04_0*	
P04_1_V1833_6_SD1_DATA1	Data 1	P04_1*	
P04_2_V1833_6_SD1_DATA2	Data 2	P04_2*	
P04_3_V1833_6_SD1_DATA3	Data 3	P04_3*	
P15_0_SD1_CD	Card detection	P15_0*	—
P13_1_SD1_PWEN	Power supply control	P13_1	
P13_2_SD1_IOVS	IO voltage selection of SD1	P13_2	

Note: Connected via the bus switch IC. To use the microSD card slot, pins 3 and 4 of J25 should be short-circuit.

**Figure 7-12 Switch Settings When Using the NAND Flash Memory**

7.11 CAN

This board is equipped with a CAN transceiver (U45) and a CAN interface connector (J37) so that the CAN module of the RZ/T2N can be evaluated. Figure 7-13 shows the configuration of the CAN interface circuit, and Table 7-16 lists the signal connections.

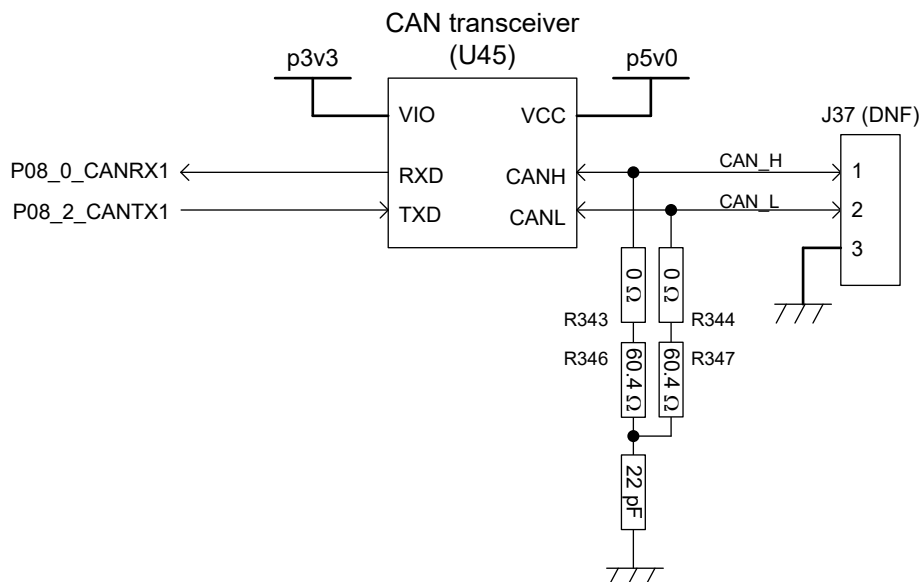


Figure 7-13 Configuration of the CAN Interface Circuit

Table 7-16 Signal Connections of the CAN

Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P08_0_CANRX1	Reception of CAN data	P08_0	—
P08_2_CANTX1	Transmission of CAN data	P08_2	—

7.12 RS485 Interface

This board is equipped with an RS485 transceiver (U49) and an RS485 interface connector (J38). Figure 7-14 shows the configuration of the RS485 interface circuit, Table 7-17 lists the signal connections of the connector, and Table 7-18 lists the ports to be used.

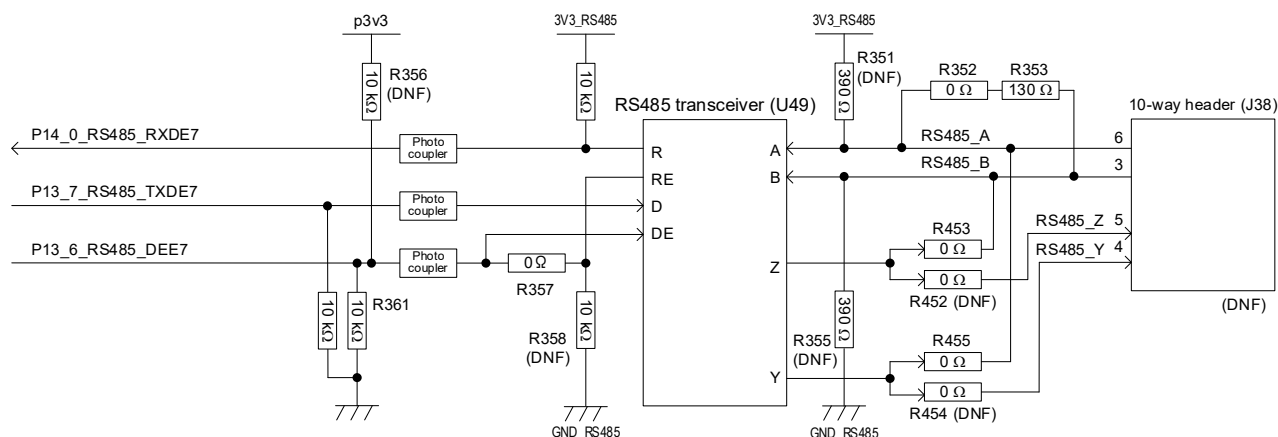


Figure 7-14 Configuration of the RS485 Interface Circuit

Table 7-17 Signal Connections of the RS485 Interface Connector (J38)

Pin	Signal Name	Pin	Signal Name
1	GND_RS485	2	GND_RS485
3	RS485_B	4	RS485_Y
5	RS485_Z	6	RS485_A
7	GND_RS485	8	GND_RS485
9	GND_RS485	10	GND_RS485

Table 7-18 Ports Used with the RS485 Interface

Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P14_0_RS485_RXDE7	Reception of data	P14_0	—
P13_6_RS485_DEE7	Driver enable signal	P13_6	—
P13_7_RS485_TXDE7	Transmission of data	P13_7	—

7.13 USB

This board is equipped with a USB Type-A connector (J2), a USB Micro-B connector (J3), and a USB Micro-AB connector (J4). The USB function of the RZ/T2N can be used as a USB host interface, a USB function interface, or an OTG interface (they cannot be used at the same time).

Figure 7-15 shows the configuration of the USB circuit, Table 7-19 lists the signal connections, and Figure 7-16 shows the switch settings when using the USB.

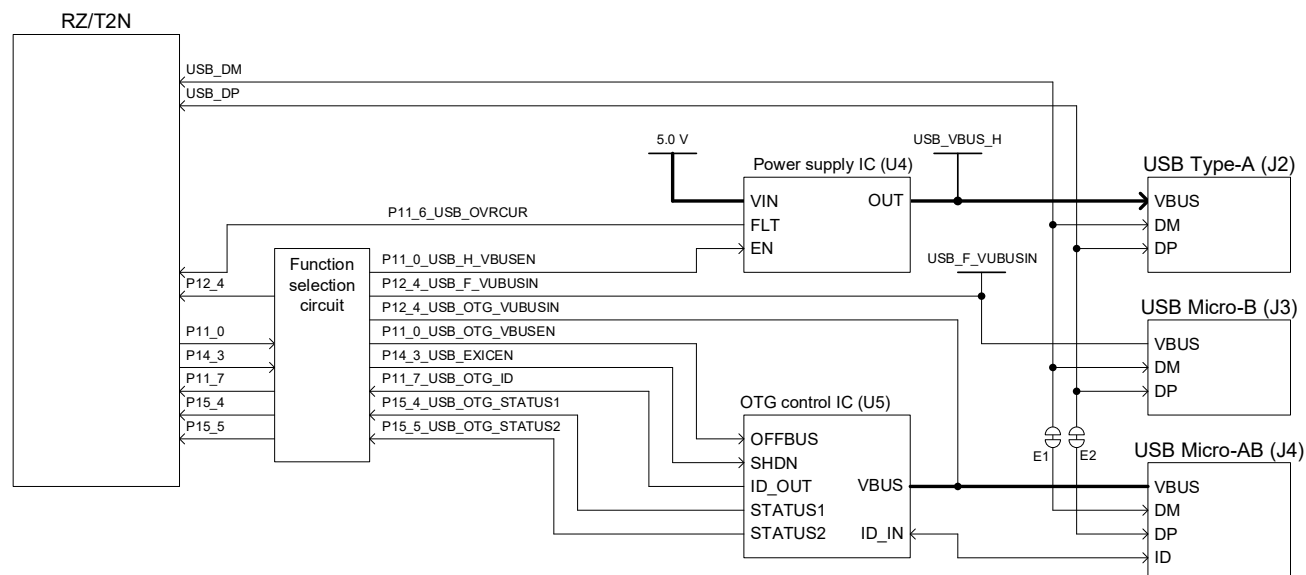


Figure 7-15 Configuration of the USB Circuit

Table 7-19 Signal Connections of the USB

Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
USB_DP	Input/output of D+ data (host or function)	USB_DP	—
	Input/output of D+ data (OTG)		E2: Short-circuit
USB_DM	Input/output of D- data (host or function)	USB_DM	—
	Input/output of D- data (OTG)		E1: Short-circuit
P12_4_USB_F_VUBUSIN	VBUS detection (function)	P12_4*1	SW11-5: ON, SW11-6: OFF, SW11-7: OFF
P12_4_USB_OTG_VUBUSIN	VBUS detection (OTG)		SW11-5: OFF, SW11-6: ON, SW11-7: OFF
P11_0_USB_H_VBUSEN	VBUS enable signal (host)	P11_0*1	SW11-1: ON, SW11-2: OFF
P11_0_USB_OTG_VBUSEN	VBUS enable signal (OTG)		SW11-1: OFF, SW11-2: ON
P11_6_USB_OVRCUR	Overcurrent (host)	P11_6	—
P11_7_USB_OTG_ID	OTG_ID input	P11_7*1	SW11-3: ON, SW11-4: OFF
P14_3_USB_EXICEN	OTG power supply IC control	P14_3*1	SW11-8: ON, SW11-9: OFF
P15_4_USB_OTG_STATUS1	External power supply IC status input 1 (OTG)	P15_4*2	SW13-3: OFF, SW13-4: OFF, SW13-5: ON
P15_5_USB_OTG_STATUS2	External power supply IC status input 2 (OTG)		SW13-8: OFF, SW13-9: OFF, SW13-10: ON

Notes: 1. Connected via SW11.

2. Connected via SW13.

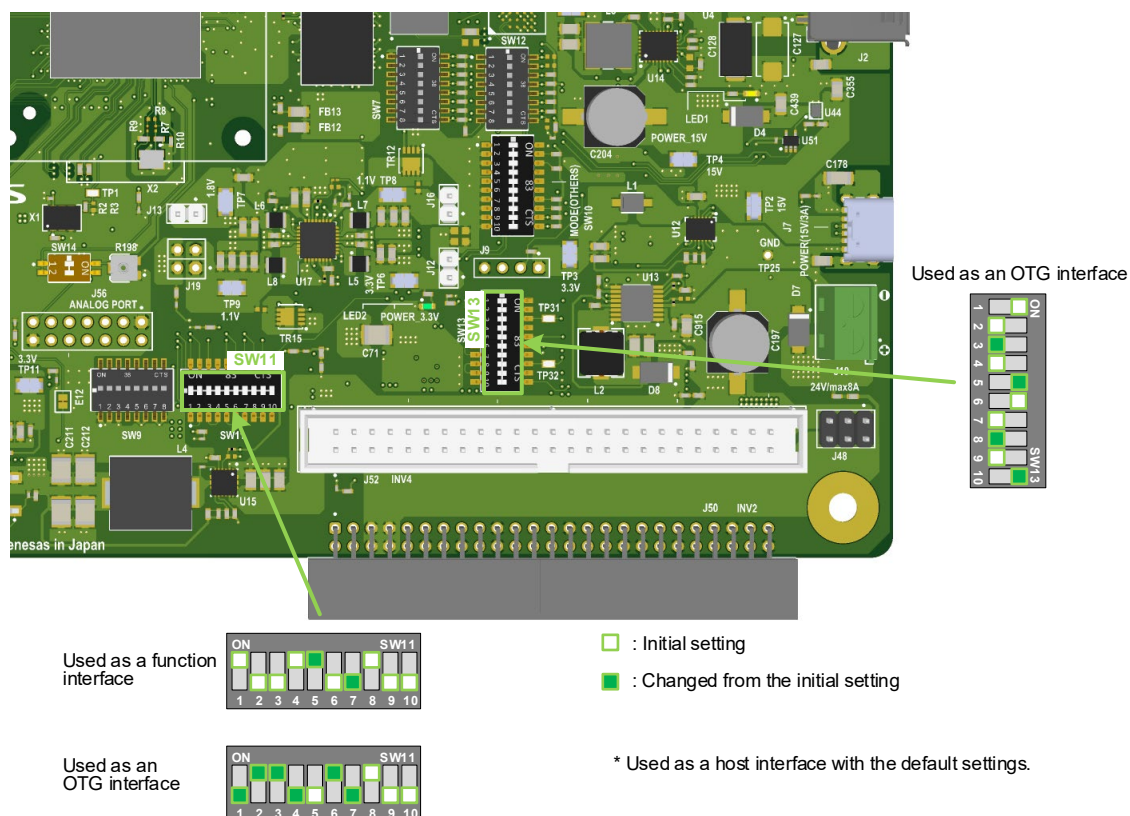


Figure 7-16 Switch Settings When Using the USB

7.14 Ethernet System

When running any Ethernet software, do so with the use of a unique MAC address. A sticker indicating the unique MAC address that was assigned by Renesas is affixed to this board (top side) to ensure full compatibility in the case of connection to other Renesas hardware modules.

An EtherCAT ID number is required to execute the EtherCAT slave controller software. Please use SW6 as required.

This board is equipped with five Ethernet PHY devices and Ethernet connectors (J8 (two ports), J30 (one port), and J36 (two ports)) so that the Ethernet system of the RZ/T2N can be evaluated. Figure 7-17 shows the configuration of the Ethernet system circuit. Table 7-20 to Table 7-24 list the signal connections. Table 7-25 shows initial settings by hardware strapping of the PHY devices.

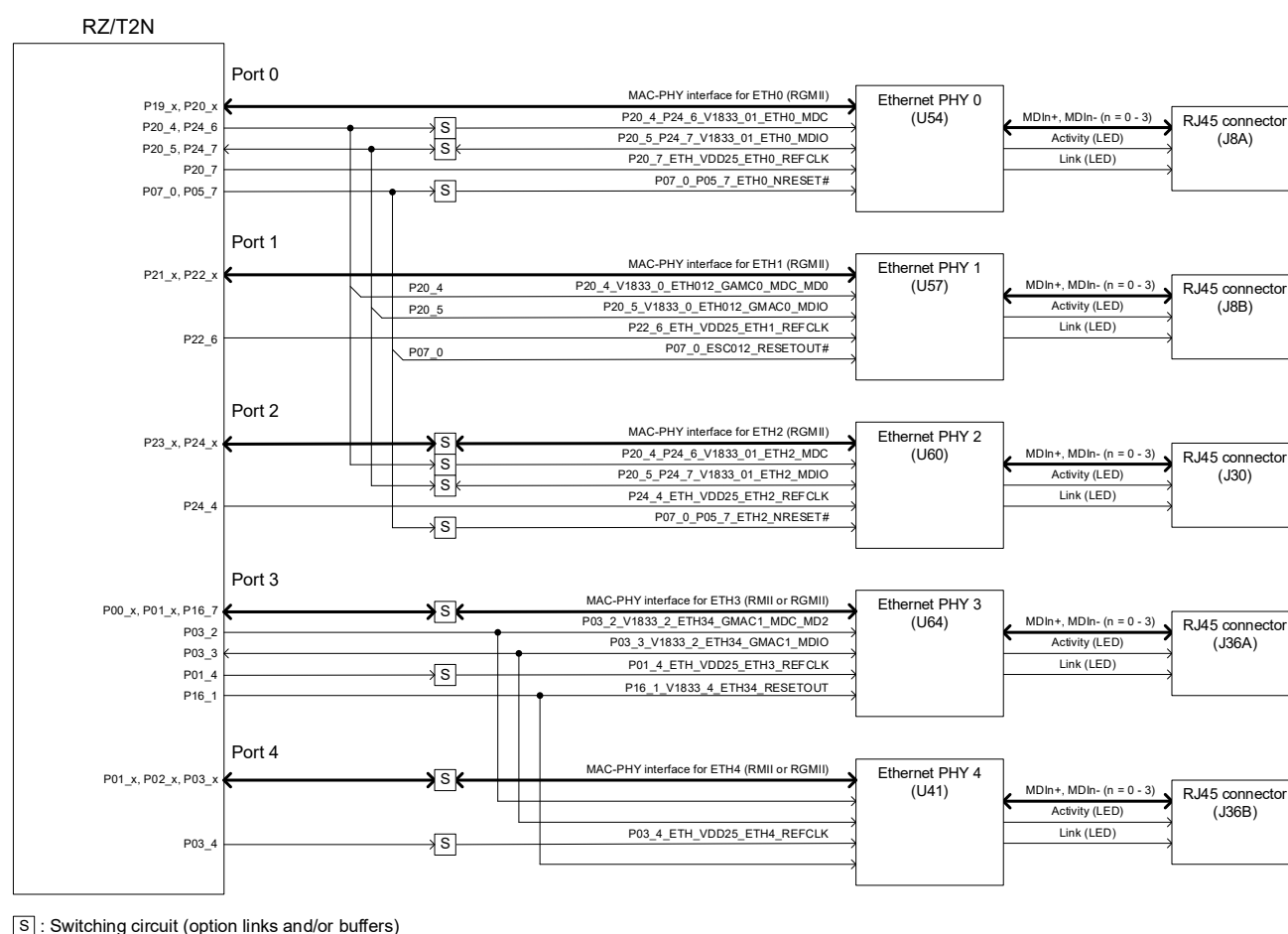


Figure 7-17 Configuration of the Ethernet System Circuit

Table 7-20 Signal Connections of Ethernet Port 0 (ETH0)

Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P19_0_V1833_0_ETH0_TXCLK	Transmit clock	P19_0	—
P19_1_V1833_0_ETH0_TXD0	Transmit data 0	P19_1	—
P19_2_V1833_0_ETH0_TXD1	Transmit data 1	P19_2	—
P19_3_V1833_0_ETH0_TXD2	Transmit data 2	P19_3	—
P19_4_V1833_0_ETH0_TXD3	Transmit data 3	P19_4	—
P19_5_V1833_0_ETH0_TXEN	Transmit data enable or error	P19_5	—
P19_6_V1833_0_ETH0_RXCLK	Receive clock	P19_6	—
P19_7_V1833_0_ETH0_RXD0	Receive data 0	P19_7	—
P20_0_V1833_0_ETH0_RXD1	Receive data 1	P20_0	—
P20_1_V1833_0_ETH0_RXD2	Receive data 2	P20_1	—
P20_2_V1833_0_ETH0_RXD3	Receive data 3	P20_2	—
P20_3_V1833_0_ETH0_RXDV	Receive data valid or error	P20_3	—
P20_4_P24_6_V1833_01_ETH0_MDC	MDI clock	P20_4*	SW12-3: ON
		P24_6*	SW12-3: OFF
P20_5_P24_7_V1833_01_ETH0_MDIO	MDI data	P20_5*	SW12-3: ON
		P24_7*	SW12-3: OFF
P21_0_V1833_0_PHY0_IRQ21	MDI interrupt input	P21_0	—
P20_6_V1833_0_ETHSW_PHYLINK0	Link status	P20_6	—
P20_7_V1833_0_ETH0_REFCLK	Clock output (25 MHz)	P20_7	—
P07_0_P05_7_ETH0_NRESET#	Reset output	P07_0*	SW12-3: ON
		P05_7*	SW12-3: OFF

Note: Connected via the bus switch IC. When SW12-3 is turned on, pins 2 and 3 of J41 should be short-circuit. When SW12-3 is turned off, pins 1 and 2 of J41 should be short-circuit.

Table 7-21 Signal Connections of Ethernet Port 1 (ETH1)

Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P21_1_V1833_0_ETH1_TXCLK	Transmit clock	P21_1	—
P21_2_V1833_0_ETH1_TXD0	Transmit data 0	P21_2	—
P21_3_V1833_0_ETH1_TXD1	Transmit data 1	P21_3	—
P21_4_V1833_0_ETH1_TXD2	Transmit data 2	P21_4	—
P21_5_V1833_0_ETH1_TXD3	Transmit data 3	P21_5	—
P21_6_V1833_0_ETH1_TXEN	Transmit data enable or error	P21_6	—
P21_7_V1833_0_ETH1_RXCLK	Receive clock	P21_7	—
P22_0_V1833_0_ETH1_RXD0	Receive data 0	P22_0	—
P22_1_V1833_0_ETH1_RXD1	Receive data 1	P22_1	—
P22_2_V1833_0_ETH1_RXD2	Receive data 2	P22_2	—
P22_3_V1833_0_ETH1_RXD3	Receive data 3	P22_3	—
P22_4_V1833_0_ETH1_RXDV	Receive data valid or error	P22_4	—
P20_4_V1833_0_ETH012_GAMC0_MDC_MD0	MDI clock	P20_4	—
P20_5_V1833_0_ETH012_GMAC0_MDIO	MDI data	P20_5	—
P22_7_V1833_0_PHY1_IRQ22	MDI interrupt input	P22_7	—
P22_5_V1833_0_ETHSW_PHYLINK1	Link status	P22_5	—
P22_6_V1833_0_ETH1_REFCLK	Clock output (25 MHz)	P22_6	—
P07_0_ESC012_RESETOUT#	Reset output	P07_0	—

Table 7-22 Signal Connections of Ethernet Port 2 (ETH2)

Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P23_0_V1833_1_ETH2_TXCLK	Transmit clock	P23_0	—
P23_1_V1833_1_ETH2_TXD0	Transmit data 0	P23_1*	SW7-2: ON
P23_2_V1833_1_ETH2_TXD1	Transmit data 1	P23_2*	
P23_3_V1833_1_ETH2_TXD2	Transmit data 2	P23_3	—
P23_4_V1833_1_ETH2_TXD3	Transmit data 3	P23_4*	SW7-2: ON
P23_5_V1833_1_ETH2_TXEN	Transmit data enable or error	P23_5*	
P23_6_V1833_1_ETH2_RXCLK	Receive clock	P23_6*	
P23_7_V1833_1_ETH2_RXD0	Receive data 0	P23_7*	
P24_0_V1833_1_ETH2_RXD1	Receive data 1	P24_0*	
P24_1_V1833_1_ETH2_RXD2	Receive data 2	P24_1*	
P24_2_V1833_1_ETH2_RXD3	Receive data 3	P24_2*	
P24_3_V1833_1_ETH2_RXDV	Receive data valid or error	P24_3*	
P20_4_P24_6_V1833_01_ETH2_MDC	MDI clock	P20_4*	SW12-4: ON
		P24_6*	SW12-4: OFF
P20_5_P24_7_V1833_01_ETH2_MDIO	MDI data	P20_5*	SW12-4: ON
		P24_7*	SW12-4: OFF
P07_6_PHY2_IRQ7	MDI interrupt input	P07_6	—
P25_0_V1833_1_ETHSW_PHYLINK2	Link status	P25_0*	SW7-2: ON
P24_4_V1833_1_ETH2_REFCLK	Clock output (25 MHz)	P24_4*	
P07_0_P05_7_ETH2_NRESET#	Reset output	P07_0*	SW12-4: ON
		P05_7*	SW12-4: OFF

Note: Connected via the bus switch IC. To use Ethernet port 2, pins 1 and 2 of J15 should be short-circuit and SW10-2 should be turned on.

Table 7-23 Signal Connections of Ethernet Port 3 (ETH3)

Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P00_0_V1833_2_ETH3_TXCLK	Transmit clock	P00_0*	SW7-3: ON
P00_1_V1833_2_ETH3_TXD0	Transmit data 0	P00_1*	
P00_2_V1833_2_ETH3_TXD1	Transmit data 1	P00_2*	
P00_3_V1833_2_ETH3_TXD2	Transmit data 2	P00_3*	
P00_4_V1833_2_ETH3_TXD3	Transmit data 3	P00_4*	
P00_5_V1833_2_ETH3_TXEN	Transmit data enable or error	P00_5*	
P00_6_V1833_2_ETH3_RXCLK	Receive clock	P00_6*	
P00_7_V1833_2_ETH3_RXD0	Receive data 0	P00_7*	
P01_0_V1833_2_ETH3_RXD1	Receive data 1	P01_0*	
P01_1_V1833_2_ETH3_RXD2	Receive data 2	P01_1*	
P01_2_V1833_2_ETH3_RXD3	Receive data 3	P01_2*	
P01_3_V1833_2_ETH3_RXDV_CRS_DV	Receive data valid , error, or carrier sense	P01_3*	
P16_7_V1833_4_ETH3_RXER	Receive data error	P16_7*	—
P03_2_V1833_2_ETH34_GMAC1_MDC_MD2	MDI clock	P03_2	
P03_3_V1833_2_ETH34_GMAC1_MDIO	MDI data	P03_3	
P06_0_PHY3_IRQ6	MDI interrupt input	P06_0	—
P01_5_V1833_2_PHY3_PHYLINK	Link status	P01_5*	SW7-3: ON
P01_4_V1833_2_ETH3_REFCLK	Clock output (25 MHz)	P01_4*	
P16_1_V1833_4_ETH34_RESETOUT	Reset output	P16_1*	

Note: Connected via the bus switch IC. To use Ethernet port 3 in the RGMII mode, pins 1 and 2 of J18 should be short-circuit and SW10-3 should be turned on. To use Ethernet port 3 in the RMII mode, pins 2 and 3 of J18 should be short-circuit and SW10-3 should be turned off.

Table 7-24 Signal Connections of Ethernet Port 4 (ETH4)

Signal Name	Function or Intended Use	MPU Port	Settings of Configuration Circuits
P01_6_V1833_2_ETH4_TXCLK	Transmit clock	P01_6*	SW7-4: ON
P01_7_V1833_2_ETH4_TXD0	Transmit data 0	P01_7*	
P02_0_V1833_2_ETH4_TXD1	Transmit data 1	P02_0*	
P02_1_V1833_2_ETH4_TXD2	Transmit data 2	P02_1*	
P02_2_V1833_2_ETH4_TXD3	Transmit data 3	P02_2*	
P02_3_V1833_2_ETH4_TXEN	Transmit data enable or error	P02_3*	
P02_4_V1833_2_ETH4_RXCLK	Receive clock	P02_4*	
P02_5_V1833_2_ETH4_RXD0	Receive data 0	P02_5*	
P02_6_V1833_2_ETH4_RXD1	Receive data 1	P02_6*	
P02_7_V1833_2_ETH4_RXD2	Receive data 2	P02_7*	
P03_0_V1833_2_ETH4_RXD3	Receive data 3	P03_0*	
P03_1_V1833_2_ETH4_RXDV_CRS_DV	Receive data enable, error, or carrier sense	P03_1*	
P07_1_ETH4_RXER	Receive data error	P07_1	—
P03_2_V1833_2_ETH34_GMAC1_MDC_MD2	MDI clock	P03_2	—
P03_3_V1833_2_ETH34_GMAC1_MDIO	MDI data	P03_3	—
P15_1_PHY4_IRQ15	MDI interrupt input	P15_1*	SW7-4: ON
P03_5_V1833_2_PHY4_PHYLINK	Link status	P03_5*	
P03_4_V1833_2_ETH4_REFCLK	Clock output (25 MHz)	P03_4*	
P16_1_V1833_4_ETH34_RESETOUT	Reset output	P16_1*	SW7-3: ON

Note: Connected via the bus switch IC. To use Ethernet port 4 in the RGMII mode, pins 1 and 2 of J18 should be short-circuit and SW10-3 should be turned on. To use Ethernet port 4 in the RMII mode, pins 2 and 3 of J18 should be short-circuit and SW10-3 should be turned off.

Table 7-25 Initial Settings by Hardware Strapping of the PHY Devices

Items of PHY Initial Settings	Contents of PHY Initial Settings
CLKOUT	Disable
Managed or unmanaged	Unmanaged mode
CLK delay	2.0 ns
Link advertisement	Default operating mode, 10, 100, or 1000 FDX/HDX, auto-nego is ON
MAC interface	PHY0 (U54), PHY1 (U57), PHY2 (U60): RGMII mode only PHY3 (U64), PHY4 (U41): RGMII mode (when R418, R456, R318, and R320 are DNF)
Selection of GMII/MII or RGMII/RMII	RGMII/RMII mode
PHY address	PHY 0 (U54): 0 (GMAC0) PHY 1 (U57): 1 (GMAC0) PHY 2 (U60): 2 (GMAC0) PHY 3 (U64): 0 (GMAC1) PHY 4 (U41): 1 (GMAC1)
Enabling of forced 1000-BT mode	Not set

Ethernet ports 0 to 2 are fixed to the 1.8-V/RGMII mode (pins 1 and 2 of J15 are short-circuit and SW10-2 is turned on). Ethernet ports 3 and 4 are set to the 1.8-V/RGMII mode on the board as shipped (pins 1 and 2 of J18 are short-circuit, SW10-3 is turned on, R396, R423, R429, R325, R331, and R464 are set as "fit", and R262, R338, R414, R431, R333, R436, R463, and R465 are set as DNF). When switching between the RMII and RGMII modes, change the settings with reference to Table 6-9 and Table 6-15.

7.15 PCIe

This board is equipped with a clock driver, a power-supply IC, and a connector (J6) for the PCIe so that the PCIe function of the RZ/T2N can be evaluated. Figure 7-18 shows the configuration of the PCIe circuit.

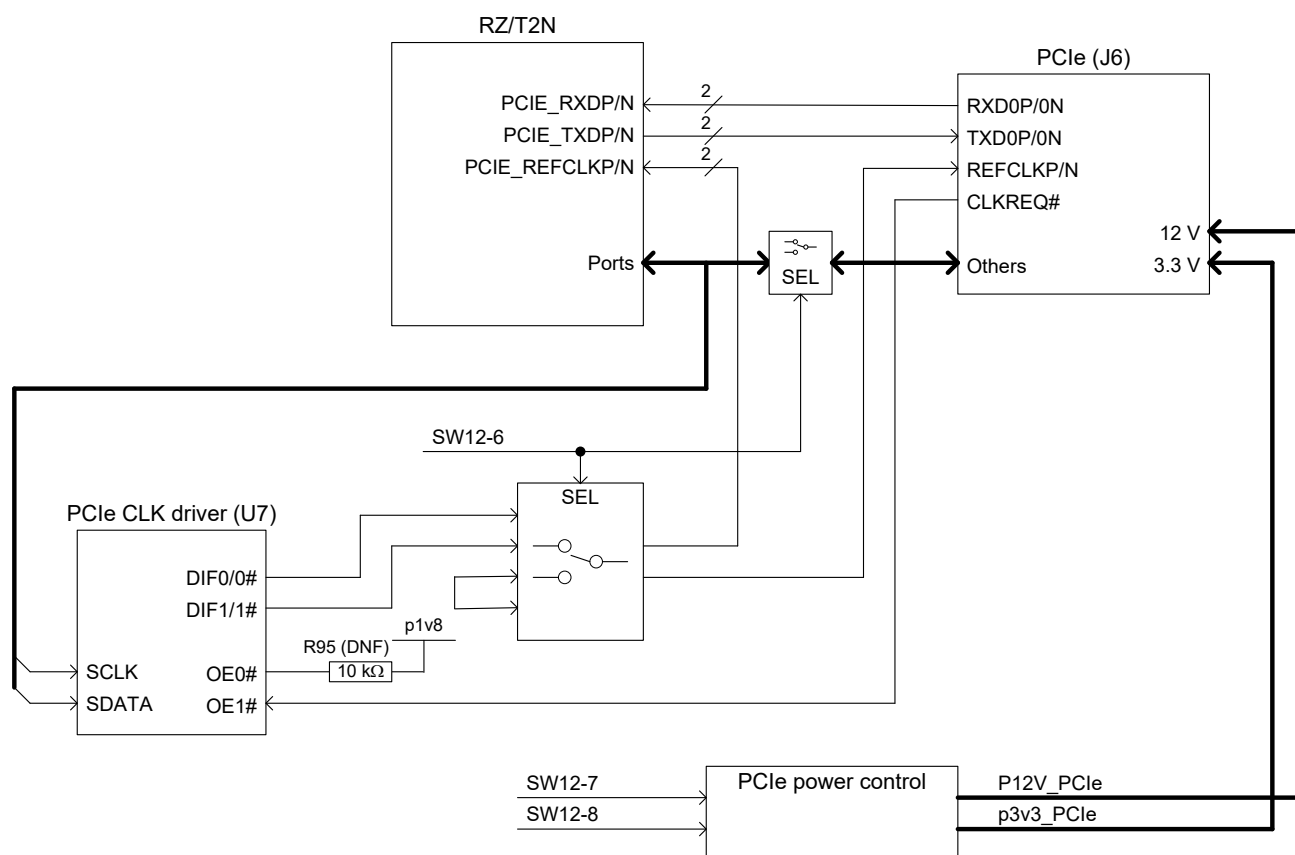


Figure 7-18 Configuration of the PCIe Circuit

The configuration of root complex or endpoint can be selected by setting SW12-6. In addition, the supply of power to the connector can be controlled by setting SW12-7 and SW12-8. However, since the connection of data signals to the connector is the same for an endpoint setting as for a root complex setting, a crossover cable should be used when performing evaluation. Table 7-26 and Figure 7-19 show the PCIe configurations and associated switch settings.

Table 7-26 PCIe Configurations and Associated Switch Settings (Excluding Signal Function Selection Switches)

Configuration No.	Description of Configuration	Settings of Switches
1	Root complex	SW12-6 : ON, SW12-7: ON, SW12-8: ON
2	Endpoint	SW12-6 : OFF, SW12-7 : OFF, SW12-8 : OFF

Table 7-27 lists the signal connections of the PCIe connector (J6) for a root complex. Table 7-28 lists the signal connections for an endpoint.

Table 7-27 Signal Connections of the PCIe Connector (J6) for a Root Complex

Pin* ¹	Function Name	Connection	MPU Port	Settings of Configuration Circuits* ²
A1	PRSNT1#	Fixed to the low level	—	—
A5	TCK	Pull-down	—	—
A6	TDI	Pull-up	—	—
A7	TDO	NC	—	—
A8	TMS	Pull-up	—	—
A11	PERST#	Connected to P24_5_V1833_1_PCIE_RSTOUTB_INV3_MDAT22	P24_5* ³	—
A13	REFCLK+	Clock driver output	—	—
A14	REFCLK-	Clock driver output	—	—
A16	HSIP0	Connected to PCIE_RXDP	—	—
A17	HSIN0	Connected to PCIE_RXDN	—	—
B5	SMCLK	Pull-up	—	—
B6	SMDAT	Pull-up	—	—
B9	TRST#	Pull-down	—	—
B10	3V3AUX	Connected to the 3.3-V power supply for the PCIe	—	—
B11	WAKE#	Connected to P06_5_PCIE_WAKE	P06_5	—
B12	CLKREQ#	Clock driver input	—	—
B14	HSOP0	Connected to PCIE_TXDP	—	—
B15	HSOIN0	Connected to PCIE_TXDN	—	—
B17	PRSNT2#	Connected to P06_4_PCIE_CLKREQ_PRST	P06_4	—

Notes: 1. The pins for power supplies (12-V, 3.3-V, and GND) and reserved pins are omitted.
 2. The switch settings listed in Table 7-26 are omitted.
 3. Pins 2 and 3 of J15 should be short-circuit and SW10-2 should be turned off.

Table 7-28 Signal Connections of the PCIe Connector (J6) for an Endpoint

Pin*1	Function Name	Connection	MPU Port	Settings of Configuration Circuits*2
A1	PRSNT1#	Connected to PRSNT2#	—	—
A5	TCK	Pull-down	—	—
A6	TDI	Pull-up	—	—
A7	TDO	NC	—	—
A8	TMS	Pull-up	—	—
A11	PERST#	Input to the reset IC via J1	—	—
A13	REFCLK+	Input to PCIE_REFCLK_T2N_P	—	—
A14	REFCLK-	Input to PCIE_REFCLK_T2N_N	—	—
A16	HSIP0	Connected to PCIE_RXDP	—	—
A17	HSIN0	Connected to PCIE_RXDN	—	—
B5	SMCLK	Pull-up	—	—
B6	SMDAT	Pull-up	—	—
B9	TRST#	Pull-down	—	—
B10	3V3AUX	Connected to the 3.3-V power supply for the PCIe	—	—
B11	WAKE#	Connected to P06_5_PCIE_WAKE	P06_5	—
B12	CLKREQ#	Connected to P06_4_PCIE_CLKREQ_PRSNT	P06_4	—
B14	HSOP0	Connected to PCIE_TXDP	—	—
B15	HSON0	Connected to PCIE_TXDN	—	—
B17	PRSNT2#	Connected to PRSNT1#	—	—

Notes: 1. The pins for power supplies (12-V, 3.3-V, and GND) and reserved pins are omitted.

2. The switch settings listed in Table 7-26 are omitted.

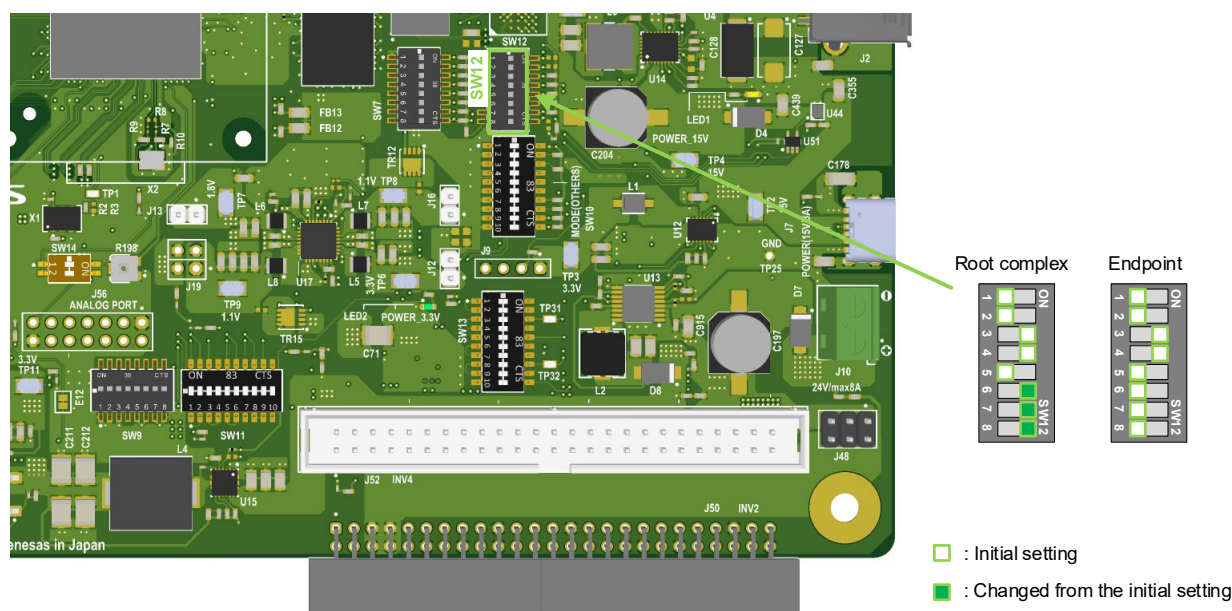


Figure 7-19 Switch Settings When Using PCIe

When endpoint mode is selected, the PCIe reset signal can be included in the system reset factors by short-circuiting J1. On the board as shipped, J1 is open-circuit.

7.16 Serial Host Interface

This board is equipped with a connector (J45) for the serial host interface, and the serial host interface of the RZ/T2N can be evaluated by connecting the connector to an external host CPU. Table 7-29 lists the signal connections of the serial host interface connector (J45). Figure 7-20 shows the switch settings when using the serial host interface.

Table 7-29 Signal Connections of the Serial Host Interface Connector (J45)

Pin	Signal Name	MPU Port	Settings of Configuration Circuits
1	GND	—	—
2	P04_4_V1833_5_HSPI_INT#	P04_4*1	SW7-7 : OFF, SW7-8: OFF
3	P05_2_V1833_5_HSPI_CK	P05_2*1	
4	P04_5_V1833_5_HSPI_CS#	P04_5*1	
5	P05_6_V1833_5_HSPI_IO7	P05_6*1	
6	P05_5_V1833_5_HSPI_IO6_PMOD2_IRQ5	P05_5*1	
7	P05_4_V1833_5_HSPI_IO5_PMOD2_TXD2	P05_4*1	
8	P05_3_V1833_5_HSPI_IO4_INV3_ENCIFDI05_PMOD2_RXD2	P05_3*1	
9	P05_1_V1833_5_HSPI_IO3_INV3_ENCIFOE05_PMOD2_RST	P05_1*1	
10	P05_0_V1833_5_HSPI_IO2_INV3_ENCIFCK05	P05_0*1	
11	P04_7_V1833_5_HSPI_IO1	P04_7*1	
12	P04_6_V1833_5_HSPI_IO0	P04_6*1	
13	P11_7_INV2_GTETRGB_MBX_HINT#	P11_7*2	SW11-3 : OFF, SW11-4 : ON
14	p3v3	—	—

Notes: 1. Connected via the bus switch IC. To use the serial host interface, pins 2 and 3 of J39 should be short-circuit and SW10-6 should be turned off.
2. Connected via SW11.

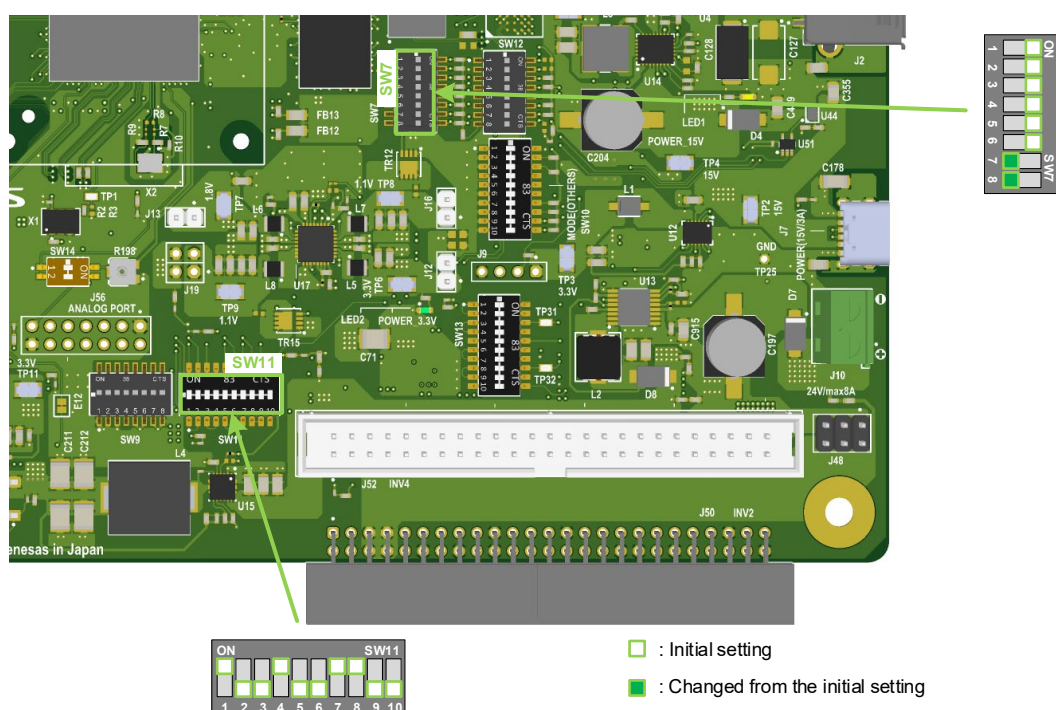


Figure 7-20 Switch Settings When Using the Serial Host Interface

7.17 Inverter Board Interfaces

This board is equipped with connectors (J49 to J52) for inverter board interfaces and the functions of the RZ/T2N that are related to motor driving can be evaluated by connecting inverter boards. Table 7-30 to Table 7-33 list the signal connections of the inverter board interface connectors (J49 to J52). Figure 7-21 to Figure 7-24 show the switch settings when using the inverter board interfaces.

Table 7-30 Signal Connections of Inverter Board Interface Connector INV1 (J49)

Pin	Signal Name	MPU Port	Settings of Configuration Circuits
1-4	P24V_INV	—	—
5-8	GND_24V	—	—
9	INV1_AN204	—	—
10	NC	—	—
11	p1v8_LDO	—	—
12	GND	—	—
13	NC	—	—
14	NC	—	—
15	NC	—	—
16	GND	—	—
17, 18	INV_3V3	—	—
19, 20	GND	—	—
21	P01_2_V1833_2_BSC_BS#_INV1_MCLK00	P01_2*	SW7-3: OFF
22	P06_1_INV1_MDAT00	P06_1	—
23	P06_2_INV1_MCLK01	P06_2	—
24	P01_5_V1833_2_BSC_CS2#_INV1_MDAT01	P01_5*	SW7-3: OFF
25	P01_6_V1833_2_BSC_D13_INV1_MCLK02	P01_6*	SW7-4: OFF
26	P01_7_V1833_2_BSC_D14_INV1_MDAT02	P01_7*	—
27	GND	—	—
28	P00_0_V1833_2_BSC_A16_INV1_GTI0C00_0A	P00_0*	SW7-3: OFF
29	P00_1_V1833_2_BSC_A17_INV1_GTI0C00_0B	P00_1*	
30	P00_3_V1833_2_BSC_A19_INV1_GTI0C00_1A	P00_3*	
31	P00_2_V1833_2_BSC_A18_INV1_GTI0C00_1B	P00_2*	
32	P00_4_V1833_2_BSC_A20_INV1_GTI0C00_2A	P00_4*	
33	P00_5_V1833_2_BSC_A21_INV1_GTI0C00_2B	P00_5*	
34	GND	—	—
35	P11_5_INV1_GTETRGA	P11_5	E12: Short-circuit
36	GND	—	—
37	P00_6_V1833_2_INV1_GTI0C00_3A	P00_6*	SW7-3: OFF, SW9-5: ON
38	P00_7_V1833_2_INV1_GTI0C00_3B	P00_7*	
39	P01_0_V1833_2_INV1_GTI0C00_4A	P01_0*	
40	GND	—	—
41	P00_6_V1833_2_INV1_ENCIFCK00	P00_6*	SW7-3: OFF, SW9-5: OFF
42	P00_7_V1833_2_INV1_ENCIFOE00	P00_7*	
43	P01_0_V1833_2_INV1_ENCIFDO00	P01_0*	
44	P01_1_V1833_2_BSC_RD/WR#_INV1_ENCIFDI00	P01_1*	SW7-3: OFF
45	GND	—	—
46	P18_3_V1833_3_INV1_ENCIFCK04	P18_3*	SW7-6: OFF
47	P18_4_V1833_3_INV1_ENCIFOE04	P18_4*	
48	P09_5_BSC_A1_INV1_ENCIFDO04_MDV2	P09_5	—
49	P09_2_BSC_WAIT#_INV1_ENCIFDI04	P09_2	—
50	GND	—	—

Note: Connected via the bus switch IC. To use INV1, pins 2 and 3 of J18 should be short-circuit and SW10-3 should be turned off.

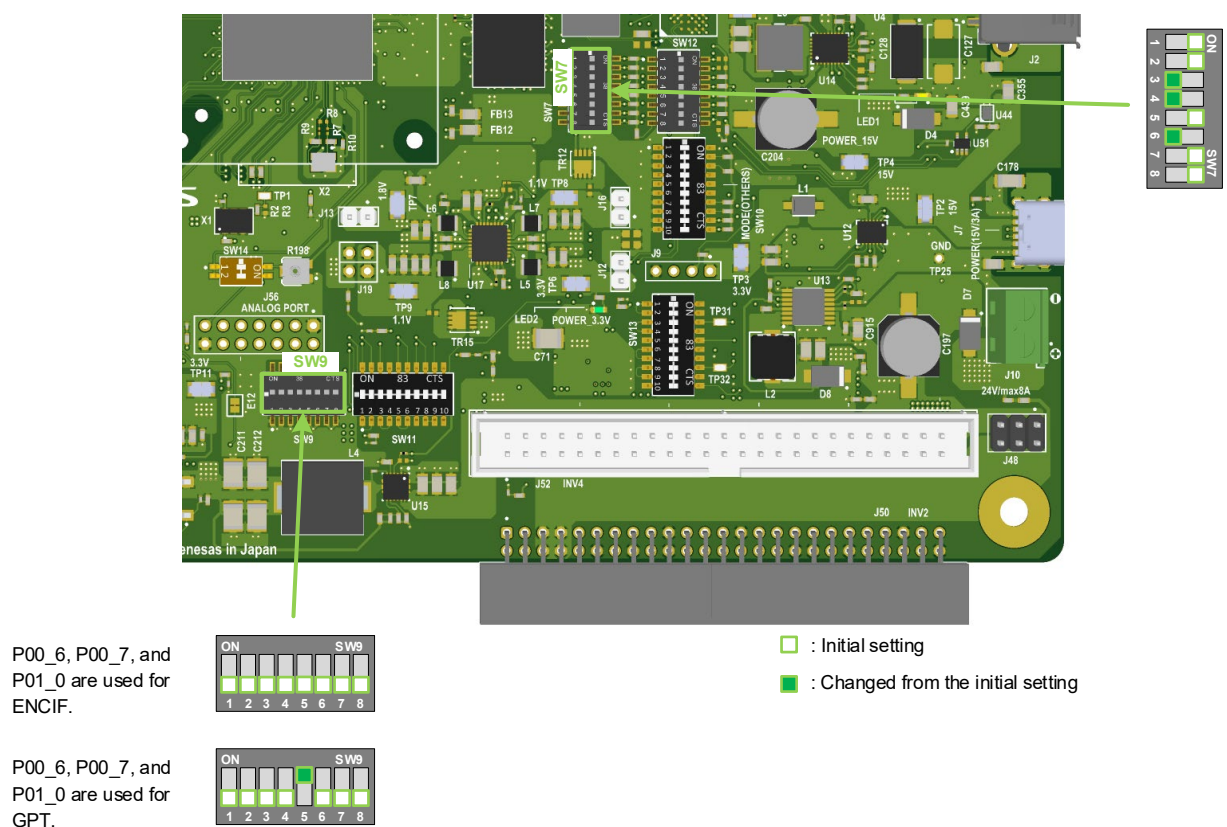


Figure 7-21 Switch Settings When Using Inverter Board Interface Connector INV1 (J49)

Table 7-31 Signal Connections of Inverter Board Interface Connector INV2 (J50)

Pin	Signal Name	MPU Port	Settings of Configuration Circuits
1-4	P24V_INV	—	—
5-8	GND_24V	—	—
9	INV2_AN205	—	—
10	NC	—	—
11	p1v8_LDO	—	—
12	GND	—	—
13	NC	—	—
14	NC	—	—
15	NC	—	—
16	GND	—	—
17, 18	INV_3V3	—	—
19, 20	GND	—	—
21	P03_0_V1833_2_BSC_A14_INV2_MCLK10_PMOD2_CTS2#	P03_0*1	SW7-4: OFF
22	P03_1_V1833_2_BSC_A15_ETHSW_PTPOUT3_INV2_MDAT10	P03_1*1	
23	P24_1_V1833_1_BSC_DACK_INV2_MCLK11	P24_1*1	SW7-2: OFF
24	P24_2_V1833_1_BSC_TEND_INV2_MDAT11	P24_2*1	
25	P24_4_V1833_1_INV2_MCLK12	P24_4*1	
26	P24_3_V1833_1_INV2_MDAT12	P24_3*1	
27	GND	—	—
28	P14_1_BSC_D0_INV2_GTI0C02_0A_USER_LED0	P14_1	—
29	P14_2_BSC_D1_INV2_GTI0C02_0B_USER_LED1	P14_2	—
30	P14_4_BSC_D3_INV2_GTI0C02_1A	P14_4	—
31	P14_5_BSC_D4_INV2_GTI0C02_1B_USER_LED2	P14_5	—
32	P14_6_BSC_D5_INV2_GTI0C02_2A_USER_LED3	P14_6	—
33	P14_7_BSC_D6_INV2_GTI0C02_2B	P14_7	—
34	GND	—	—
35	P11_7_INV2_GTETRGB_MBX_HINT#	P11_7*2	SW11-3: OFF, SW11-4: ON
36	GND	—	—
37	P02_4_V1833_2_INV2_GTI0C01_3A	P02_4*1	SW7-4: OFF, SW9-6: ON
38	P02_5_V1833_2_INV2_GTI0C01_3B	P02_5*1	
39	P02_6_V1833_2_INV2_GTI0C01_4A	P02_6*1	SW7-4: OFF, SW9-6: OFF
40	GND	—	
41	P02_4_V1833_2_INV2_ENCIFCK01	P02_4*1	
42	P02_5_V1833_2_INV2_ENCIFOE01	P02_5*1	
43	P02_6_V1833_2_INV2_ENCIFDO01	P02_6*1	SW7-4: OFF
44	P02_7_V1833_2_BSC_A13_INV2_ENCIFDI01_PMOD2_RTS2#	P02_7*1	
45	GND	—	—
46	P09_7_BSC_A3_INV2_ENCIFCK06_ETHSW_TDMAOUT1_ESC_LINKACT2_MDV4	P09_7	—
47	P10_0_BSC_A4_XSPI1_IRQ10_INV2_ENCIFOE06_ETHSW_TDMAOUT2_MDV5	P10_0	—
48	P09_6_BSC_A2_INV2_ENCIFDO06_ETHSW_TDMAOUT0	P09_6*1	Any settings other than the combination of SW7-7: OFF and SW7-8: ON*3
49	P15_7_V1833_4_INV2_ENCIFDI06	P15_7*1	SW7-5: OFF
50	GND	—	—

- Notes: 1. Connected via the bus switch IC. To use INV2, pins 2 and 3 of J15 and J18 should be short-circuit and SW10-2 and SW10-3 should be turned off.
2. Connected via SW11.
3. This signal is also used as a signal for controlling the NAND flash memory. To use it as an inverter board interface signal, SW7-7 and SW7-8 should be set to a combination other than SW7-7 = OFF and SW7-8 = ON (such settings are for using the signal as a NAND flash memory control signal).

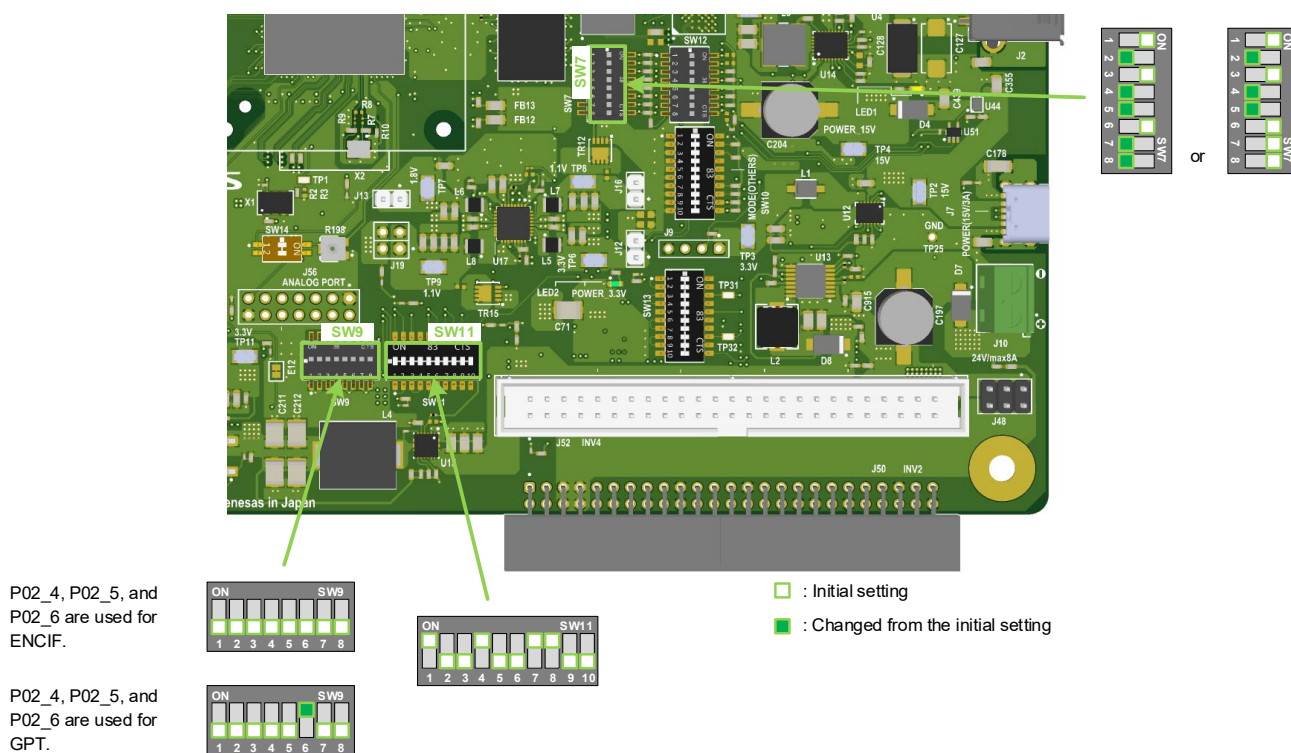


Figure 7-22 Switch Settings When Using Inverter Board Interface Connector INV2 (J50)

Table 7-32 Signal Connections of Inverter Board Interface Connector INV3 (J51)

Pin	Signal Name	MPU Port	Settings of Configuration Circuits
1-4	P24V_INV	—	—
5-8	GND_24V	—	—
9	INV3_AN206	—	—
10	NC	—	—
11	p1v8_LDO	—	—
12	GND	—	—
13	NC	—	—
14	NC	—	—
15	NC	—	—
16	GND	—	—
17, 18	INV_3V3	—	—
19, 20	GND	—	—
21	P18_5_V1833_3_INV3_MCLK20	P18_5*	SW7-6: OFF
22	P18_6_V1833_3_INV3_MDAT20	P18_6*	
23	P23_1_V1833_1_INV3_MCLK21	P23_1*	SW7-2: OFF
24	P23_2_V1833_1_INV3_MDAT21	P23_2*	
25	P25_0_V1833_1_INV3_MCLK22	P25_0*	
26	P24_5_V1833_1_PCIE_RSTOUTB_INV3_MDAT22	P24_5	—
27	GND	—	—
28	P03_6_V1833_6_INV3_GTI0C01_0A	P03_6*	SW7-1: OFF
29	P03_7_V1833_6_INV3_GTI0C01_0B	P03_7*	
30	P04_1_V1833_6_INV3_GTI0C01_1A	P04_1*	
31	P04_0_V1833_6_INV3_GTI0C01_1B	P04_0*	
32	P04_2_V1833_6_INV3_GTI0C01_2A	P04_2*	
33	P04_3_V1833_6_INV3_GTI0C01_2B	P04_3*	
34	GND	—	—
35	P07_7_INV3_GTETRGC	P07_7	—
36	GND	—	—
37	P15_0_INV3_GTI0C02_3A	P15_0*	SW7-1: OFF, SW9-7: ON
38	P15_1_INV3_GTI0C02_3B	P15_1*	SW7-4: OFF, SW9-7: ON
39	P15_2_INV3_GTI0C02_4A	P15_2*	SW9-7: ON
40	GND	—	—
41	P15_0_INV3_ENCIFCK02	P15_0*	SW7-1: OFF, SW9-7: OFF
42	P15_1_INV3_ENCIFOE02	P15_1*	SW7-4: OFF, SW9-7: OFF
43	P15_2_INV3_ENCIFDO02	P15_2*	SW9-7: OFF
44	P15_3_BSC_D10_INV3_ENCIFDI02	P15_3	—
45	GND	—	—
46	P05_0_V1833_5_HSPI_IO2_INV3_ENCIFCK05	P05_0*	SW7-7: OFF, SW7-8: OFF
47	P05_1_V1833_5_HSPI_IO3_INV3_ENCIFOE05_PMOD2_RST	P05_1*	SW7-7: OFF, SW7-8: OFF, R188: Fit
48	P05_2_V1833_5_INV3_ENCIFDO05	P05_2*	
49	P05_3_V1833_5_HSPI_IO4_INV3_ENCIFDI05_PMOD2_RXD2	P05_3*	SW7-7: OFF, SW7-8: OFF
50	GND	—	—

Note: Connected via the bus switch IC. To use INV3, pins 2 and 3 of J15 and J39 should be short-circuit, SW10-2 and SW10-6 should be turned off, and pins 1 and 2 of J25 should be short-circuit.

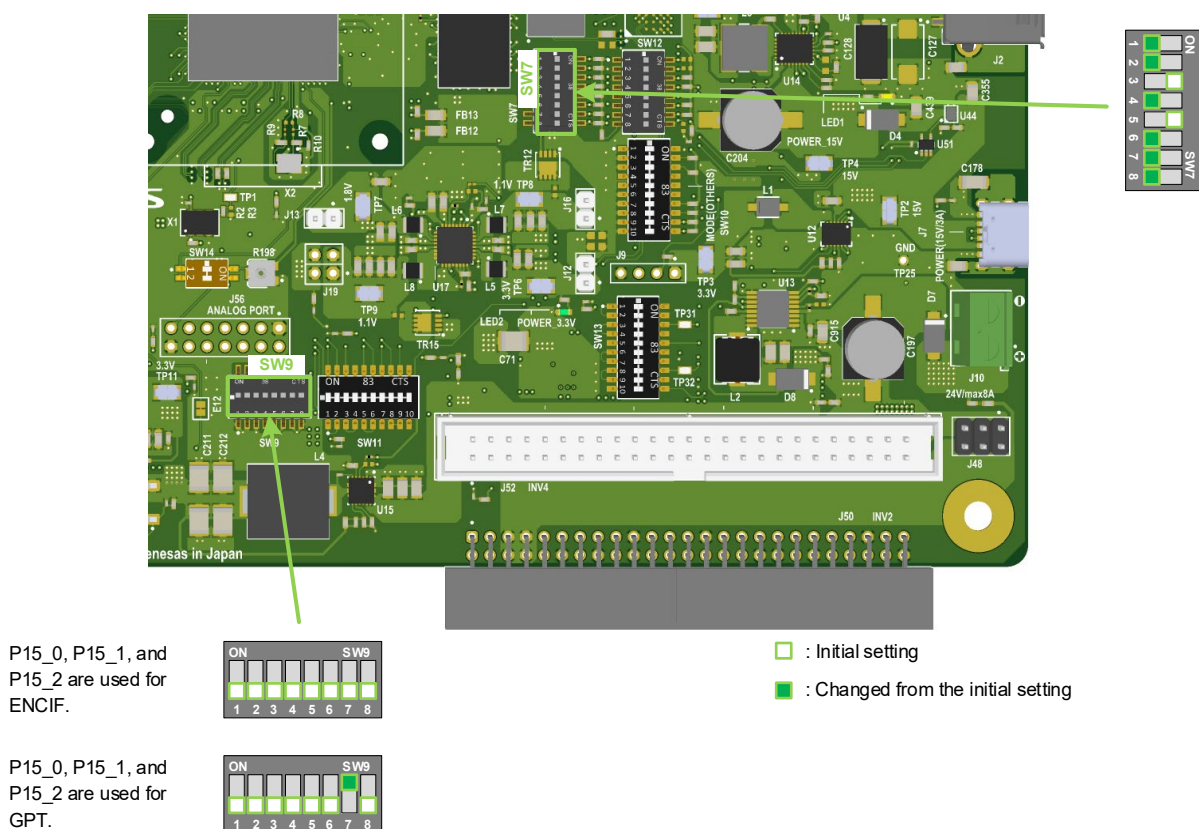


Figure 7-23 Switch Settings When Using Inverter Board Interface Connector INV3 (J51)

Table 7-33 Signal Connections of Inverter Board Interface Connector INV4 (J52)

Pin	Signal Name	MPU Port	Settings of Configuration Circuits
1-4	P24V_INV	—	—
5-8	GND_24V	—	—
9	INV4_AN207	—	—
10	NC	—	—
11	p1v8_LDO	—	—
12	GND	—	—
13	NC	—	—
14	NC	—	—
15	NC	—	—
16	GND	—	—
17, 18	INV_3V3	—	—
19, 20	GND	—	—
21	P23_5_V1833_1_INV4_MCLK30	P23_5*1	SW7-2 : OFF
22	P23_6_V1833_1_INV4_MDAT30	P23_6*1	
23	P09_3_BSC_CS0#_INV4_MCLK31	P09_3*1	SW9-3 : OFF
24	P09_4_BSC_RD#_INV4_MDAT31	P09_4*1	Any settings other than the combination of SW7-7 : OFF and SW7-8 : ON*3
25	P23_7_V1833_1_INV4_MCLK32	P23_7*1	SW7-2: OFF
26	P24_0_V1833_1_BSC_DREQ_INV4_MDAT32	P24_0*1	
27	GND	—	—
28	P16_0_V1833_4_XSPI1_CS1#_INV4_GTIOC03_0A_PMO D1_RST	P16_0	—
29	P16_1_V1833_4_INV4_GTIOC03_0B	P16_1*1	SW7-3: OFF
30	P16_3_V1833_4_INV4_GTIOC03_1A_PMOD1_SSL02	P16_3*1	SW7-5: OFF
31	P16_2_V1833_4_INV4_GTIOC03_1B_PMOD1_SSL01	P16_2*1	
32	P16_4_V1833_4_INV4_GTIOC03_2A_PMOD1_MISO0	P16_4*1	
33	P16_5_V1833_4_INV4_GTIOC03_2B_PMOD1_MOSI0	P16_5*1	
34	GND	—	—
35	P02_0_V1833_2_INV4_GTETRGD_ETHSW_PTPOUT0	P02_0*1	SW7-4: OFF
36	GND	—	—
37	P16_6_V1833_4_INV4_GTIOC03_3A	P16_6*1	SW9-8 : ON, SW12-5 : ON
38	P16_7_V1833_4_INV4_GTIOC03_3B	P16_7*1	SW7-3: OFF, SW9-8 : ON, SW12-5 : ON
39	P17_0_V1833_4_INV4_GTIOC03_4A	P17_0*1*2	SW9-8 : ON, SW12-5 : ON, SW13-1 : ON, SW13-2 : OFF
40	GND	—	—
41	P16_6_V1833_4_INV4_ENCIFCK03	P16_6*1	SW9-8 : OFF, SW12-5 : ON
42	P16_7_V1833_4_INV4_ENCIFOE03	P16_7*1	SW7-3: OFF, SW9-8 : OFF, SW12-5 : ON
43	P17_0_V1833_4_INV4_ENCIFDO03	P17_0*1*2	SW9-8 : OFF, SW12-5 : ON, SW13-1 : ON, SW13-2 : OFF
44	P17_1_V1833_4_XSPI1_IO7_INV4_ENCIFDI03	P17_1*2	SW13-6 : ON, SW13-7 : OFF
45	GND	—	—
46	P09_1_BSC_WE1#_INV4_ENCIFCK07_MDV1	P09_1	—
47	P08_7_BSC_A8_INV4_ENCIFOE07	P08_7*1	SW9-3 : OFF
48	P09_0_BSC_WE0#_INV4_ENCIFDO07_ETHSW_PTPOU T1_MDV0	P09_0	—
49	P17_5_INV4_V1833_3_ENCIFDI07	P17_5*1	SW7-6: OFF
50	GND	—	—

- Notes:
1. Connected via the bus switch IC. To use INV4, pins 2 and 3 of J15 and J18 should be short-circuit and SW10-2 and SW10-3 should be turned off.
 2. Connected via SW13.
 3. This signal is also used as a signal for controlling the NAND flash memory. To use it as an inverter board interface signal, SW7-7 and SW7-8 should be set to a combination other than SW7-7 = OFF and SW7-8 = ON (such settings are for using the signal as a NAND flash memory control signal).

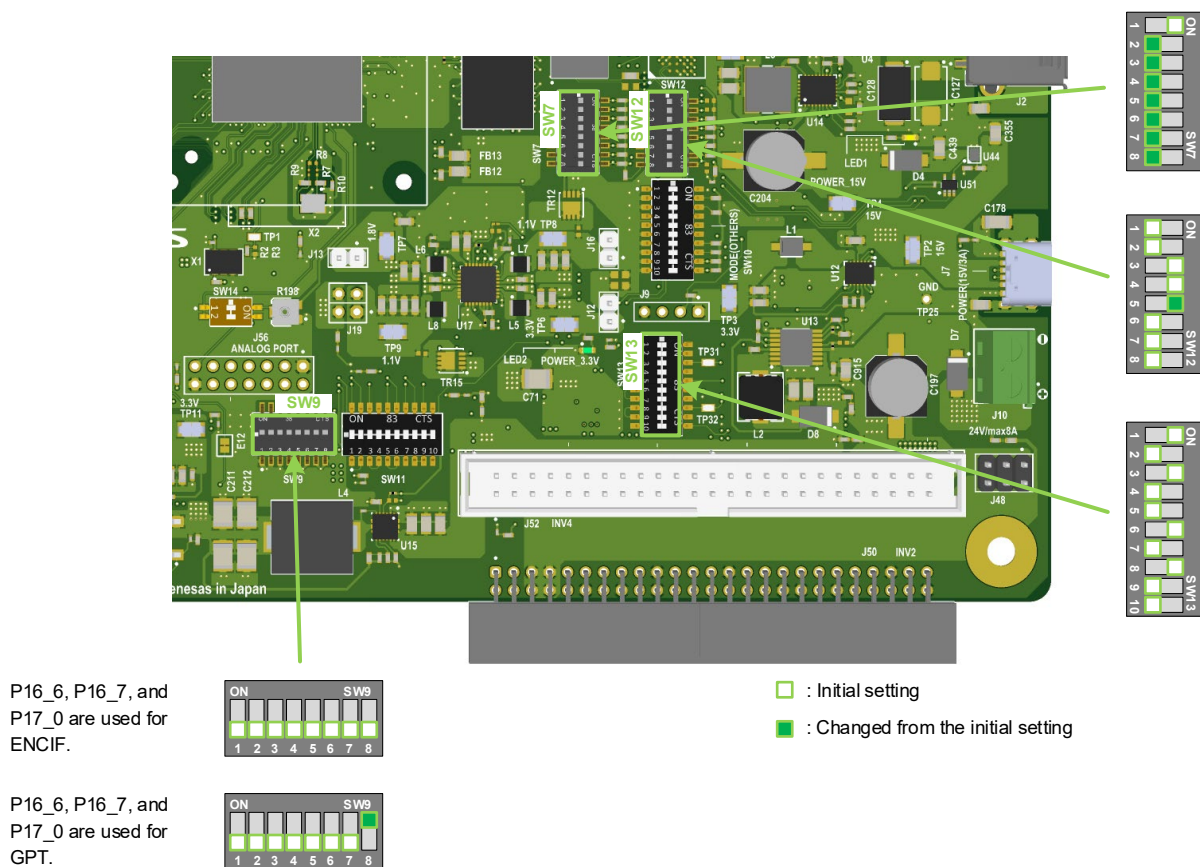


Figure 7-24 Switch Settings When Using Inverter Board Interface Connector INV4 (J52)

7.18 RMW Interface

This board is equipped with a connector (J40) for serial communications with the communication board (RTK0EMXC90Z00000BJ), which is used for evaluation through the Renesas Motor Workbench (RMW), a development support tool for evaluating motor control. Table 7-34 lists the signal connections of the RMW interface connector (J40).

Table 7-34 Signal Connections of the RMW Interface Connector (J40)

Pin	Signal Name	MPU Port	Settings of Configuration Circuits
1	GND	—	—
2	P06_6_RM_W_RXD4	P06_6	—
3	P06_7_RM_W_TXD4	P06_7	—
4	p3v3	—	—

7.19 Pin Headers and Socket

This board is equipped with the 2.54-mm pitch pin headers and a socket listed in Table 7-35. Table 7-36 to Table 7-39 list the signal connections of the pin headers and socket. Figure 7-25 to Figure 7-27 show the switch settings when using the pin headers and socket.

Table 7-35 List of Pin Headers and Socket

Function	Reference	Number of Pins	Description
Bus interface (BSC1, BSC2)	J46	40 (20 × 2)	For the address line and others
	J47	40 (20 × 2)	For the data line and others
GPIO connector	J55	14 (7 × 2)	For digital ports
ADC connector	J56	14 (7 × 2)	For analog ports

Table 7-36 Signal Connections of BSC1 (J46)

Pin	Signal Name	MPU Port	Settings of Configuration Circuits
1	P01_0_V1833_2_BSC_A0_INV1_GTIOC00_4A_ENCIFO00	P01_0*1	SW7-3 : OFF
2	p3v3	—	—
3	P09_5_BSC_A1_INV1_ENCIFO04_MDV2	P09_5	—
4	P00_0_V1833_2_BSC_A16_INV1_GTIOC00_0A	P00_0*1	SW7-3: OFF
5	P09_6_BSC_A2_INV2_ENCIFO06_ETHSW_TDMAOUT0	P09_6*1	Any settings other than the combination of SW7-7: OFF and SW7-8: ON *2
6	P00_1_V1833_2_BSC_A17_INV1_GTIOC00_0B	P00_1*1	SW7-3: OFF
7	P09_7_BSC_A3_INV2_ENCIFCK06_ETHSW_TDMAOUT1_ESC_LINKACT2_MDV4	P09_7	—
8	P00_2_V1833_2_BSC_A18_INV1_GTIOC00_1B	P00_2*1	SW7-3: OFF
9	P10_0_BSC_A4_XSPI1_IRQ10_INV2_ENCIFOE06_ETHSW_TDMAOUT2_MDV5	P10_0	—
10	P00_3_V1833_2_BSC_A19_INV1_GTIOC00_1A	P00_3*1	SW7-3: OFF
11	GND	—	—
12	P00_4_V1833_2_BSC_A20_INV1_GTIOC00_2A	P00_4*1	SW7-3: OFF
13	P10_1_BSC_A5_ESC_LED RUN_ETHSW_TDMAOUT3_MDB	P10_1	—
14	P00_5_V1833_2_BSC_A21_INV1_GTIOC00_2B	P00_5*1	SW7-3: OFF
15	P08_5_BSC_A6_XSPI1_IRQ8	P08_5*1	SW9-3: OFF
16	P00_6_V1833_2_BSC_A22_INV1_GTIOC00_3A_ENCIFCK00	P00_6*1	SW7-3: OFF
17	P08_6_BSC_A7	P08_6*1	SW9-3: OFF
18	P00_7_V1833_2_BSC_A23_INV1_GTIOC00_3B_ENCIFOE00	P00_7*1	SW7-3: OFF
19	P08_7_BSC_A8_INV4_ENCIFOE07	P08_7*1	SW9-3: OFF
20	P01_4_V1833_2_BSC_CS5#	P01_4*1	SW7-3: OFF
21	P02_3_V1833_2_BSC_A9_GMAC1_PTPTRG0	P02_3*1	SW7-4: OFF
22	P03_4_V1833_2_BSC_A24	P03_4*1	
23	P02_4_V1833_2_BSC_A10_INV2_GTIOC01_3A_ENCIFCK01_GMAC1_PTPTRG1	P02_4*1	
24	P03_5_V1833_2_BSC_A25	P03_5*1	
25	P02_5_V1833_2_BSC_A11_INV2_GTIOC01_3B_ENCIFOE01_GMAC2_PTPTRG1	P02_5*1	
26	P24_1_V1833_1_BSC_DACK_INV2_MCLK11	P24_1*1	SW7-2: OFF
27	P02_6_V1833_2_BSC_A12_INV2_GTIOC01_4A_ENCIFO01_GMAC2_PTPTRG0	P02_6*1	SW7-4: OFF
28	P24_0_V1833_1_BSC_DREQ_INV4_MDAT32	P24_0*1	SW7-2: OFF
29	GND	—	—
30	P01_2_V1833_2_BSC_BS#_INV1_MCLK00	P01_2*1	SW7-3: OFF
31	P02_7_V1833_2_BSC_A13_INV2_ENCIFDI01_PMOD2_RTS2#	P02_7*1	SW7-4: OFF
32	P09_3_BSC_CS0#_INV4_MCLK31	P09_3*1	SW9-3: OFF
33	P03_0_V1833_2_BSC_A14_INV2_MCLK10_PMOD2_CTS2#	P03_0*1	SW7-4: OFF
34	P01_5_V1833_2_BSC_CS2#_INV1_MDAT01	P01_5*1	SW7-3: OFF
35	P03_1_V1833_2_BSC_A15_ETHSW_PTPOUT3_INV2_MDAT10	P03_1*1	SW7-4: OFF
36	P01_3_V1833_2_BSC_CS3#	P01_3*1	SW7-3: OFF
37	NC	—	—
38	P01_1_V1833_2_BSC_RD/WR#_INV1_ENCIFDI00	P01_1*1	SW7-3: OFF
39	P09_4_BSC_RD#_INV4_MDAT31	P09_4*1	Any settings other than the combination of SW7-7: OFF and SW7-8: ON *2
40	P24_2_V1833_1_BSC_TEND_INV2_MDAT11	P24_2*1	SW7-2: OFF

- Notes:
1. Connected via the bus switch IC. To use BSC1, pins 2 and 3 of J15 and J18 should be short-circuit and SW10-2 and SW10-3 should be turned off.
 2. This signal is also used as a signal for controlling the NAND flash memory. To use it as an inverter board interface signal, SW7-7 and SW7-8 should be set to a combination other than SW7-7 = OFF and SW7-8 = ON (such settings are for using the signal as a NAND flash memory control signal).

Table 7-37 Signal Connections of BSC2 (J47)

Pin	Signal Name	MPU Port	Settings of Configuration Circuits
1	P14_1_BSC_D0_INV2_GTI0C02_0A_USER_LED0	P14_1	—
2	P11_5_BSC_CKIO_INV1_GTETRG	P11_5	—
3	P14_2_BSC_D1_INV2_GTI0C02_0B_USER_LED1	P14_2	—
4	NC	—	—
5	P14_3_BSC_D2	P14_3*1	SW11-8 : OFF, SW11-9: ON
6	NC	—	—
7	P14_4_BSC_D3_INV2_GTI0C02_1A	P14_4	—
8	NC	—	—
9	P14_5_BSC_D4_INV2_GTI0C02_1B_USER_LED2	P14_5	—
10	NC	—	—
11	GND	—	—
12	NC	—	—
13	P14_6_BSC_D5_INV2_GTI0C02_2A_USER_LED3	P14_6	—
14	NC	—	—
15	P14_7_BSC_D6_INV2_GTI0C02_2B	P14_7	—
16	NC	—	—
17	P15_0_BSC_D7_INV3_GTI0C02_3A_ENCIFCK02	P15_0*2	SW7-1 : OFF
18	NC	—	—
19	P15_1_BSC_D8_INV3_GTI0C02_3B_ENCIFOE02	P15_1*2	SW7-4: OFF
20	NC	—	—
21	P15_2_BSC_D9_INV3_GTI0C02_4A_ENCIFDO02	P15_2	—
22	NC	—	—
23	P15_3_BSC_D10_INV3_ENCIFDI02	P15_3	—
24	NC	—	—
25	P15_4_BSC_D11_PMOD2_GPIO0	P15_4*1	SW13-3 : OFF, SW13-4: ON, SW13-5 : OFF
26	NC	—	—
27	P15_5_BSC_D12_PMOD2_GPIO1	P15_5*1	SW13-8: OFF, SW13-9: ON, SW13-10 : OFF
28	NC	—	—
29	GND	—	—
30	NC	—	—
31	P01_6_V1833_2_BSC_D13_INV1_MCLK02	P01_6*2	SW7-4: OFF
32	NC	—	—
33	P01_7_V1833_2_BSC_D14_INV1_MDAT02	P01_7*2	SW7-4: OFF
34	P09_2_BSC_WAIT#_INV1_ENCIFDI04	P09_2	—
35	P02_2_V1833_2_BSC_D15_GMAC0_PTPTRG1	P02_2*2	SW7-4: OFF
36	P09_0_BSC_WE0#_INV4_ENCIFDO07_ETHSW_PTPOUT1_MDV0	P09_0	—
37	NC	—	—
38	P09_1_BSC_WE1#_INV4_ENCIFCK07_MDV1	P09_1	—
39	NC	—	—
40	P02_1_V1833_2_BSC_AH#_PMOD1_IRQ2_GMAC0_PTPT RG0	P02_1*2	SW7-4: OFF

Notes: 1. Connected via SW11 or SW13.

2. Connected via the bus switch IC. To use BSC2, pins 2 and 3 of J18 should be short-circuit and SW10-3 should be turned off.

Table 7-38 Signal Connections of the GPIO Connector (J55)

Pin	Signal Name	MPU Port	Settings of Configuration Circuits
1	GND	—	—
2	GND	—	—
3	P12_6_IOPORTS_MDAT40	P12_6	—
4	P12_5_IOPORTS_MCLK40	P12_5	—
5	P10_5_IOPORTS_GPIO	P10_5	—
6	P10_6_IOPORTS_GPIO	P10_6	—
7	P10_7_IOPORTS_GPIO	P10_7	—
8	P12_7_IOPORTS_GPIO	P12_7	—
9	p3v3	—	—
10	P13_4_IOPORTS_GPIO	P13_4	—
11	P13_0_IOPORTS_GPIO	P13_0	—
12	P23_4_V1833_1_IOPORTS_GPIO_ETHSW_PTPOUT2	P23_4*	SW7-2 : OFF
13	GND	—	—
14	GND	—	—

Note: Connected via the bus switch IC. To use the GPIO connector, pins 2 and 3 of J15 should be short-circuit and SW10-2 should be turned off.

Table 7-39 Signal Connections of the ADC Connector (J56)

Pin	Signal Name	MPU Port	Settings of Configuration Circuits
1	GND	—	—
2	ADC_AN203	—	—
3	ADC_AN202	—	—
4	ADC_AN201	—	—
5	ADC_AN200	—	—
6	ADC_AN103	—	—
7	ADC_AN102	—	—
8	ADC_AN101	—	—
9	ADC_AN100	—	—
10	ADC_AN003	—	—
11	ADC_AN002	—	—
12	ADC_AN001	—	—
13	ADC_AN000	—*	SW14-1 : OFF, SW14-2 : ON
14	GND	—	—

Note: Connected via SW14.

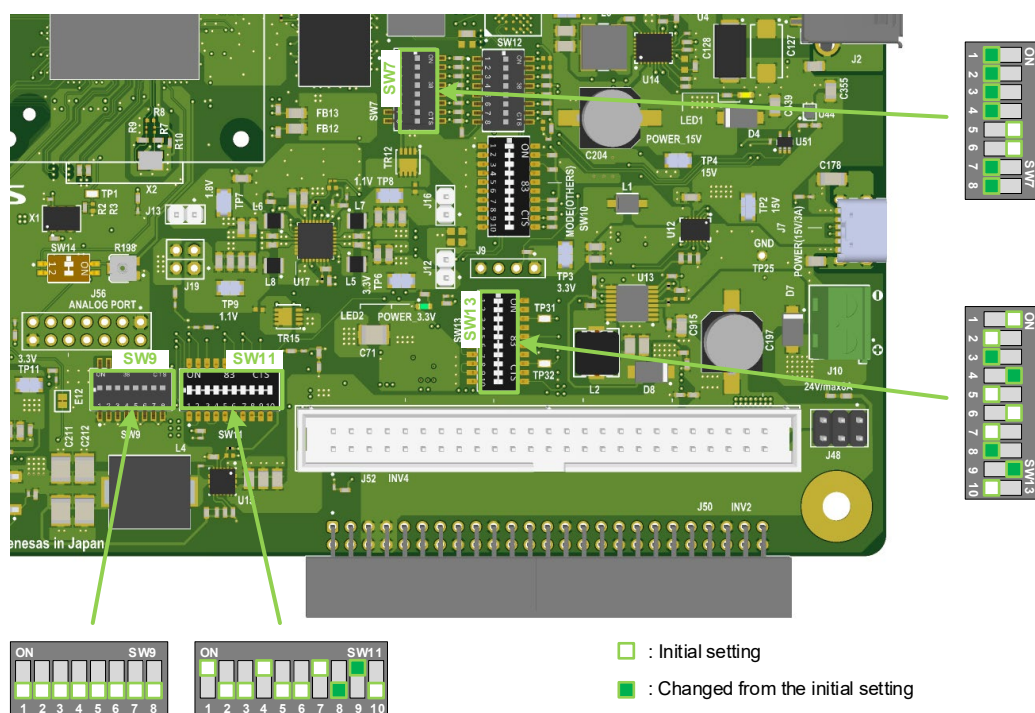


Figure 7-25 Switch Settings When Using BSC1 (J46) and BSC2 (J47)

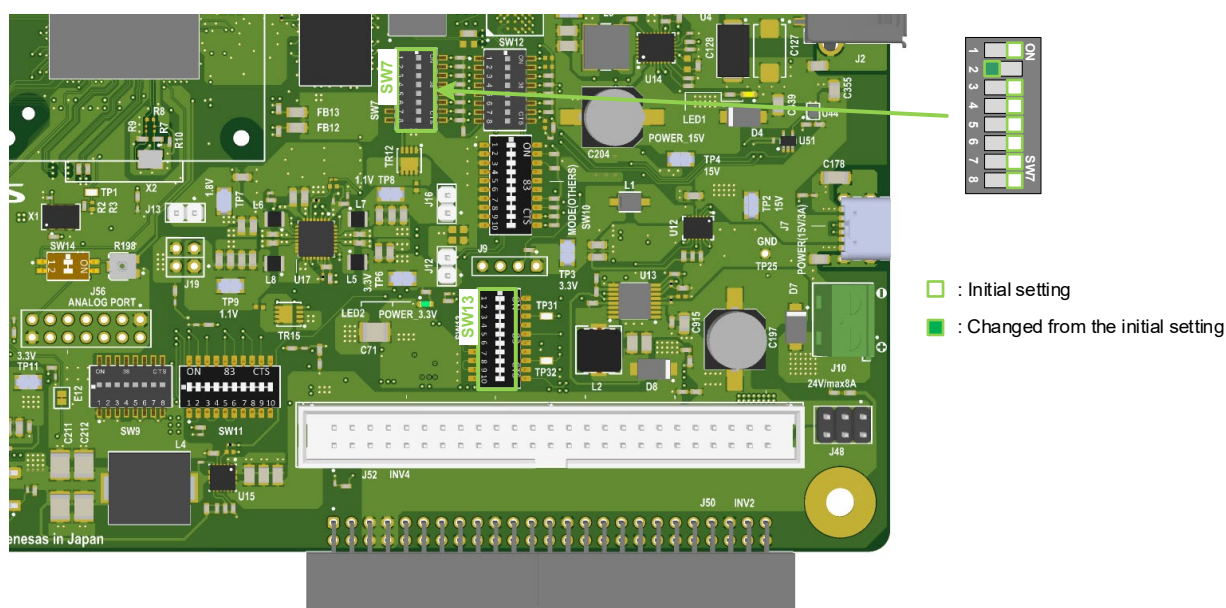


Figure 7-26 Switch Settings When Using the GPIO Connector (J55)

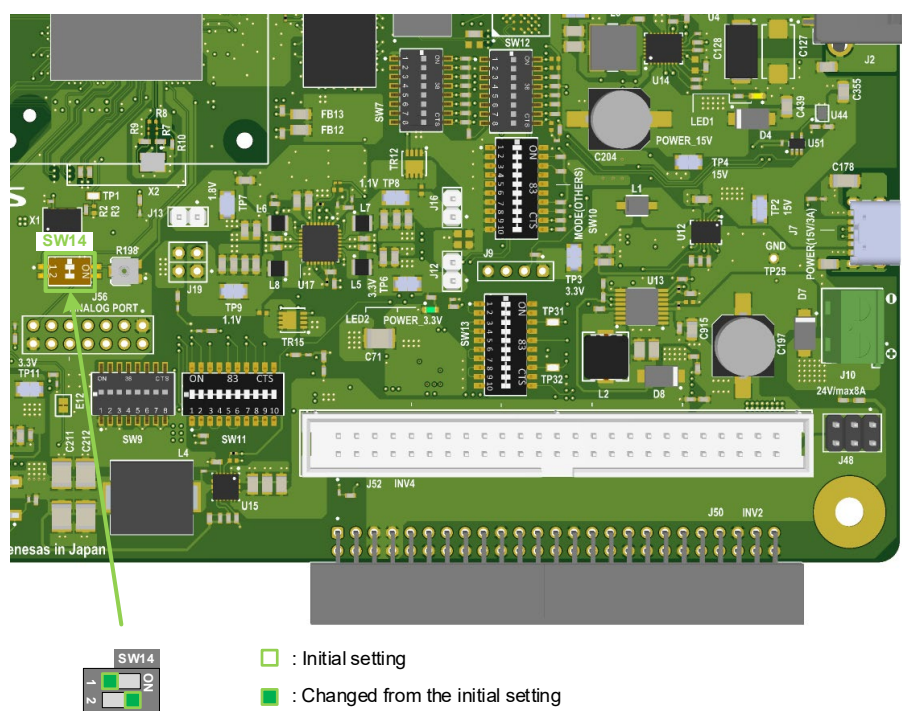


Figure 7-27 Switch Settings When Using the ADC Connector (J56)

7.20 Test Points

This board is equipped with the test points listed in Table 7-40 and Figure 7-28 for monitoring power supply lines and other signals. Only pads are provided for all test points and components are not mounted.

Table 7-40 List of Test Points

Reference	Description	Reference	Description
TP1	EXTCLKIN	TP17	ESC_LINKACT0 (P08_3)
TP2	cVBUS	TP18	ESC_LINKACT1 (P08_4)
TP3	P3V3_USB_PD	TP19	ESC_LINKACT2 (P09_7)
TP4	P15V	TP20	USER_LED0 (P13_3)
TP5	P12V	TP21	USER_LED1 (P13_5)
TP6	p3v3	TP22	USER_LED2 (P10_2)
TP7	p1v8	TP23	USER_LED3 (P10_3)
TP8	p1v1_Q	TP24	GND
TP9	p1v1	TP25	GND
TP10	p1v8_LDO	TP26	GND
TP11	INV_3V3	TP27	GND
TP12	ETH_VDD10	TP28	p5v0
TP13	ETH_VDD25	TP29	p3v3_LDO
TP14	PCIE3V3	TP30	P13_2_SD1_IOVS
TP15	ESC_LED RUN (P10_1)	TP31	P15_4_ESC_I2CCLK
TP16	ESC_LED ERR (P06_3)	TP32	P15_5_ESC_I2CDATA

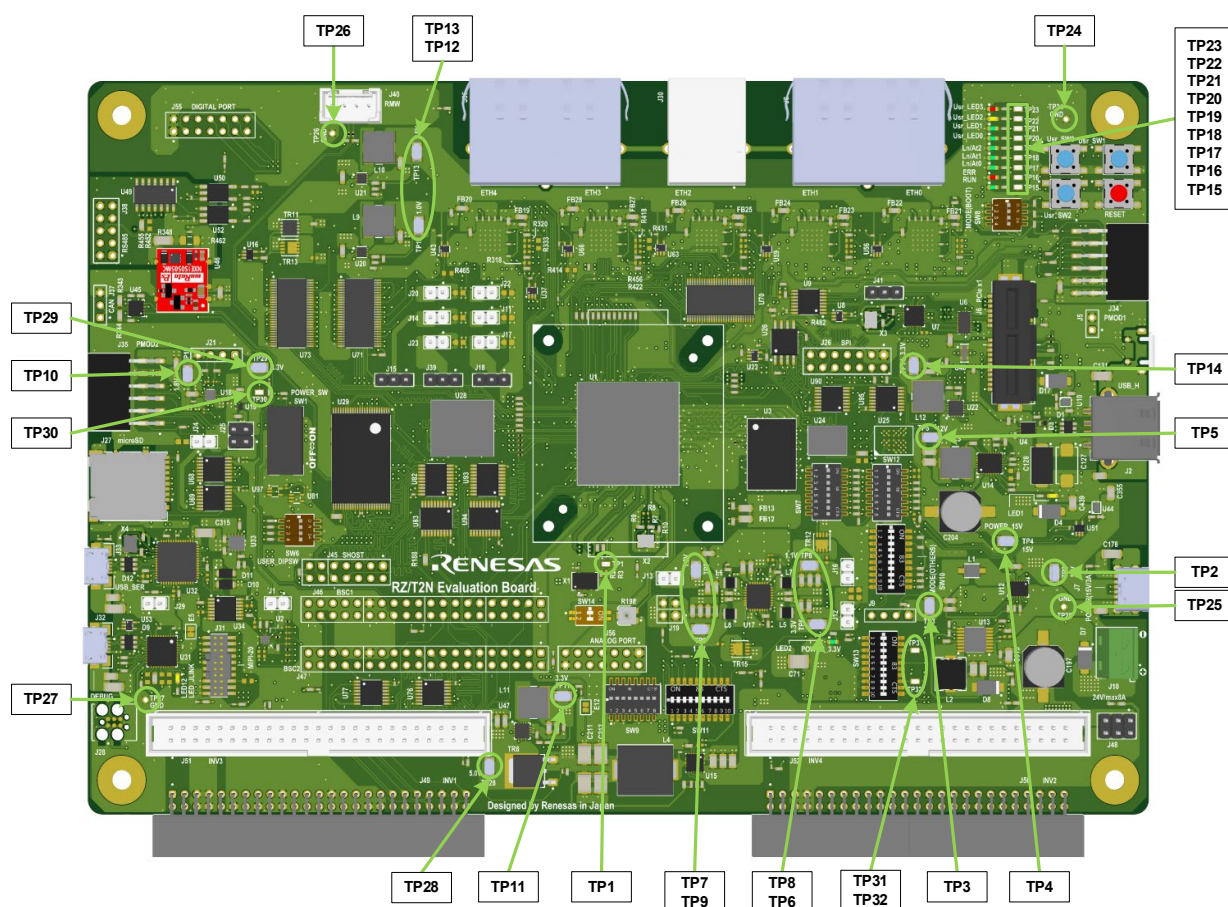


Figure 7-28 Arrangement of the Test Points (Top Side)

8. Certifications

This board meets the following certifications/standards. See the beginning of this manual for the disclaimer and precautions.

8.1 EMC/EMI Standards

- FCC Notice (Class A)



This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

NOTE- This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/television technician for help.

- Innovation, Science and Economic Development Canada ICES-003 Compliance:
CAN ICES-3 (A)/NMB-3(A)

- CE Class A (EMC)



This product is herewith confirmed to comply with the requirements set out in the Council Directives on the Approximation of the laws of the Member States relating to Electromagnetic Compatibility Directive 2014/30/EU.

Warning – This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

- UKCA Class A (EMC)



This product is in conformity with the following relevant UK Statutory Instrument(s) (and its amendments): 2016 No. 1091 Electromagnetic Compatibility Regulations 2016.

Warning – This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

8.2 Material Selection, Waste, Recycling and Disposal Standards

- EU RoHS
- China SJ/T 113642014, 10-year environmental protection use period.
- WEEE Directive (2012/19/EU) & The Waste Electrical and Electronic Equipment Regulations 2013



The WEEE (Waste Electrical and Electronic Equipment) regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union.

This equipment (including all accessories) is not intended for household use. After use the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled and disposed of in an environmentally sound manner.

Renesas Electronics Europe GmbH can take back end of life equipment. Register for this service at;
<https://www.renesas.com/eu/en/support/regional-customer-support/weee>

8.3 Safety Standards

- UL 94V-0

9. Design and Manufacturing Information

The design and manufacturing information for this board is available in the “RZ/T2N Evaluation Board Design Package” available on renesas.com/rzt2n-evk

- Design package file name: rzt2n-evaluation-board-v1-designpackage.zip
- Design package contents

Table 9-1 Contents of the RZ/T2N Evaluation Board Design Package

File Type	Description	File Name or Folder Name
File (PDF)	Schematics	rzt2n-evaluation-board-v1-schematic
File (PDF)	Mechanical drawings	rzt2n-evaluation-board-v1-mechdwg
File (PDF)	3D drawings	rzt2n-evaluation-board-v1-3d
File (xlsx)	Bill of materials (BOM)	rzt2n-evaluation-board-v1-BOM
Folder (zip)	Manufacturing files	rzt2n-evaluation-board-Manufacturing Files
Folder (zip)	Design files	rzt2n-evaluation-board-Design Files

10. Website and Support

Visit the following URLs to learn about the kit and the RZ family of MPUs, download tools and documentation, and get support.

RZ/T2N Evaluation Board Resources	renesas.com/rzt2n-evk
RZ Product Information	renesas.com/rz
Renesas Support	renesas.com/support

11. Appendix

The arrangements of individual components on this board are shown in this appendix.

Revision History	RZ/T2N Group RZ/T2N Evaluation Board Manual
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Rev.	Date	Description	
		Page	Summary
1.00	Nov.4.26	—	First edition issued

RZ/T2N Group
RZ/T2N Evaluation Board Manual

Publication Date: Rev.1.00 Nov.4.26

Published by: Renesas Electronics Corporation

RZ/T2N Group



Renesas Electronics Corporation

R20UT5574EJ0100