SLG46801 In-System Programming Guide

Introduction

This document describes the in-system programming procedures for the SLG46801.

The SLG46801 device integrates commonly used mixed-signal functions with multi-time programmable (MTP) memory to provide a low-power, highly flexible solution for analog signal processing and mixed-signal applications. The non-volatile memory (NVM) used in the device is multi-time programmable with the I2C serial interface.

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1. Hardware Requirements

1.1 Pinout and Signals

Four pins are required to program the SLG46801: VDD, GND, SCL, and SDA.

The VDD pin requires a voltage in the range of 1.71 V to 5.5 V for programming (write) operations and verification (read) operations. The SCL and SDA pins use standard I²C signaling. I²C Fast-Mode Plus speed (1 MHz) is supported for NVM read operations, and I²C Fast-Mode speed (400 kHz) is supported for NVM write operations. For timing characteristics of the signals on these pins, refer to Table 1.

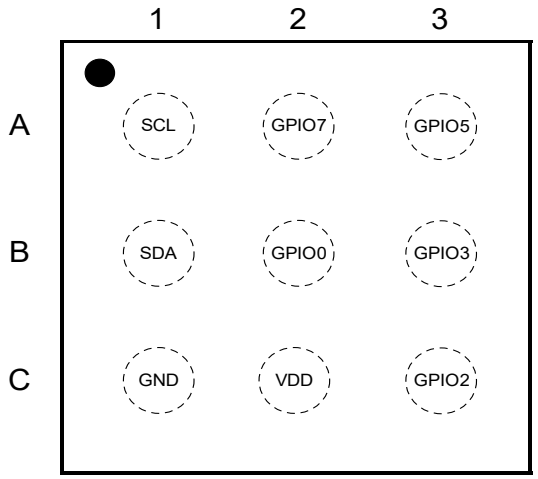


Figure 1. WLCSP-9 Pin Configuration

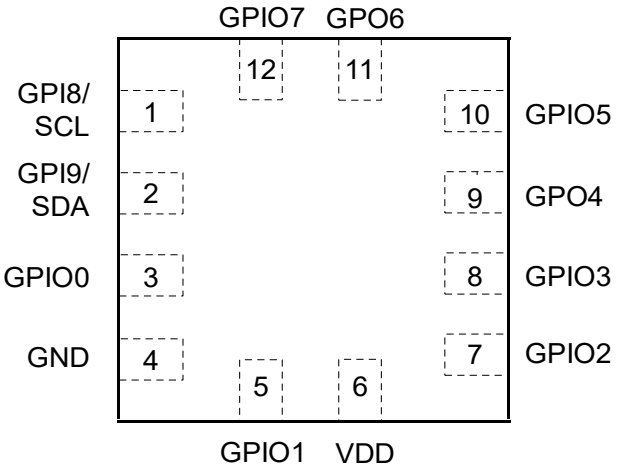


Figure 2. STQFN-12 Pin Configuration

Table 1. I²C Specifications

Parameter	Symbol	Conditions	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}	-	-	400	-	1000	kHz
Hold Time for (Repeated) START Condition	t_{HD_STA}	-	600	-	260	-	ns
SCL Clock, LOW Period	t_{LOW}	-	1300	-	500	-	ns
SCL Clock, HIGH Period	t_{HIGH}	-	600	-	260	-	ns
Set-up Time for Repeated START Condition	t_{SU_STA}	-	600	-	260	-	ns
Data Hold Time	t_{HD_DAT}	-	0	-	0	-	ns
		Low-voltage Logic Input Mode[1]	447	-	N/A	N/A	
Data Set-up Time	t_{SU_DAT}		100	-	40.85	-	ns
		Low-voltage Logic Input Mode[1]	583	-	N/A	N/A	
SCL, SDA Rise Time	t_R	-	-	300	--	120	ns
SCL, SDA Fall Time	t_F	-	-	300	--	120	ns
Set-up Time for STOP Condition	t_{SU_STO}	-	600	-	260	-	ns
Bus Free Time between STOP and START Conditions	t_{BUF}	-	1300	-	500	-	ns
Capacitive Load for Each Bus Line	C_b	-	-	400	-	400	pF
Data Valid Time	t_{VD_DAT}	-	-	900	-	450	ns
Data Valid Acknowledge Time	t_{VD_ACK}	-	-	900	-	450	ns

1. Does not meet Standard I2C Specifications

2. Programming Algorithm for NVM Configuration Register Space

The SLG46801 programming algorithm for the NVM configuration space consists of a series of I²C Sequential Write commands, each of which programs one 16-byte page of NVM memory.

Data programmed as 1 cannot be reprogrammed as 0 without page erase operation. Each byte can be programmed only once without erasure.

Note: The functionality of the device is based on the registers. The registers are not reloaded from the NVM until power is cycled, or a reset command is issued.

The SLG46801 can be programmed either with (Figure 3) or without (Figure 4) an acknowledge polling routine. The acknowledge polling routine is provided to optimize time-sensitive applications that prefer not to wait for the fixed maximum write cycle time (t_{WR}). This method allows the application to determine immediately when the NVM write cycle has completed, enabling a subsequent operation to be started without delay.

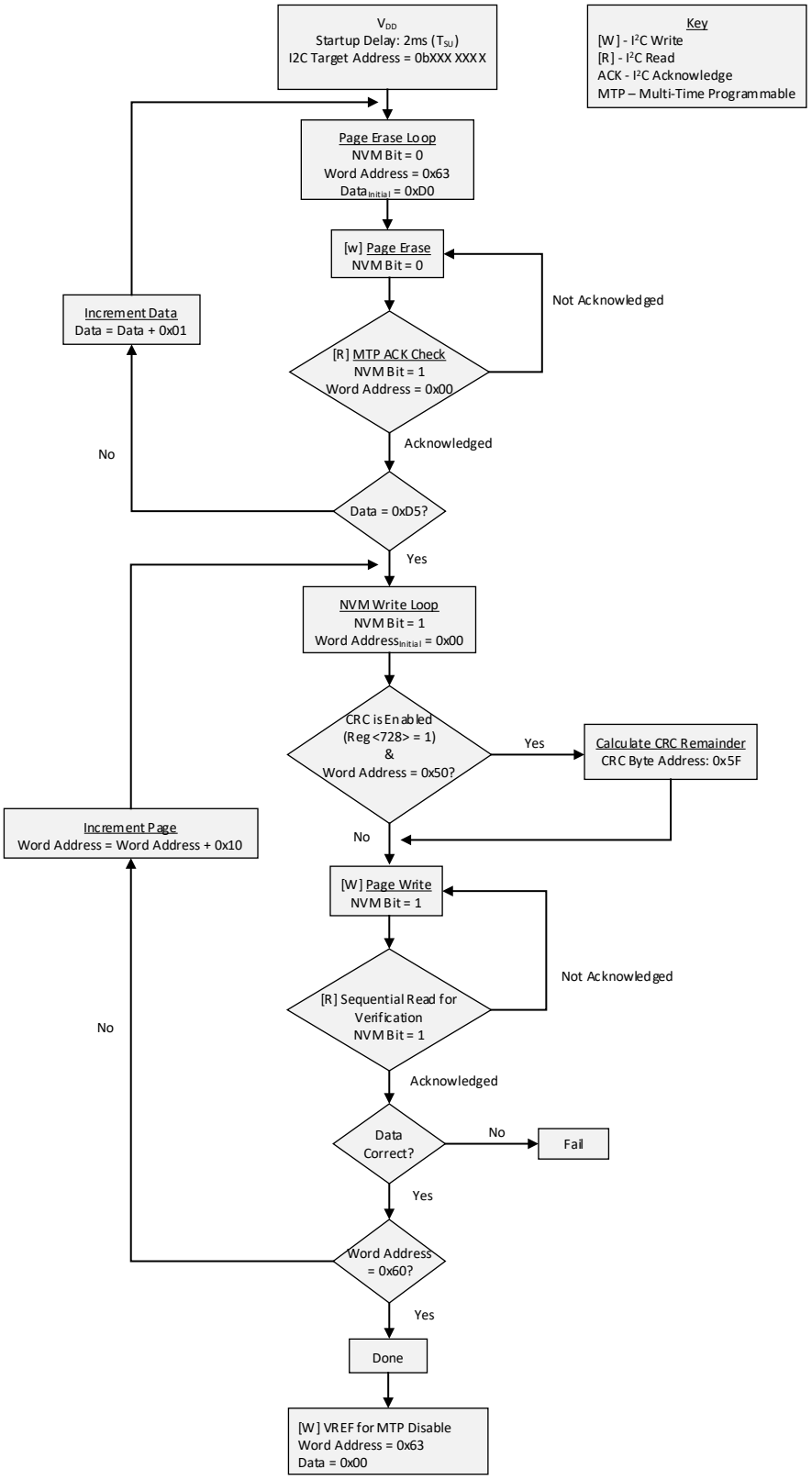


Figure 3. Flowchart for Programming NVM with Acknowledge Polling

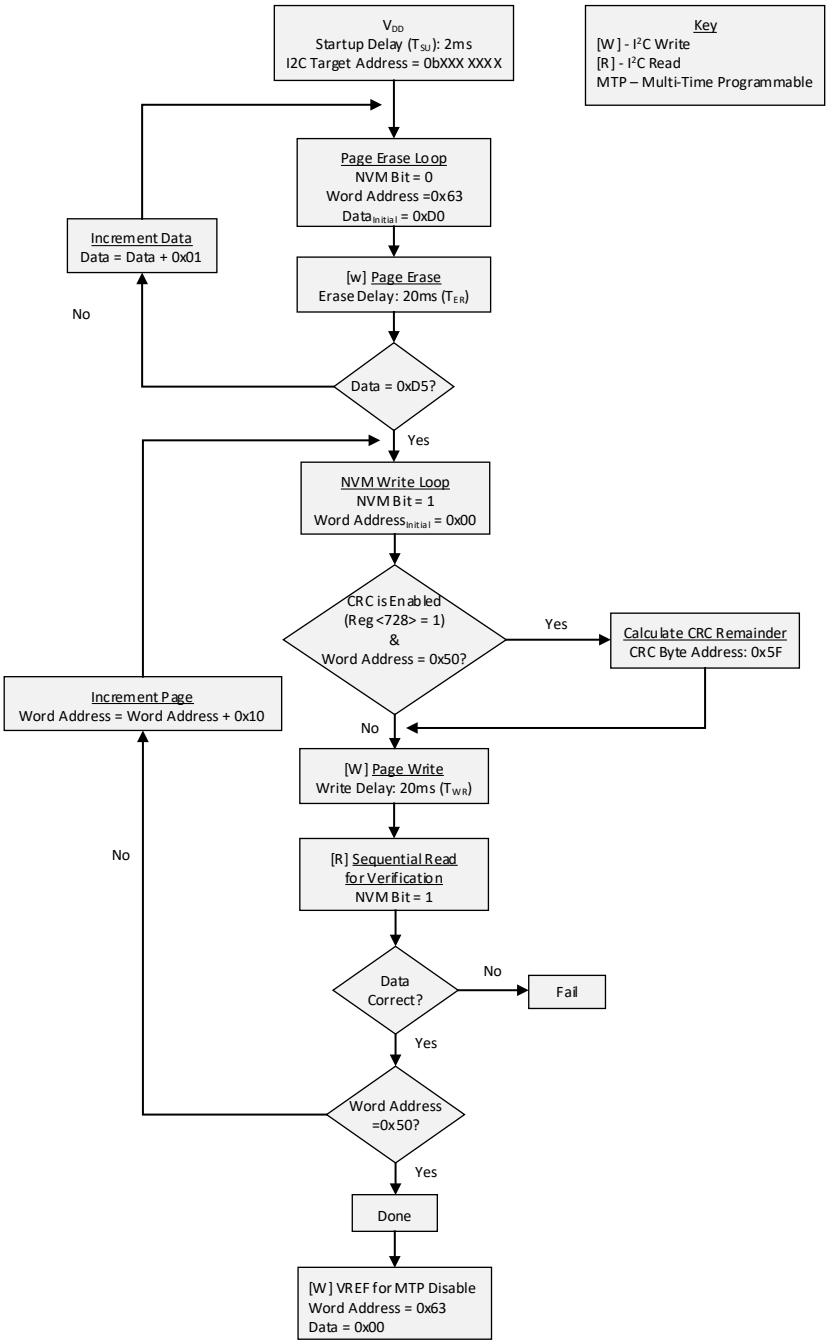


Figure 4. Flowchart for Programming NVM without Acknowledge Polling

3. I²C Signal Specification

3.1 Target Address

Each command of the I²C Serial Communication begins with a target address. After the START condition, the next seven bits form the 7-bit target address as shown in Figure 5, which is selected using internal registers in the device. The two LSBs of the 7-bit target address can also be selected externally through GPIO0 at POR. All four combinations of the two LSBs can be achieved by connecting an external resistor of the corresponding value to GPIO0, as follows:

00: Floating;

01: 3 MΩ to GND;

10: 910 kΩ to GND;

11: 250 kΩ to GND.

The 7-bit device address in the SLG46801 can be stored on an unprotected page (register 0x5C), which allows modification during reprogramming based on the design lock settings, or it can be stored in a protected page, where it cannot be modified further, regardless of the design lock settings.

As shown in Figure 5, setting the NVM Access bit to 1 selects writing to or reading from NVM while setting the bit to 0 enables writing to or reading from register/volatile memory.

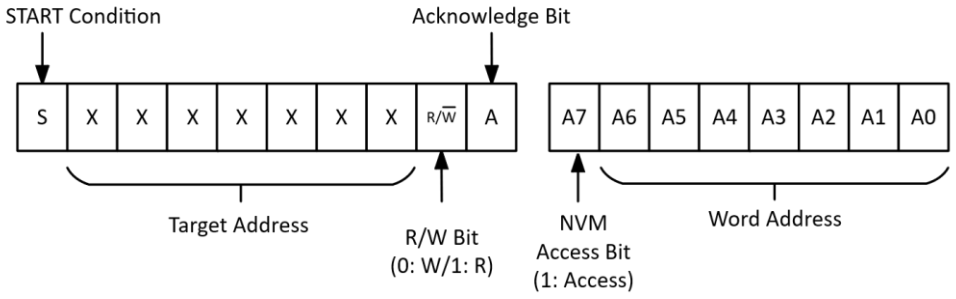


Figure 5. Page Write Command Example

3.2 Commands

3.2.1 Write Command

Upon receipt of the correct I²C target address reprogramming access to NVM is possible by setting the NVM Access bit to 1 in the word address, which allows serial NVM data to be written for a single page only. SLG46801 sends an ACK once it receives both I²C target address and word address, after which it is ready to receive page data, consisting of 16 sequential writes of 8-bit data words. The SLG46801 also responds with an ACK after each data word is received. The addressing device, such as a bus controller, must then terminate the write operation with a stop condition after all page data has been written. At that time, GreenPAK enters an internally self-timed write cycle, which is completed within t_{WR} = 20 ms (max). While the data is being written to the NVM memory array, all inputs, outputs, internal logic, and I²C access to the register data remain operational and valid.

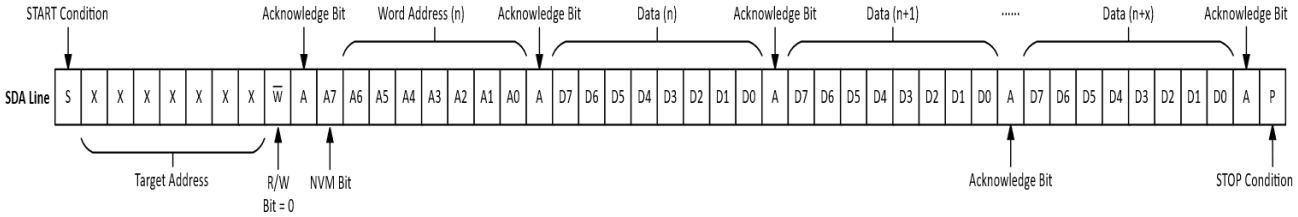


Figure 6. Random Sequential Write Command

3.2.2 Verify Command

The Random Sequential Read command can be used for verification. The command starts with a START condition, followed by the 7-bit target address with RW = 0 (indicating a write command). After the SLG46801 generates an ACK bit, the I²C controller sends the Word Address with NVM Access Bit selected as 1 to set the internal address pointer of NVM memory. After another ACK bit from the SLG46801, the I²C controller generates a Repeated START (Sr) condition without issuing a STOP condition, which keeps the internal address pointer unchanged in preparation for the next command. After initiating the Repeated START condition, the I²C controller sends the same 7-bit target address with the RW bit set to 1. After the SLG46801 issues an ACK bit, it transmits the data byte from the register indicated by the internal address pointer. When the data transmission is complete, the I²C controller issues a Not Acknowledge (NACK) bit before generating a STOP condition.

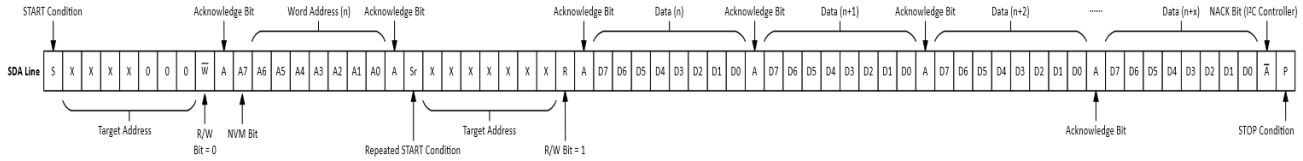


Figure 7. Random Sequential Read Command

3.2.3 Erase Command

The erase procedure allows an individual page in the NVM memory to be erased to accommodate a modified design. The erase procedure starts with a simple I²C write command to the ERSR register in register/volatile memory i:e NVM Access Bit in word address is set to 0. When the ERSE bits are set in the ERSR register, the device starts a self-timed erase cycle, which is completed within a maximum of t_{ER} = 20 ms (max). Changing the state of the ERSR register is accomplished using a byte write sequence that meets the requirements outlined in this section. The ERSE register address is 0x63.

Table 2. Erase Register Bit Format

	b7	b6	b5	b4	b3	b2	b1	b0
Page Erase Register	ERSE2	ERSE1	ERSE0	MTP V_{REF} Enable	-	ERSEB2	ERSEB1	ERSEB0

Table 3. Erase Register Bit Function Description

Bit	Name		Type	Description
7	ERSE2	Erase Enable	W	Setting bits [7:5] to '110' will start the internal erase cycle on the page defined by bits[2:0]
6	ERSE1		W	
5	ERSE0		W	
4	MTP V_{REF}	-	W	0: Disable, 1: Enable
3	-	-	-	-
2	ERSEB2	Page Selection for Erase	W	Defines the page address to be erased.
1	ERSEB1		W	
0	ERSEB0		W	

Following receipt of the correct target address and ERSE register address, the SLG46801 sends an ACK. The device is then ready to receive ERSE register data. The SLG46801 responds with a non-compliant I²C ACK after the ERSE register data word is received. To reprogram the device, MTP V_{REF} bit must be enabled in the ERSE register data; otherwise, the device is not reprogrammed. The addressing device, such as a bus controller, must then terminate the write operation with a Stop condition. At that time, GreenPAK enters an internally self-timed

erase cycle, which is completed within t_{ER} = 20 ms (max). While the data is being written to the memory array, all inputs, outputs, internal logic, and I^2C access to the register data remain operational and valid. After the erase operation is complete, the ERSE bits are automatically reset to 0, whereas the MTP V_{REF} Enable must be disabled manually using a simple I^2C command.

3.3 CRC Remainder

Cyclic Redundancy Check (CRC) is a powerful technique used to detect errors in register/NVM memory during startup to ensure proper device operation. In theory, the CRC algorithm in the SLG46801 treats the entire register/NVM data “Pages 0–5” as a binary number and divides it by another binary number, referred to as the polynomial. The remainder of this division is called the CRC remainder, or checksum, and is stored in register address 0x5F.

During startup, if enabled, the SLG46801 CRC algorithm divides the entire register/NVM data “Pages 0–5” by the polynomial and evaluates the division result. If the result is zero, the SLG46801 releases POR and operates normally; otherwise, it enters fault mode and sets the corresponding CRC flag in register byte address 0x6B.

CRC checking can be enabled by setting register bit [728] (register address 0x5B) to 1. When enabled, the CRC remainder must be recalculated whenever the register data in Pages 0–5 changes and written to Page 5 (register address 0x5F) during reprogramming of the SLG46801.

3.4 Reset

The user can do an immediate reset using one of the following methods to apply the changes to the design in NVM.

- Hard Power Reset – Power down the device and then power it back on.
- Soft Reset – I^2C write command to register address 0x5A with data value of 0x01 in register memory.

4. Service Pages

GreenPAK’s 1K bits of internal NVM memory are divided into eight pages, each containing 16 bytes. Pages six and seven within the 1K-bit NVM register memory space contain reserved information that is preprogrammed during final device testing and protected from errors by using individual page CRC. The contents of these pages can be read, and only a limited number of bytes in page six can be written by the user via the register memory, because they provide access to device reprogramming. Most of the NVM memory on these pages is used exclusively during chip manufacturing and testing procedures. After production, these bits can be ignored and not used during normal operation.

5. Terms and Definitions

ACK	Acknowledge Bit
ERSE	Erase Enable
ERSR	Erase Register
IO	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
NPR	Non-Volatile Memory Read/Write/Erase Protection
NVM	Non-Volatile Memory
PRL	Protect Lock Bit
R/W	Read/Write
RPR	Register Read/Write Protection

SCL	I^2C Clock Input
SDA	I^2C Data Input/Output
WPB	Write Protect Block Bits
WPR	Write Protection Register
WPRE	Write Protect Register Enable
CRC	Cyclic Redundancy Check

6. Revision History

Revision	Date	Description
1.00	May 29, 2026	Initial Release
1.01	June 22, 2026	Updated Document