In-System Programming Guide

SLG47004

ISPG-SLG47004

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1 Terms and Definitions

ACK	Acknowledge Bit
ERSE	Erase Enable
ERSR	Erase Register
IO	Input/Output
IP	Intellectual Property
LSB	Least Significant Bit
MSB	Most Significant Bit
MTP	Multi-Time Programmable
NPR	Non-Volatile Memory Protection Register
NVM	Non-Volatile Memory
PRL	Protect Lock Bit
R/W	Read/Write
RPR	Register Read/Write Protection
SCL	I^2C Clock Input
SDA	I^2C Data Input/Output
WPB	Write Protect Block Bits
WPR	Write Protection Register
WPRE	Write Protect Register Enable

2 Introduction

This document describes the in-system programming procedures for the SLG47004.

3 Hardware Requirements

3.1 Pinout and Signals

Four pins are required to program the SLG47004: V_{DD}, GND, SCL, and SDA.

The V_{DD} pin requires a voltage ranging from 2.5 V to 5.5 V for Programming (Write) operations, and 2.4 V to 5.5 V for Verification (Read) operations.

The SCL and SDA pins are defined to be standard I²C signaling. I²C Fast Mode Plus speed (1 MHz) NVM read and I²C Fast Mode speed (400 kHz) NVM write communication is supported for these devices. Refer to Table 1 for the signal timing characteristics of these pins.

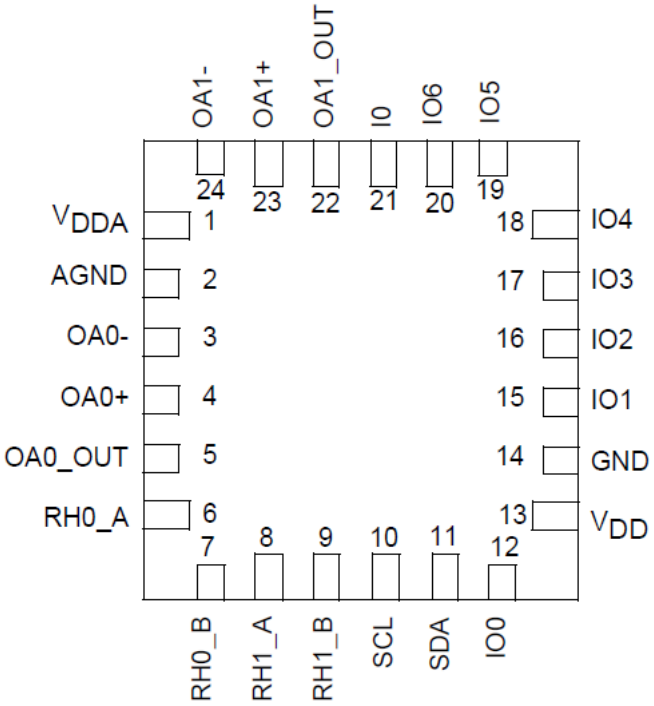

Figure 1: STQFN-24 Pin Configuration

Table 1: I²C Specifications

Symbol	Parameter	Condition	Fast-Mode			Fast-Mode Plus			Unit
			Min	Typ	Max	Min	Typ	Max	
F_{SCL}	Clock Frequency, SCL	V_{DD} = 2.4 V to 5.5 V	--	--	400	--	--	1000	kHz
t_{LOW}	Clock Pulse Width Low	V_{DD} = 2.4 V to 5.5 V	1300	--	--	500	--	--	ns
t_{HIGH}	Clock Pulse Width High	V_{DD} = 2.4 V to 5.5 V	600	--	--	260	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = 2.4 V to 5.5 V	--	--	50	--	--	50	ns
t_{AA}	Clock Low to Data Out Valid	V_{DD} = 2.4 V to 5.5 V	--	--	900	--	--	450	ns
t_{BUF}	Bus Free Time between Stop and Start	V_{DD} = 2.4 V to 5.5 V	1300	--	--	500	--	--	ns
t_{HD_STA}	Start Hold Time	V_{DD} = 2.4 V to 5.5 V	600	--	--	260	--	--	ns
t_{SU_STA}	Start Set-up Time	V_{DD} = 2.4 V to 5.5 V	600	--	--	260	--	--	ns
t_{HD_DAT}	Data Hold Time	V_{DD} = 2.4 V to 5.5 V	0	--	--	0	--	--	ns
t_{SU_DAT}	Data Set-up Time	V_{DD} = 2.4 V to 5.5 V	100	--	--	50	--	--	ns
t_R	Inputs Rise Time	V_{DD} = 2.4 V to 5.5 V	--	--	300	--	--	120	ns
t_F	Inputs Fall Time	V_{DD} = 2.4 V to 5.5 V	--	--	300	--	--	120	ns
t_{SU_STD}	Stop Set-up Time	V_{DD} = 2.4 V to 5.5 V	600	--	--	260	--	--	ns
t_{DH}	Data Out Hold Time	V_{DD} = 2.4 V to 5.5 V	50	--	--	50	--	--	ns

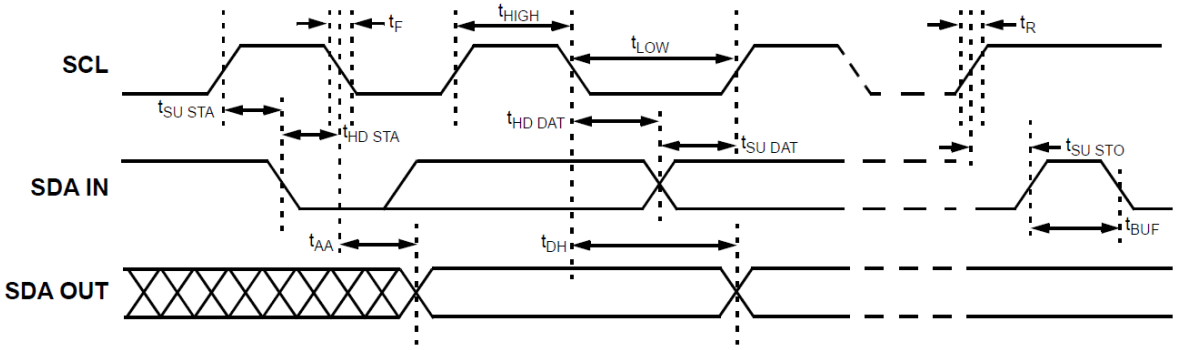

Figure 2: I²C General Timing Characteristics

4 I²C Signal Specification

4.1 Addressing

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 3.

After the Start bit, the first four bits make up the control code. Each bit in the control code can be sourced independently from registers [1019:1016] or can be defined externally by IO4, IO3, IO2, and IO1. If external GPIO source is selected, the LSB of the control code is defined by the value of IO1, while the MSB is defined by the value of IO4. The address source (either register bit or PIN) for each bit in the control code is defined by registers [1023:1020]. This provides flexibility on the chip level when addressing this device and other devices on the same I²C bus. **The default control code is 0001 and is selected by registers [1019:1016]**.

The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the I²C command. For the SLG47004, these 3 bits determine whether the I²C command accesses the Register Data Configuration, NVM Data Configuration, or EEPROM address spaces, as defined in Figure 6. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting a Read command and a "0" selecting a Write command.

This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

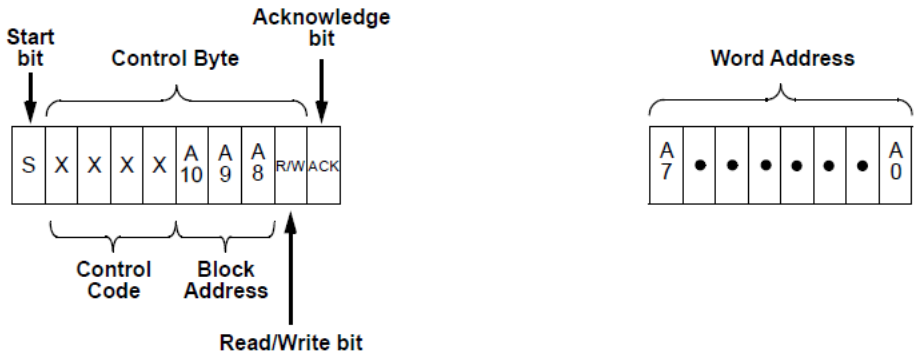

Figure 3: Page Write Command

4.2 Commands

4.2.1 Write Command

To program the SLG47004, a 16-byte I²C page write command can be sent to configure the MTP memory. Upon receipt of a proper Control Byte and Word Address, the SLG47004 will send an ACK. The device will then be ready to receive page data, which is 16 sequential writes of 8-bit data words. The SLG47004 will respond with an ACK after each data word is received. After all page data is written, the addressing device, such as a Bus Controller, must then terminate the write operation with a Stop condition. At that time, the SLG47004 will enter an internal, self-timed write cycle, which will be completed within t_{WR} = 20 ms (max). While the data is being written into the NVM Memory Array, all inputs, outputs, internal logic, and I²C access to the Register Data Configuration address space will be operational/valid.

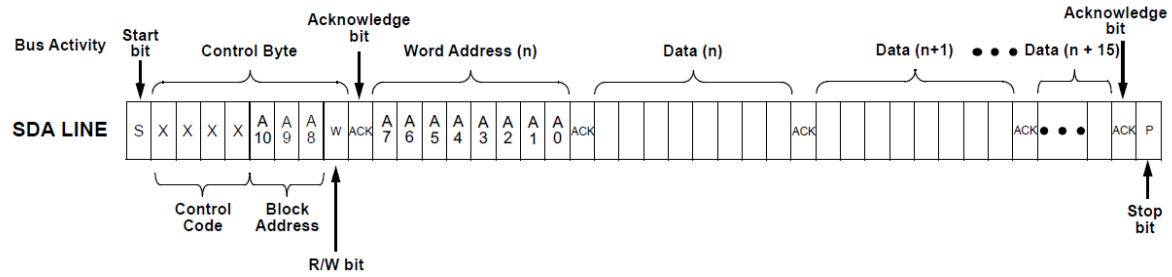

Figure 4: Page Write Command Example

4.2.2 Verify Command

The Random Sequential Read command can be used for verification. The command starts with a Control Byte (with R/W bit set to "0", indicating a write command) and a Word Address to set the internal byte address. These bytes are followed by another start bit with the same Control Byte (with R/W bit set to “1”, indicating a read command). The start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the start bit, the Bus Controller issues a second Control Byte with the R/W bit set to "1", after which the SLG47004 issues an Acknowledge bit, followed by the requested eight data bits. Once the SLG47004 transmits the first data byte, the Bus Controller issues an Acknowledge bit. The Bus Controller can continue reading sequential bytes of data by sending additional Acknowledge bits or it can terminate the command with a Stop condition.

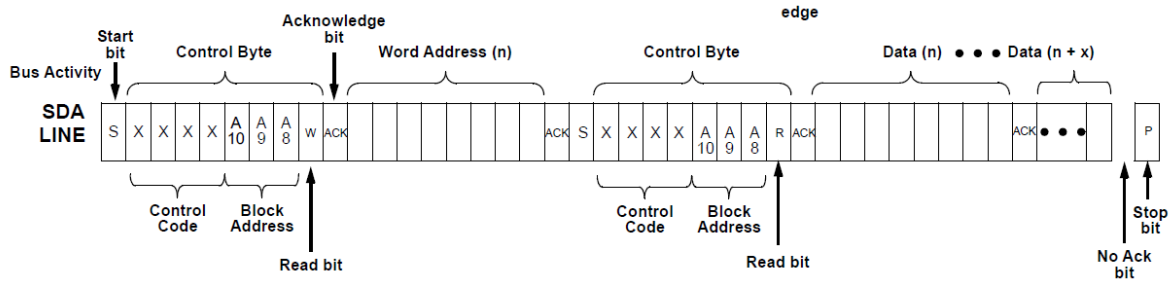

Figure 5: Random Sequential Read Command

4.2.3 Erase Command

The erase scheme allows a 16-byte page within the MTP memory to be erased by modifying the contents of the Erase Register (ERSR) found at 0xE3. This erase command should be written to the Register Data Configuration address space as defined by Figure 6. In addition, this erase command can be configured to erase a page within either the 2 kbits of NVM or 2 kbits of EEPROM by setting ERSEB4 (register [1820]) in accordance with Table 3. The page can be selected by setting registers [1819:1816] (bits ERSEB0, ERSEB1, ERSEB2, ERSEB3 from Table 3) to match the desired page number shown in Figure 7. When registers [1823:1821] (bits ERSEB0, ERSEB1, ERSEB2 from Table 3) are set to “110” in the ERSR register, the device will start a self-timed erase cycle, which will complete in a maximum of t_{ER} = 20 ms (max).

Table 2: ERSR Register Format

	b7	b6	b5	b4	b3	b2	b1	b0
Page Erase Register	ERSE2	ERSE1	ERSE0	ERSEB4	ERSEB3	ERSEB2	ERSEB1	ERSEB0

Table 3: ERSR Register Bits Function Description

Bit	Name		Type	Description
7	ERSE2	Erase	W	000: erase disable;

Bit	Name		Type	Description
6	ERSE1	Enable	W	110: cause the NVM erase: full NVM (4k bits) erase for ERSCHIP = 1 if DIS_ERSCHIP = 0 or page erase for ERSCHIP = 0.
5	ERSE0		W	
4	ERSEB4	Page Selection for Erase	W	Define the page address, which will be erased: ERSB4 = 0 corresponds to the Upper 2K NVM used for chip configuration; ERSB4 = 1 corresponds to the 2-k emulated EEPROM.
3	ERSEB3		W	
2	ERSEB2		W	
1	ERSEB1		W	
0	ERSEB0		W	

Upon receipt of the proper Device Address and Erase Register Address, the SLG47004 will send an ACK. The device will then be ready to receive Erase Register data. The SLG47004 will respond with another I^2C ACK after the Erase Register data byte is received. The addressing device, such as a Bus Controller, must then terminate the write operation with a Stop condition. At that time, the SLG47004 will enter an internal, self-timed erase cycle, which will be completed within t_{ER} (max 20 ms). While the data is being erased within the MTP memory cells, all inputs, outputs, internal logic, and I^2C access to the Register Data Configuration address space will be operational/valid. After the erase has taken place, the contents of ERSE bits will be set to "0" automatically.

5 Memory Space

5.1 Memory Map

In the read and write command structure, there are a total of 11 bits that define the address for the I²C command: 3 bits for the Block Address and 8 bits for the Word Address.

As previously described, the Block Address determines which 2 kbits of address space to communicate with. The 2 kbits of Register Data Configuration cells configure the operation of the SLG47004 device. The 2 kbits of NVM Data Configuration correspond to the MTP cells that persist through power down events and are loaded into the Register Data Configuration cells upon power up. The 2 kbits of EEPROM are allocated for application-specific MTP memory storage.

The Word Address defines the specific bytes of data to access within these memory spaces. Figure 7 breaks these 2 kbits of data (256 bytes) into 16-byte pages. Refer to the register map found within the SLG47004's base die datasheet for more information.

	I²C Block Address			Memory Space	
Lowest I²C Address = 000h	A10 = 0	A9 = 0	A8 = 0	2 Kbits Register Data Configuration	
	A10 = 0	A9 = 0	A8 = 1	Not Used	
	A10 = 0	A9 = 1	A8 = 0	2 Kbits NVM Data Configuration	16 pages to configure GPAK
	A10 = 0	A9 = 1	A8 = 1	2 Kbits EEPROM	16 pages for emulated EEPROM
Highest I²C Address = 7FFh	A10 = 1	A9 = X	A8 = X	Not Used	

Figure 6: I²C Block Addressing

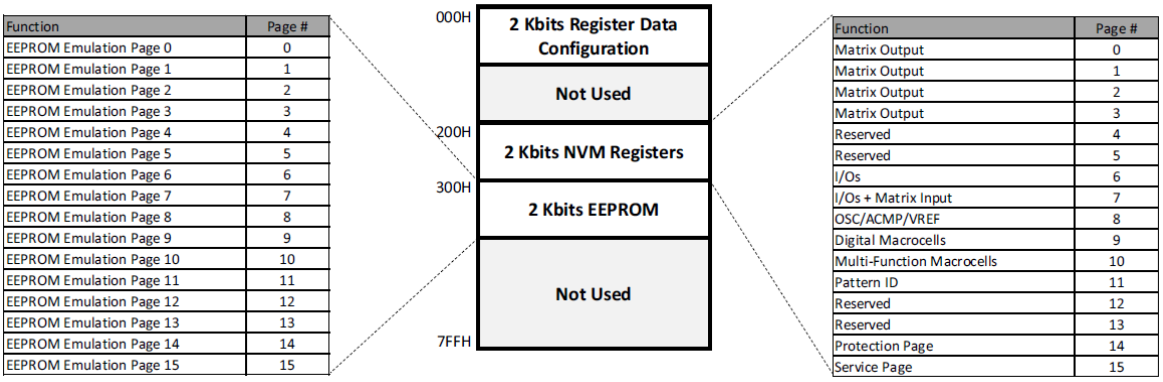

Figure 7: I²C Address Mapping

5.2 Pages

The SLG47004 I²C registers are separated into 3 address spaces: the SLG47004 Register Data Configuration, the NVM Data Configuration, and the EEPROM. Each of these address spaces contain

2048-bits of register data which equates to 16 pages of 16 bytes of data. The MTP IP limits I²C write and erase operations to 16-byte segments defined as pages for both the NVM Data Configuration and the EEPROM address spaces.

5.2.1 Protection Page

Page E (#14) contains the protection settings for the SLG47004. Individual registers determine whether the SLG47004's Register Data Configuration, NVM Data Configuration, and EEPROM address spaces can be accessed via I²C reads, writes, and erases. The Register Protection (RPR - 0xE0), NVM Protection (NPR - 0xE1), and EEPROM Protection (WPR - 0xE2) bytes can can be locked using the Protection Lock Bit (PRL - 0xE4).

The current configuration of the protection registers can be determined by performing a Random Read command of the desired register with the Block Adress set to "000". Modifying these registers using the Block Address of "000" will change the functionality of the protection scheme, but all configuration changes will be lost after a power cycle or soft reset.

Once the user determines the desired security settings for their project, they can erase and program Page E (#14) with the PRL set HIGH. Refer to section 5.2.1.4 for a description of this procedure. Note that the protection page configuration will not be active until the SLG47004 device is reset and the NVM Data Configuration contents are loaded into the SLG47004 Configuration Registers. This will cause the protection scheme to persist after a power cycle or soft reset.

5.2.1.1 Register Protection (RPR)/Rheostat Protection

The RPR register is located within address 0xE0. This register locks the ability to read, write, and erase the SLG47004's Register Data Configuration. These registers impact the "000" Block Address. In addition, this register locks the ability of the rheostats' program input to erase and program the current rheostat value into Page C (#12) and Page D (#13) of the MTP NVM Data Configuration address space. Refer to Table 4 for the format and Table 5 for the bit function descriptions.

Table 4: RPR Register Format

	b7	b6	b5	b4	b3	b2	b1	b0
RPR				RH_PRB	RPRB3	RPRB2	RPRB1	RPRB0

Table 5: RPR Register Bits Function Description

Bit	Name		Type	Description
4	RH_PRB	--	R/W	0: Program signal from connection matrix is enabled; 1: Program signal from connection matrix is disabled.
3:2	RPRB [3:2]	2k Register Write Selection Bits	R/W	00: 2k register data is unprotected for write; 01: 2k register data is partly protected for write; 10: 2k register data is fully protected for write.
1:0	RPRB [1:0]	2k Register Read Selection Bits	R/W	00: 2k register data is unprotected for read; 01: 2k register data is partly protected for read; 10: 2k register data is fully protected for read.

5.2.1.2 NVM Protection (NPR)

The NPR register is located within address 0xE1. This register locks the ability to read, write, and erase the NVM Configuration Data. These registers impact the "010" Block Address. Refer to Table 6 for the format and Table 7 for the bit function descriptions.

Table 6: NPR Format

	b7	b6	b5	b4	b3	b2	b1	b0
NPR							NPRB1	NPRB0

Table 7: NPR Bit Function Description

Bit	Name		Type	Description
1:0	NPRB [1:0]	2k NVM Configuration Selection Bits	R/W	00: 2k NVM Configuration data is unprotected for read and write/erase; 01: 2k NVM Configuration data is fully protected for read; 10: 2k NVM Configuration data is fully protected for write/erase; 11: 2k NVM Configuration data is fully protected for read and write/erase.

5.2.1.3 EEPROM Protection (WPR)

The SLG47004 utilizes a software scheme to lock portions of the EEPROM from write and erase operations. The WPR register is located within address 0xE2. This register impacts the “011” Block Address. Refer to Table 8 for the format and Table 9 for the bit function descriptions.

Table 8: WPR Register Format

	b7	b6	b5	b4	b3	b2	b1	b0
WPR						WPRE	WPB1	WPB0

Table 9: WPR Register Bits Function Description

Bit	Name		Type	Description
2	WPRE	Write Protect Register Enable	R/W	0: No Software Write Protection enabled (default); 1: Write Protection is set by the state of WPB [1:0] bits.
1:0	WPB [1:0]	Write Protect Block Bits	R/W	00: Upper quarter of emulated EEPROM is write protected (default); 01: Upper half of emulated EEPROM is write protected; 10: Upper 3/4 of emulated EEPROM is write protected; 11: Entire emulated EEPROM is write protected.

5.2.1.4 Protection Lock Bit (PRL)

The Protect Lock Bit can be used to permanently lock the current state of the RPR, NPR, and WPR protection registers. A logic “0” indicates that these protection registers can be modified, whereas a logic “1” indicates that they have been locked and can no longer be modified. The PRL register bit is located at register [1824] within 0xE4.

This bit blocks I^2C write access to these protection registers by locking the entire configuration of Page E (#14) within the NVM. To lock these registers, follow the procedure below:

1. Read and Store the Rheostat Tolerance Data Stored within 0xE6 to 0xE9 (optional).
2. Erase Page E (#14) within the NVM.
3. Program Page E (#14) within the NVM using the Desired Protection Settings (splice in the Rheostat Tolerance Data for 0xE6 to 0xE9).
4. Issue a Soft Reset using register [984] within 0x7B or Power Cycle the SLG47004 to Load the Protection Settings into the Configuration Registers. Note that the “Soft Reset” Feature is unavailable if the RPR is “Fully Protected for Write” (RPRB [3:2] = “10”).

If PRL is HIGH and the NVM is locked for I^2C writes and erases, this will permanently lock the protection settings.

Table 10: PRL Register Format

	b7	b6	b5	b4	b3	b2	b1	b0
PRL								PRL

Table 11: PRL Bit Function Description

Bit	Name		Type	Description
0	PRL	Protection Lock	R/W	0: RPR/WPR/NPR Settings can be Changed; 1: RPR/WPR/NPR Settings cannot be Changed.

5.2.2 Service Page

Page 8 (#8) and page F (#15) are both dedicated service pages within the NVM Data Configuration and SLG47004 Register Data Configuration address spaces. They contain reserved information that is preprogrammed onto the device during final test. The information on these pages can be read via I^2C, but they cannot be written or erased, since they are locked by Renesas Electronics using the Service Page Lock Bit (register [1944]). As these pages cannot be altered by the user, the programming algorithm skips all I^2C operation on these pages.

Many bits in the NVM chip remain unused during normal programming, as they are reserved for service needs and are exclusively utilized during chip manufacturing and testing procedures. After production, these bits are ignored and are never used in regular operations. Additionally, there are also bits responsible for storing the current initial state of macrocells and the current counter values. During verification and comparison processes, these bits may differ from the intended values, as they continuously change during real-time operation. Table 12 lists the bits that must be ignored while comparing the programmed chip.

Table 12: List of Bits to be Ignored (Removed Bits That are "0" in Software)

Address		Function
Byte	Register Bit	
51	655:652	Reserved
52	662, 657:656	Reserved
54	677:673	Reserved
6F~6E	891:883	Reserved
70	903:902	Reserved
71	911:910	Reserved
72	917:916	Reserved
73	926:924, 922:921	Reserved
8F~80	1151:1024	Reserved
CE~C4	1655:1568	Matrix inputs and Counted Values of CNT/DLY blocks
DF:DD	1791:1772	Reserved
E5	1839:1832	Reserved
EB~EA	1886:1872	Reserved
F2:F0	1943:1920	Reserved
F3	1947:1946	Reserved
F4	1959:1956	Reserved
F5	1963:1962	Reserved
F6	1975:1968	I^2C write mask bits
FE~F7	2039:1976	Service page

6 Programming Algorithm for NVM Configuration Register Space

The SLG47004 programming algorithm for the NVM Data Configuration address space consists of a series of sequential I^2C write and read commands. The MTP IP limits I^2C programming operations to 16-byte page writes.

Data “1” cannot be re-programmed as data “0” without first being erased. Each byte can only be programmed one time without erasure.

Note 1 The functionality of the device is based upon the SLG47004 Register Data Configuration. The NVM Data Configuration will not be reloaded from the NVM until power is cycled or a reset command is issued.

Special care should be taken when erasing and re-programming Page E (#14). The Rheostat Tolerance Data is stored within this page and should be read so that it can be inserted into the new byte sequence for programming into Page E (#14).

The SLG47004 can be programmed either with or without an acknowledge polling routine. The acknowledge polling routine is implemented to optimize time sensitive applications that would prefer not to wait the fixed maximum write cycle time (t_{WR}). This method allows the application to know instantly when the NVM write cycle has completed so a subsequent operation can start.

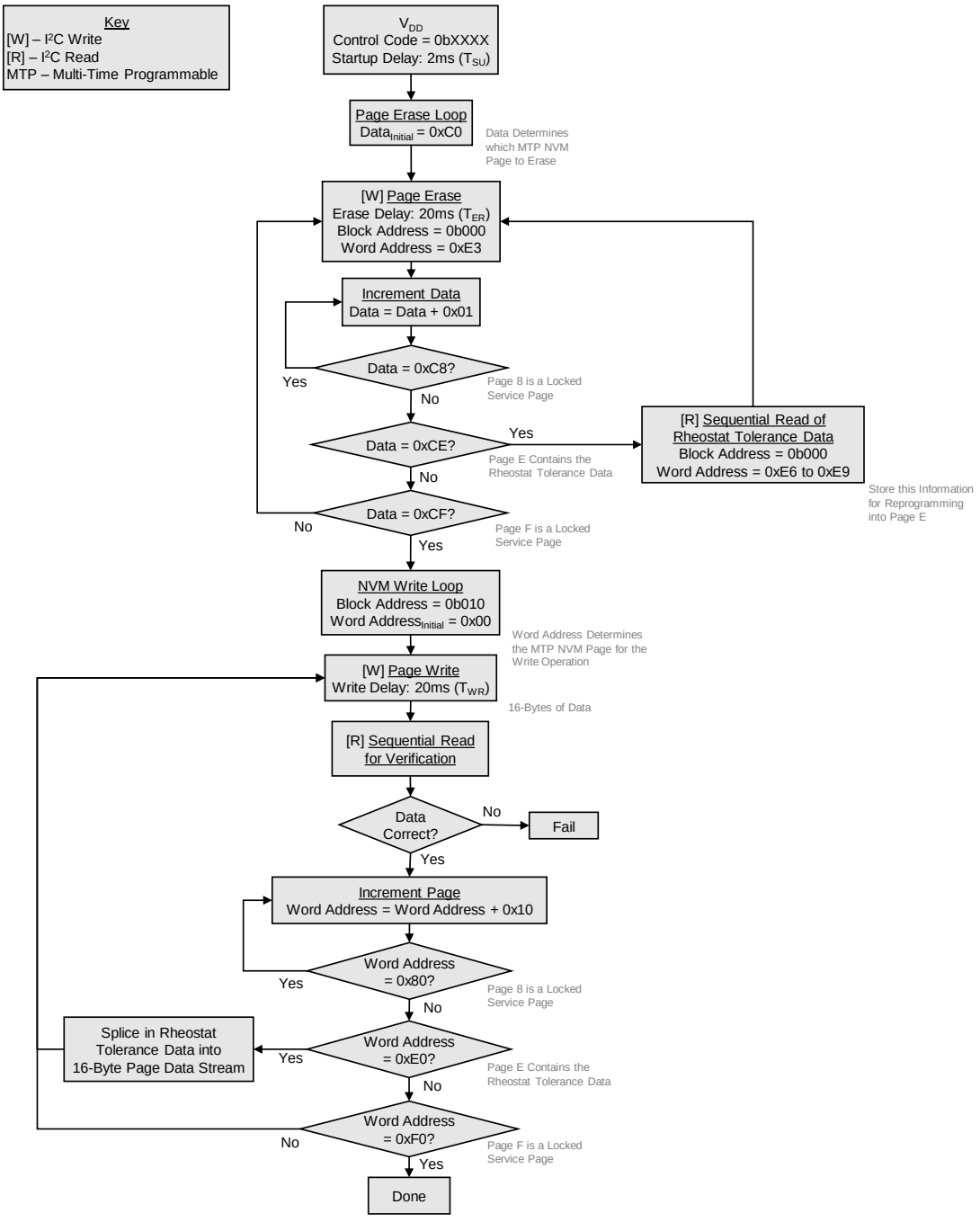

Figure 8: Flowchart for Programming NVM without Acknowledge Polling

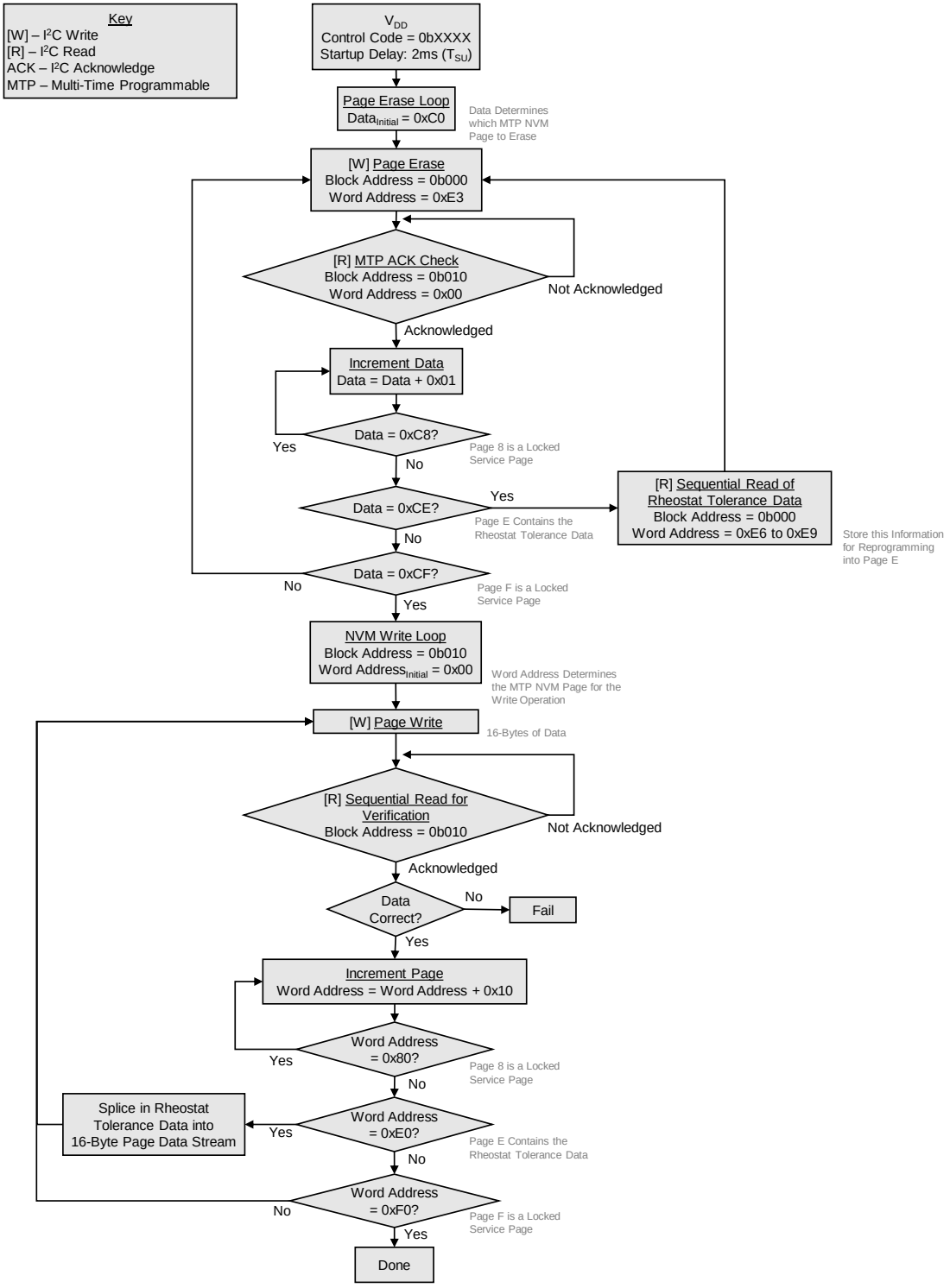

Figure 9: Flowchart for Programming NVM with Acknowledge Polling

7 Programming Algorithm for the Emulated EEPROM Space

The SLG47004 programming algorithm for the emulated EEPROM address space consists of a series of sequential I²C write and read commands. The MTP IP limits I²C programming operations to 16-byte page writes.

Data “1” cannot be re-programmed as data “0” without first being erased. Each byte can only be programmed one time without erasure.

Programming the emulated EEPROM follows a similar flow to that of the NVM with three differences:

- The Emulated EEPROM Block Address is “011” (in contrast with the “010” Block Adress of the NVM Data Configuration address space);
- With emulated EEPROM, all 16 pages are user accessible (no Service or Protection Pages);
- Rheostat Tolerance Data is stored in the NVM and does not require consideration in the EEPROM programming flow.

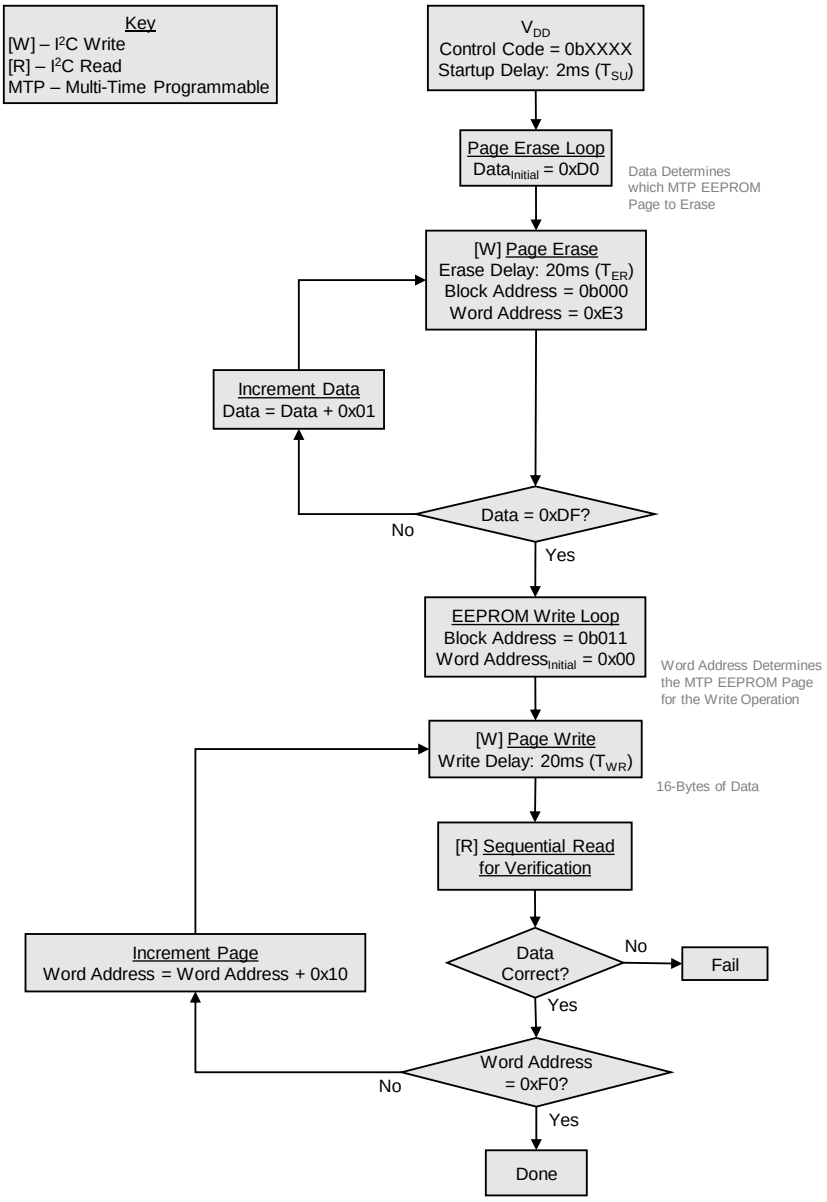

Figure 10: Flowchart for Programming EEPROM without Acknowledge Polling

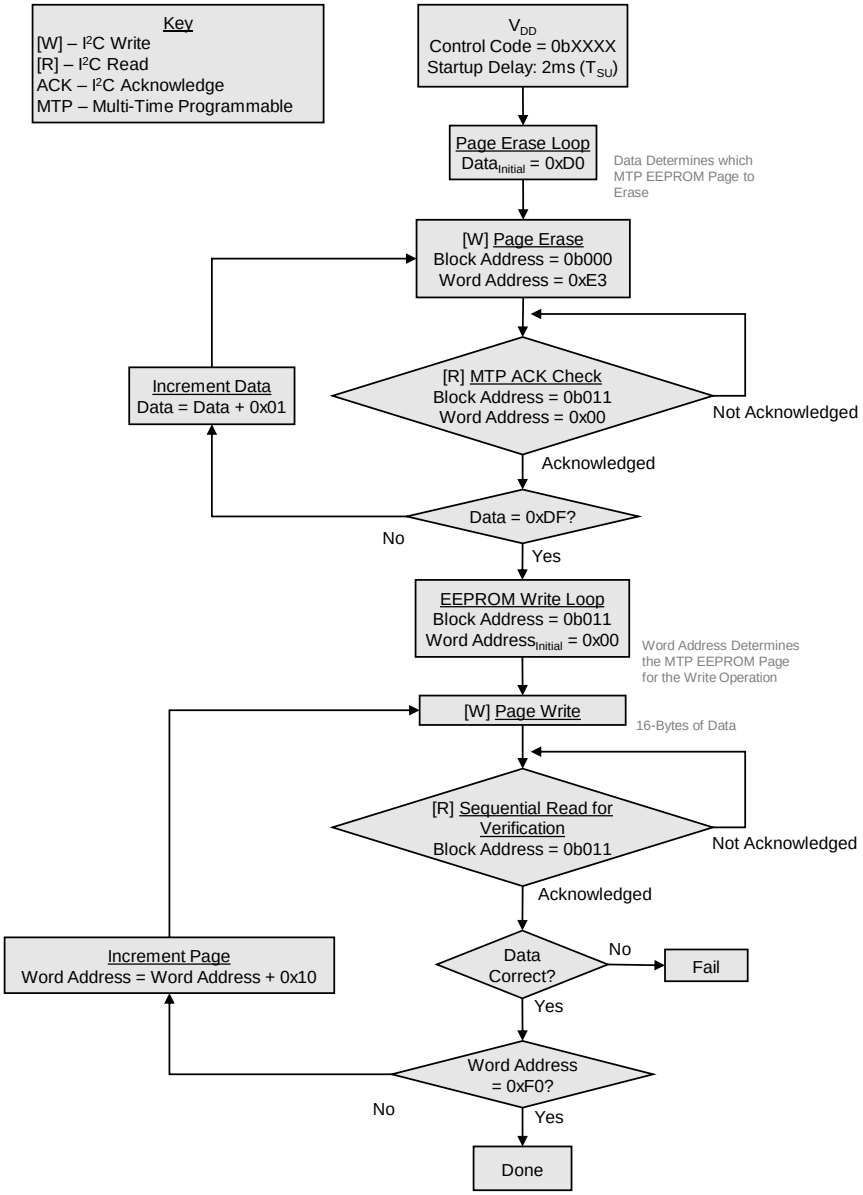

Figure 11: Flowchart for Programming Emulated EEPROM with Acknowledge Polling

Revision History

Revision	Date	Description
1.3	3-Jun-2025	Corrected Tables numbering
1.2	26-May-2025	Updated term Master to Controller to comply with the latest I^2C spec Supplemented subsection 5.2.2 Service Page
1.1	16-Mar-2022	Renesas rebranding
1.0	9-Nov-2020	Initial version

Status Definitions

Status	Definition
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