SLG47011V

Description

This document describes the key functions of the SLG47011V Evaluation Board and provides quick start instructions for using the board.

Features

- Connector for emulating/programming the SLG47011V
- Analog inputs terminal block
- Analog filters for the analog inputs
- Ability to mount SMA connectors for precision measurements
- Connector for other (digital) GPIOs.
- Onboard 3.3V LDO
- Onboard 1.8V voltage reference
- Ground connector

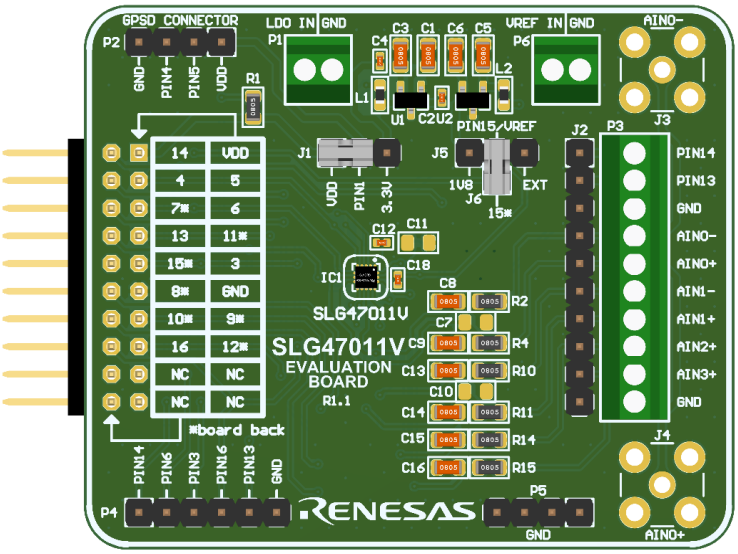

Figure 1. SLG47011V Evaluation Board (Top View)

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1. Functional Description

The SLG47011V evaluation board contains the following items.

- Connector for emulating/programming the SLG47011V chip with the Advanced Development Board (ADB), Light Development Board (LDB) SV1 and GreenPAK Serial Debugger (GPSD) P2
- Analog inputs terminal block P3 duplicated with J2 pin header
- Analog filters for the analog inputs
- Ability to mount SMA connectors (J3 and J4) for precision measurements
- Connector for other (digital) GPIOs
- Onboard 3.3V LDO (selectable by jumper)
- Onboard 1.8V voltage reference (selectable by jumper)
- Ground connector

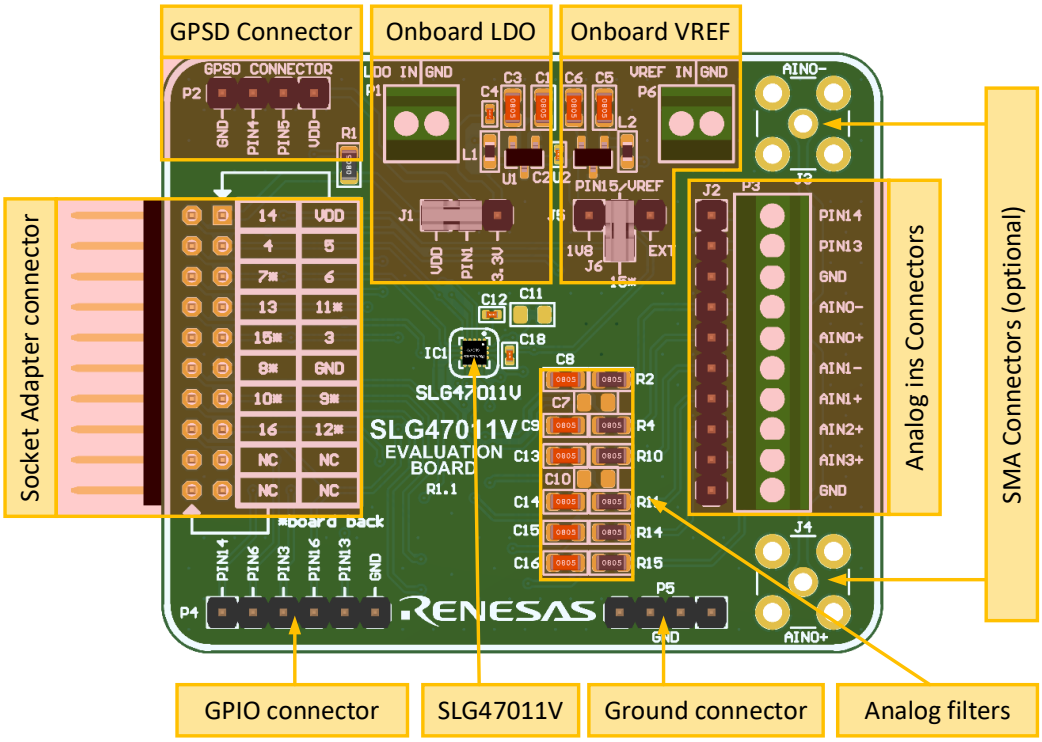


Figure 2. External Connectors and User Control

1.1 Design Emulation, Programming, and Real-Time Testing

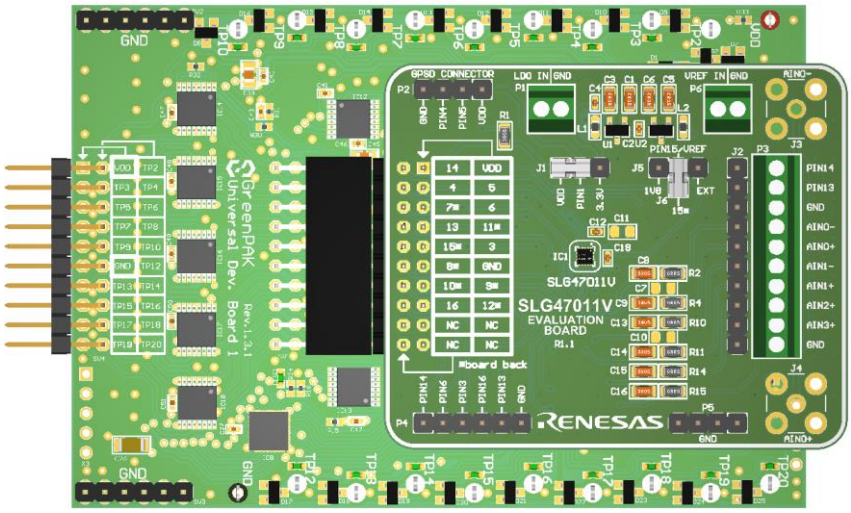


Figure 3. Using ADB for Evaluation

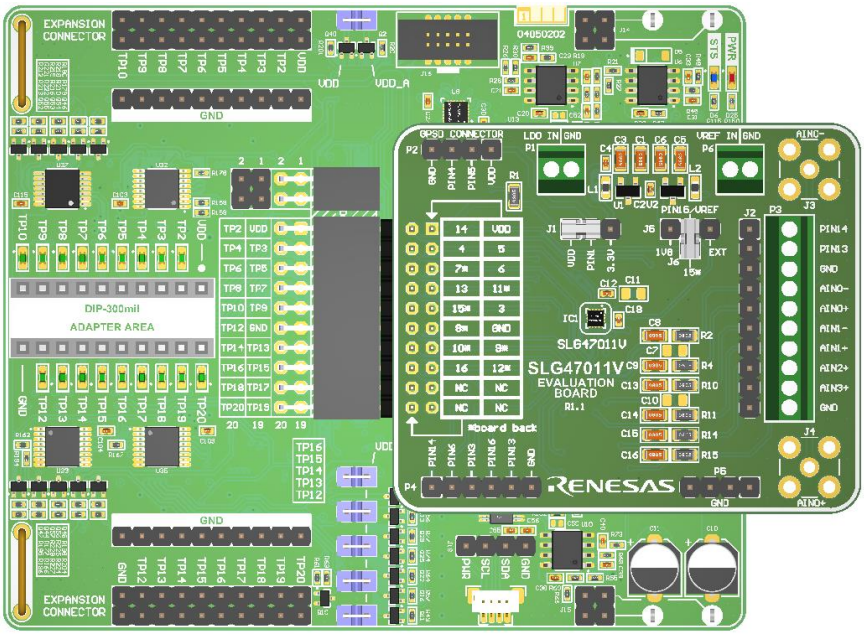


Figure 4. Using LDB for Evaluation

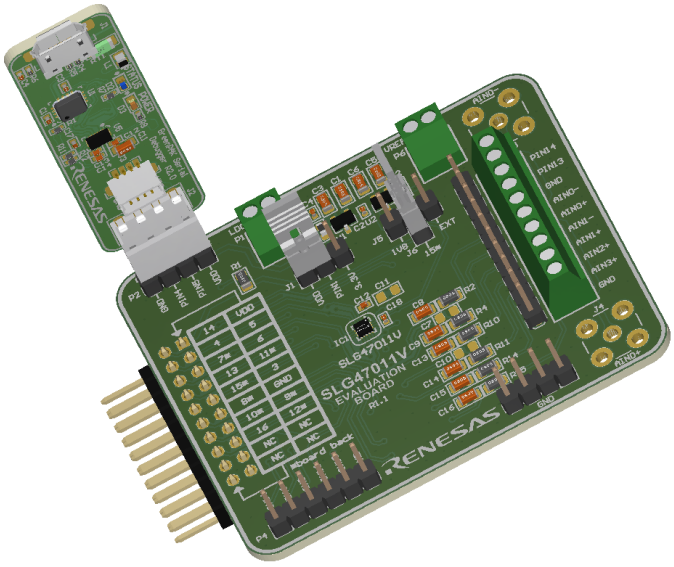


Figure 5. Using GPSD for Evaluation

1.2 Analog Inputs

P3 and J2 have the same pinouts.

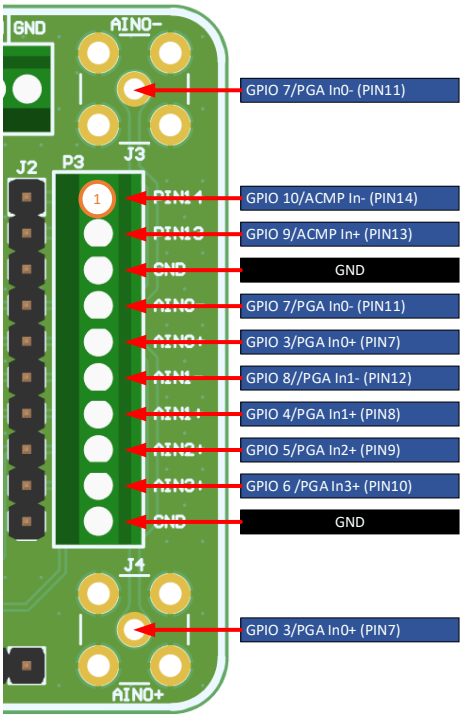


Figure 6. Analog Inputs Connectors

The board can use up to four single-ended analog inputs (AIN0+, AIN1+, AIN2+, AIN3+) or two differential inputs (AIN0+/AIN1+ and AIN0-/AIN1-) along with two additional single-ended analog inputs (AIN2+ and AIN3+).

To use full differential filters on analog inputs AIN0 and AIN1 in the differential mode it is needed to mount C7 and C10 capacitors (1 nF 0805) respectively.

For precise measurements, J3 and J4 SMA connectors (e.g., Adam Tech RF2-04A-T-00-50-G) can be mounted for AIN1+ and AIN1−.

For more information, please refer to Table 1 and Figure 7.

Table 1. P3/J2 Pinout Description

P3/J2 Contact number	P3/J2 Contact name	Assignation	Pin Functions
1	PIN14	GPIO10[1]	GPIO, ACMP In-, EXT OSC0, PGA Out-, VPP[1]
2	PIN13	GPIO9[1]	GPIO, ACMP In+, PGA Out+
3	GND	--	--
4	PIN11	GPIO7[2,4]	GPIO, PGA In0-, CS out, ACMP In+, SLA 2
5	PIN7	GPIO3[2,3,4]	GPIO, PGA In0+, EXT OSC1
6	PIN12	GPIO8[2,4]	GPIO, PGA In1-, DAC out, SLA 3
7	PIN8	GPIO4[2,3,4]	GPIO, PGA In1+
8	PIN9	GPIO5[2,3]	GPIO, PGA In2+
9	PIN10	GPIO6[2,3]	GPIO, PGA In3+, SLA 1
10	GND	--	--

Note 1: During R19UH0227EU0105 IC emulation entry and programming 7.5 V will be present on VPP (SV1-TP2, SLG47011V IC - PIN14).
Note 2: Direct connect.
Note 3: Connected through RC filter.
Note 4: Used in single-ended mode.
Note 5: Used in differential mode.

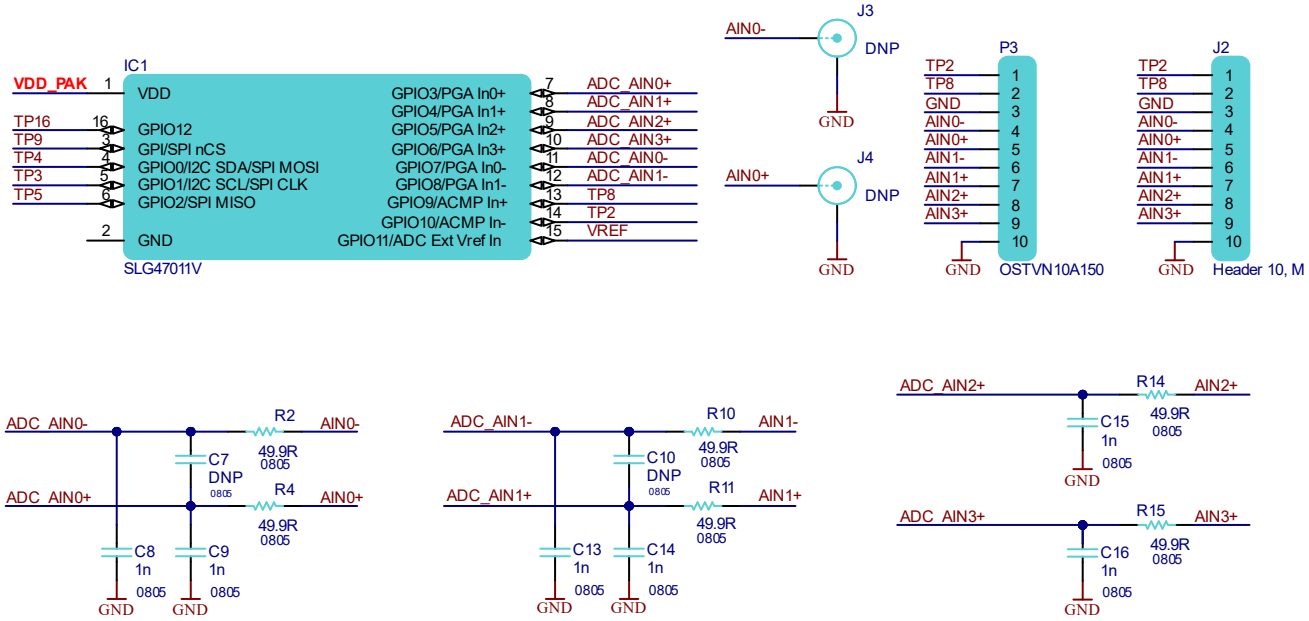


Figure 7. Analog Inputs Schematic

By default, the PGA inputs listed in Table 1 are disconnected from the socket adapter connector SV1. Connection to the SV1 test points requires mounting the corresponding resistor jumpers on the bottom side of the board (see Figure 8).

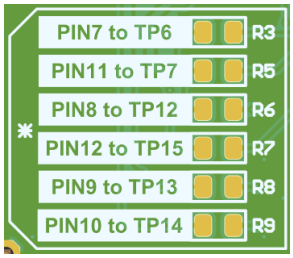
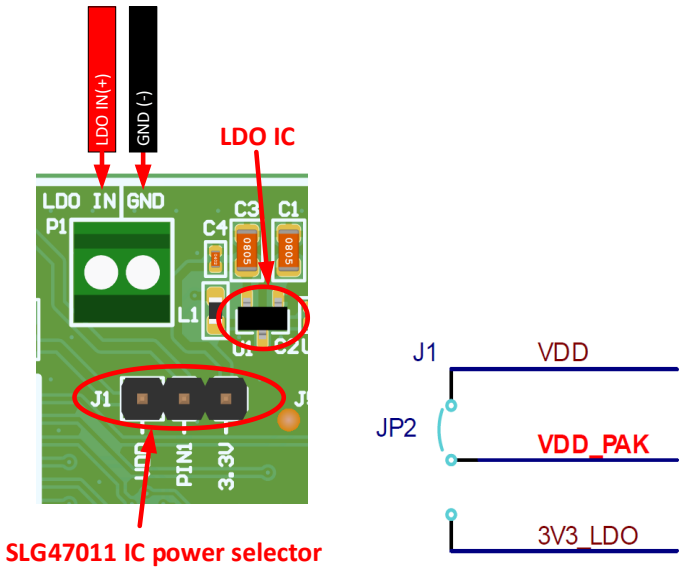


Figure 8. Jumper's Assignment to TPs of Socket Adapter Connector SV1

1.3 SLG47011V IC Power

V_{DD} source of the SLG47011V IC can be selected via jumper JP2 on J1 pin header. See **Figure 9** and **Table 2**.



a) b)

Figure 9. SLG47011V IC Power Selector View a) on Board, b) on Schematic

Table 2. R19UH0227EU0105 IC Power Selector Usage Description

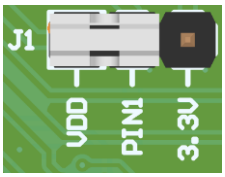
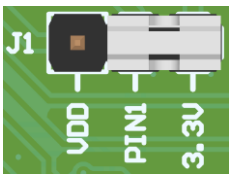
Jumper Position	Description
	Default jumper's position. Powered from V_{DD} (TP1 of socket adapter connector SV1). In the case of using onboard V_{REF}, V_{DD} should meet the operating voltage range (**Table 5**).
	Powered from LDO. Volage source for LDO must be applied to P1 terminal block. For details refer to the **Table 3**.

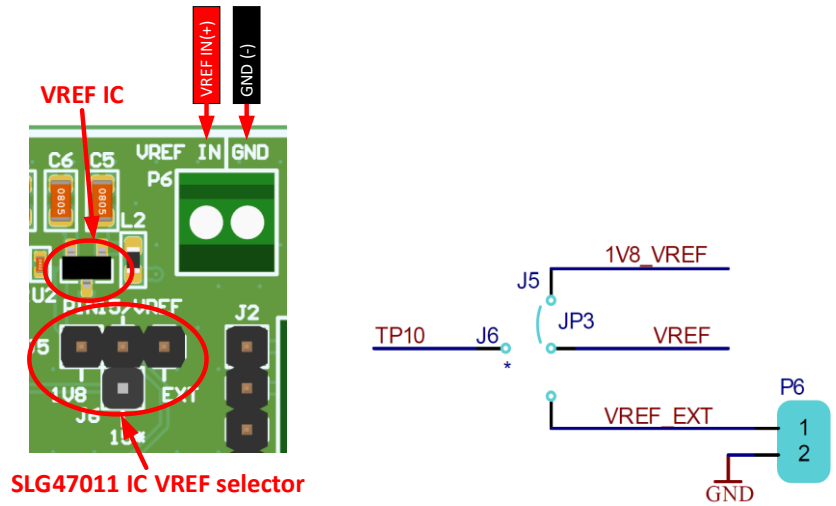
Table 3. Onboard Low-Dropout Regulator DC Characteristics

Parameter	Min	Typ	Max	Unit
Input Operating Voltage	3.7[1]	--	6.0	V
LDO Output Voltage	-	3.3	-	V
LDO Output Current	-	-	200	mA
LDO Line Regulation	-1.0	±0.75	+1.0	%/V
LDO Output Rise Time	-	500	-	µs

Note 1: To achieve output 3.3 V, dropout voltage (350 mV max) is considered.

1.4 SLG47011V IC Voltage Reference

Voltage reference (V_{REF}) for the SLG47011V IC can be selected via jumper JP5 on J6 pin header. See **Figure 10** and **Table 4**.



a) b)

Figure 10. Voltage Reference Selector View a) on Board, b) on Schematic

Table 4. R19UH0227EU0105 IC Voltage Reference Selector Usage Description

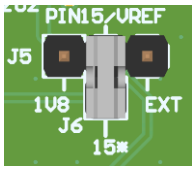
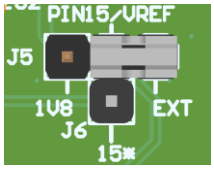
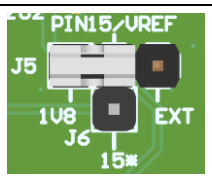
Jumper Position	Description	Note
	Default jumper's position. Connected to TP10 of socket adapter connector SV1	When using PIN15 as a GPIO, keep in mind the presence of capacitors C17 and C18 on the V_{REF} net (see section 7)
	External V_{REF} from P6 terminal block	Input voltage range: 1.5 V to 2 V
	Onboard 1.8 V V_{REF} Input voltage range: 1.5 V to 2 V	See **Table 5**

Table 5. Onboard Voltage Reference DC Characteristics

Parameter	Min.	Typ.	Max	Unit
Input Operating Voltage	2[1]	--	5.5	V
Output voltage	-	1.8	-	V
Initial accuracy	-0.15	-	0.15	%
Output Current range	-	-	5	mA
Output voltage temperature drift	-	9	30	ppm/°C

Note 1: To achieve output 1.8 V, dropout voltage (160mV max) is considered.

1.5 Zero Current Leakage Configuration

In case of the SLG47011V current consumption measurements, it is recommended to cut out jumper trace JP1 on the board back to avoid leakages through onboard V_{REF} (see Figure 11).

Current consumption measurements could be performed by connecting the amperemeter:

- to pin PIN1 and pin V_{DD} of J1 in case of powering from SV1.
- to pin PIN1 and pin 3.3V of J1 in case of powering from onboard LDO.

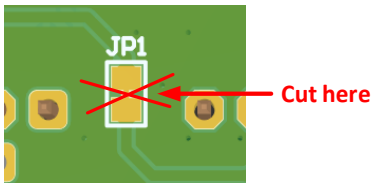


Figure 11. Cut Out Jumper Trace Usage

1.6 GPIO Connector

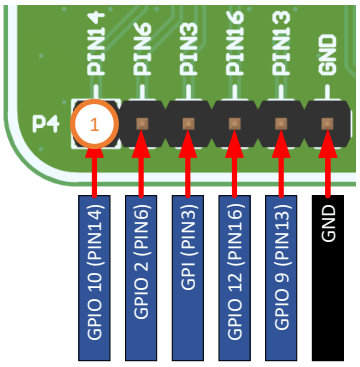


Figure 12. GPIO Connector Pinout

Table 6. P4 Pinout Description

Pin Number	SLG47011V IC pin (GPIO)	SV1
1	PIN14 (GPIO10)	TP2
2	PIN6 (GPIO2)	TP5
3	PIN3 (GPI)	TP9
4	PIN16 (GPIO12)	TP16

Pin Number	SLG47011V IC pin (GPIO)	SV1
5	PIN13 (GPIO9)	TP8
6	GND	TP11

1.7 GPSD Connector

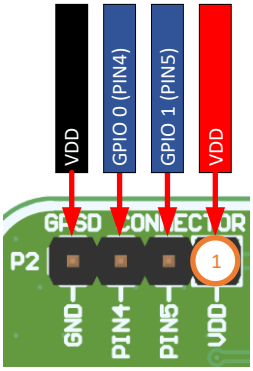


Figure 13. GPSD Connector Pinout

Table 7. GPSD (P2) Pinout Description

Pin Number	SLG47011V IC pin (GPIO)	SV1
1	PIN1 V_{DD}	TP1
2	PIN5 (GPIO1)	TP3 (SCL[1])
3	PIN4 (GPIO0)	TP4 (SDA[1])
4	GND	TP11

Note 1 – If I^2C master SCL, SDA lines do not have pull-ups it is possible to mount resistors R12 and R13 (pull up to V_{DD}) on board back.

1.8 Ground Connector

Figure 14. GND Connector View

P5 (all pins are GND) is a common usage connector, for instance, simplifying measurements by oscilloscope probes.

2. Board Design

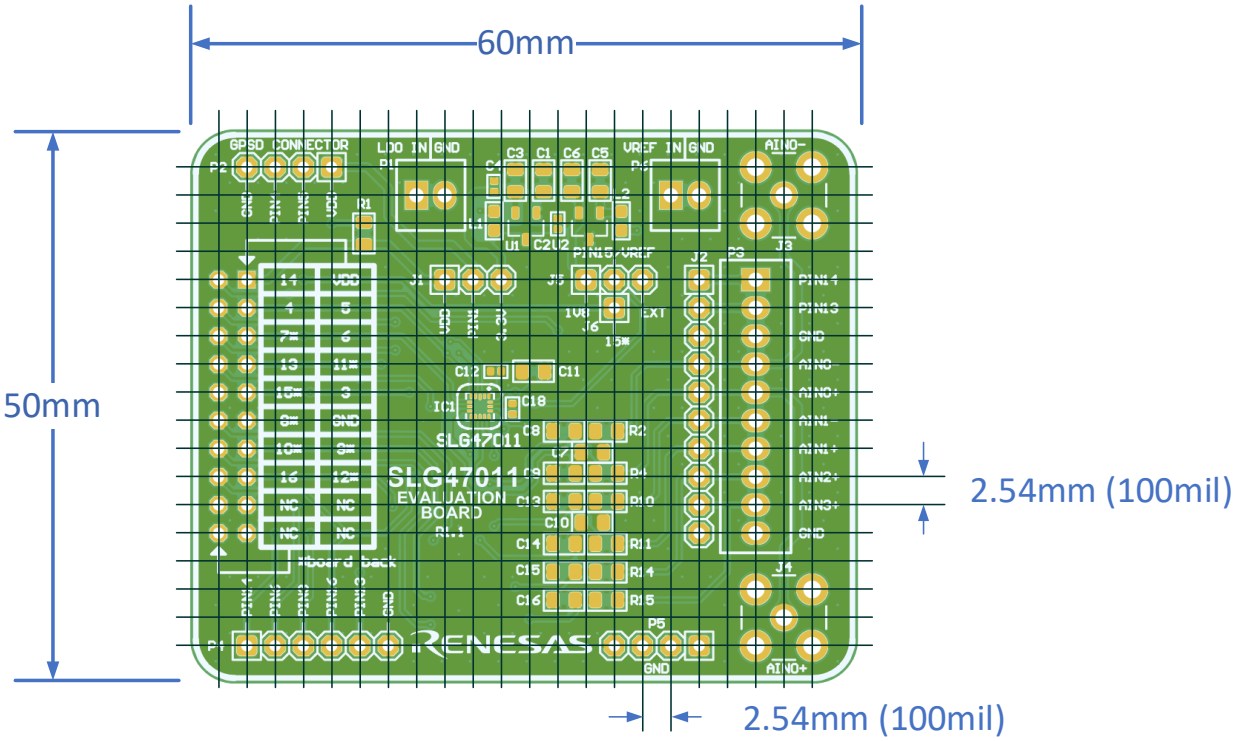


Figure 15. Board Top Dimensions

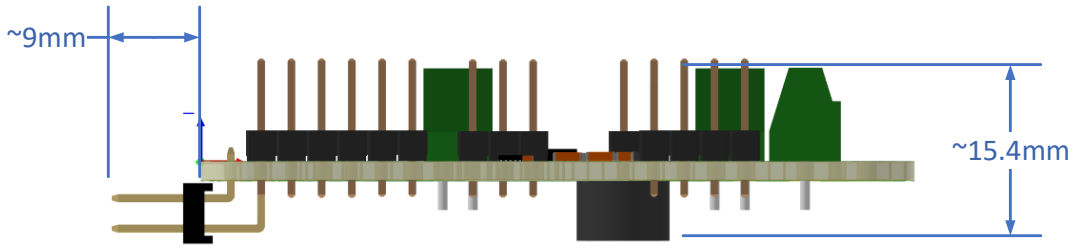
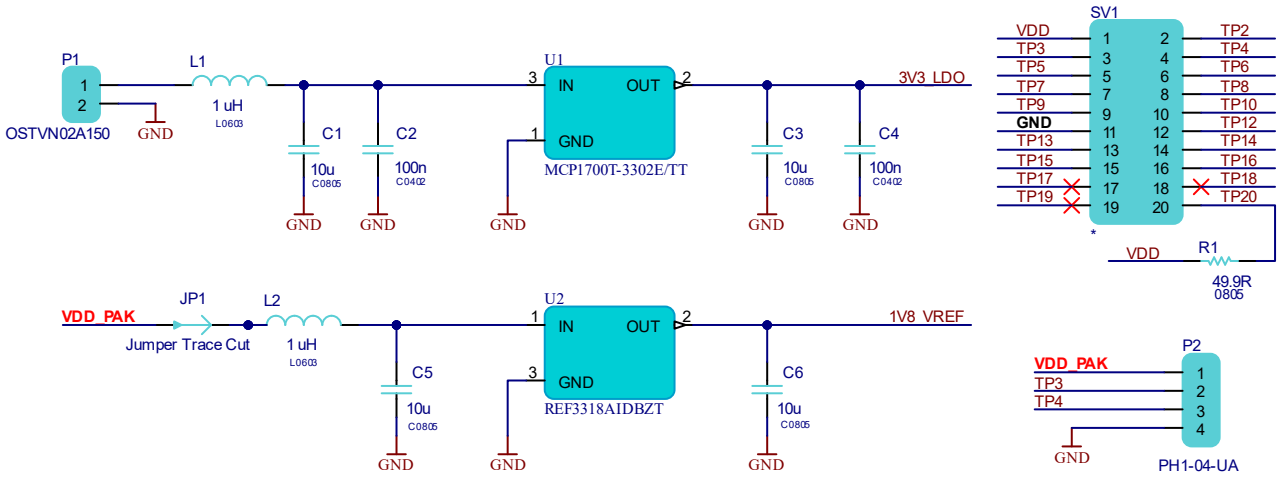
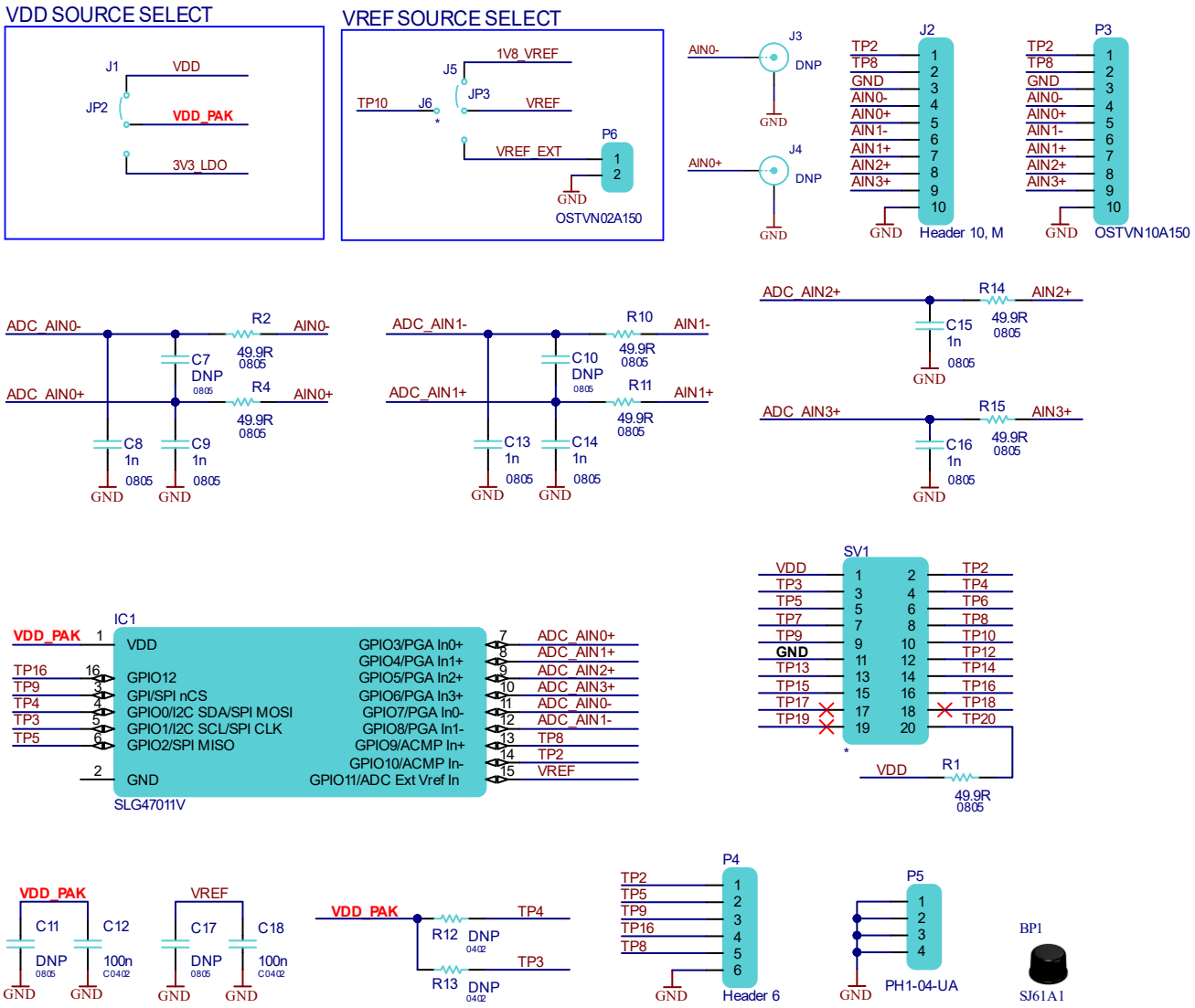


Figure 16. Board Assembly Side Dimensions

2.1 Schematic Diagrams




VDD SOURCE SELECT
J1
VDD
JP2
VDD_PAK
3V3_LDO
VREF SOURCE SELECT
1V8_VREF
J5
JP3
TP10
J6
VREF
VREF_EXT
P6
GND
OSTVN02A150
AIN0-
J3
DNP
GND
AIN0+
J4
DNP
GND
J2
TP2
TP8
GND
AIN0-
AIN0+
AIN1-
AIN1+
AIN2+
AIN3+
GND
Header 10, M
P3
TP2
TP8
GND
AIN0-
AIN0+
AIN1-
AIN1+
AIN2+
AIN3+
GND
OSTVN10A150
ADC_AIN0-
R2
AIN0-
49.9R
0805
C7
DNP
0805
ADC_AIN0+
R4
AIN0+
49.9R
0805
C8
1n
0805
C9
1n
0805
GND
GND
ADC_AIN1-
R10
AIN1-
49.9R
0805
C10
DNP
0805
ADC_AIN1+
R11
AIN1+
49.9R
0805
C13
1n
0805
C14
1n
0805
GND
GND
ADC_AIN2+
R14
AIN2+
49.9R
0805
C15
1n
0805
GND
ADC_AIN3+
R15
AIN3+
49.9R
0805
C16
1n
0805
GND
IC1
VDD_PAK
VDD
TP16
TP9
TP4
TP3
TP5
GPIO12
GPI/SPI nCS
GPIO0/I2C SDA/SPI MOSI
GPIO1/I2C SCL/SPI CLK
GPIO2/SPI MISO
GND
GPIO3/PGA In0+
GPIO4/PGA In1+
GPIO5/PGA In2+
GPIO6/PGA In3+
GPIO7/PGA In0-
GPIO8/PGA In1-
GPIO9/ACMP In+
GPIO10/ACMP In-
GPIO11/ADC Ext Vref In
ADC_AIN0+
ADC_AIN1+
ADC_AIN2+
ADC_AIN3+
ADC_AIN0-
ADC_AIN1-
TP8
TP2
VREF
SLG47011V
SV1
VDD
TP3
TP5
TP7
TP9
GND
TP13
TP15
TP17
TP19
TP2
TP4
TP6
TP8
TP10
TP12
TP14
TP16
TP18
TP20
VDD
R1
49.9R
0805
VDD_PAK
C11
DNP
0805
C12
100n
C0402
GND
GND
VREF
C17
DNP
0805
C18
100n
C0402
GND
GND
VDD_PAK
R12
DNP
0402
TP4
R13
DNP
0402
TP3
P4
TP2
TP5
TP9
TP16
TP8
GND
Header 6
P5
GND
PH1-04-UA
BP1
SJ61A1

2.2 Bill of Materials

#	Designator	Manufacturer Part Number 1	Manufacturer 1	Quantity
1	BP1	70006431426	3M	1
2	C1, C3, C5, C6	C0805C106M8RACTU	KEMET	4
3	C2, C4, C12, C18	C0402C104K4RACTU	KEMET	4
4	C7, C10, C11, C17			4
5	C8, C9, C13, C14, C15, C16	08055C102KAT2A	Kyocera AVX	6
6	IC1	SLG47011V	Renesas	1
7	J1, J5	PH1-03-UA	Adam Equipment	2
8	J2	68001-410HLF	Amphenol ICC / FCI	1
9	J3, J4			2
10	J6	PH1-01-UA	Adam Equipment	1
11	JP2, JP3	NPC02SXON-RC	Sullins	2
12	L1, L2	CS160808-1R0K	Bourns	2
13	P1, P6	OSTVN02A150	On-Shore Technology	2
14	P2, P5	PH1-04-UA	Adam Equipment	2
15	P3	OSTVN10A150	On-Shore Technology	1
16	P4	PR20206VBNN	METZ CONNECT	1
17	R1, R2, R4, R10, R11, R14, R15	CRCW080549R9FKEA	Vishay	7
18	R3, R5, R6, R7, R8, R9, R12, R13			8
19	SV1	68021-220HLF	Amphenol ICC / FCI	1
20	U1	MCP1700T-3302E/TT	Microchip	1
21	U2	REF3318AIDBZT	Texas Instruments	1

3. Ordering Information

Part Number	Description
SLG47011V-EVB	SLG47011V Evaluation Board

4. Terms and Definitions

ADB	Advanced Development Board
GPIO	General Purpose Input/Output
GPSD	GreenPAK Serial Debugger
IC	Integrated Circuit
LDB	Light Development Board
LDO	Low-dropout linear regulator
TP	Test point
V_{REF}	Voltage reference

5. References

[1] SLG47011 Datasheet, Renesas Electronics.

6. Revision History

Revision	Date	Description
1.05	Jan 5, 2026	Updated Terms and Definitions Detailed Analog Inputs Description Fixed typos
1.04	Dec 23, 2025	Updated tables P3/J2 Pinout Description and R19UH0227EU0105 IC Vref Selector Usage Description
1.03	Dec 16, 2025	Updated table Onboard Low-Dropout Regulator DC Characteristics Updated table Onboard Voltage Reference DC Characteristics Updated Figure 9 and Figure 10
1.02	Dec 2, 2025	Updated PIN14 description Updated template
1.01	Oct 24, 2023	Added Ordering Information
1.00	Sep 22, 2023	Initial release.