User Manual

DA1468x/DA1510x PRO-Development Kit

UM-B-060

Abstract

PRO-Development it consists of PRO motherboard (224-12-x) and PRO daughterboard (224-14-x or 224-15-x)

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1 Terms and definitions

BT	Bluetooth
BLE	Bluetooth Low Energy
PRO	Professional
Devkit	Development Kit
SW	Software
USB	Universal Serial Bus
JTAG	Join Test Action Group
UART	Universal Asynchronous Receiver/Transmitter
SPI	Serial Peripheral Interface
LED	Light Emitting Diode
LDO	Low-Dropout
SOC	System on Chip

2 References

Datasheet of DA14680/682, Low Power Bluetooth Smart 4.2 SoC with FLASH

Datasheet of DA14681/683, Low Power Bluetooth Smart 4.2 SoC

Datasheet of DA15100, Combo Bluetooth Smart and 802.15.4 SoC with FLASH

Datasheet of DA15101, Combo Bluetooth Smart and 802.15.4 SoC

3 Introduction

The PRO Development kit hardware set up is described on this document. The block diagram, the boards, the various sections, the settings as well as the connectivity is presented.

The PRO development kit consists of the PRO motherboard and the PRO daughterboard (two variants available, AQFN60 and WLCSP). The development kit supports DA14680, DA14681, DA14682, DA14683, DA15100 and DA15101 SoCs of Dialog Semiconductor.

Special attention for the deployment of this kit has been given in providing a trouble-free user experience.

Figure 1: PRO development kit, motherboard and daughterboard

4 System overview

4.1 Features

- Highly integrated Dialog Semiconductor DA1468x/DA1510x *SoC* supported
- DA1468x/DA1510x SoCs can be accessed over UART and/or JTAG with no additional external hardware
- Access on all GPIOs provided from the chipReset push button
- General purpose LED and Push Button
- White LED connected to dedicated PWM pin (LED1 pin)
- Current monitoring circuit associated with appropriate software on PC
- Powered from either USB2 (DBG) connector or Li-Po Battery
- JTAG and UART interface over USB2 (DBG) connector for development purposes
- Option for Coin-Cell battery on the daughterboard (non-rechargeable, no current monitored)
- Dedicated USB (USB1-CHG) connector for charging a Li-Po battery
- DA1468x/DA1510x different package easily replaceable by replacing the daughterboard
- QSPI flash on daughterboard for DA14681, DA14683 and DA15101
- 2.4GHz printed inverted-F antenna on the daughterboard
- RF mechanical switch for conducted RF measurements on the daughterboard
- Breakout headers with clearly marked signals
- 16 MHz system and 32.768 KHz low-power crystals on the daughterboard
- Fixed 3.0V/1.8V and a variable (1.9 to 4.3V) LDO power options

4.2 General description

The PRO development kit consists of the motherboard (Pro motherboard) and the PRO daughterboard (two variants available, AQFN60 and WLCSP):

- PRO motherboard with board number: 224-12-E
- AQFN60 daughterboard, with board number: 224-14-D
- WLCSP daughterboard with board number: 224-15-E

Individual daughterboards are populated with each different version of SoC. For DA14681, DA14683 and DA15101 an external Flash is populated and there are daughterboard options with the SOC in aQFN-60 or WLCSP-53 package. For DA14680, DA14682 and DA15100 no external Flash is populated and these are available only in the aQFN-60 package.

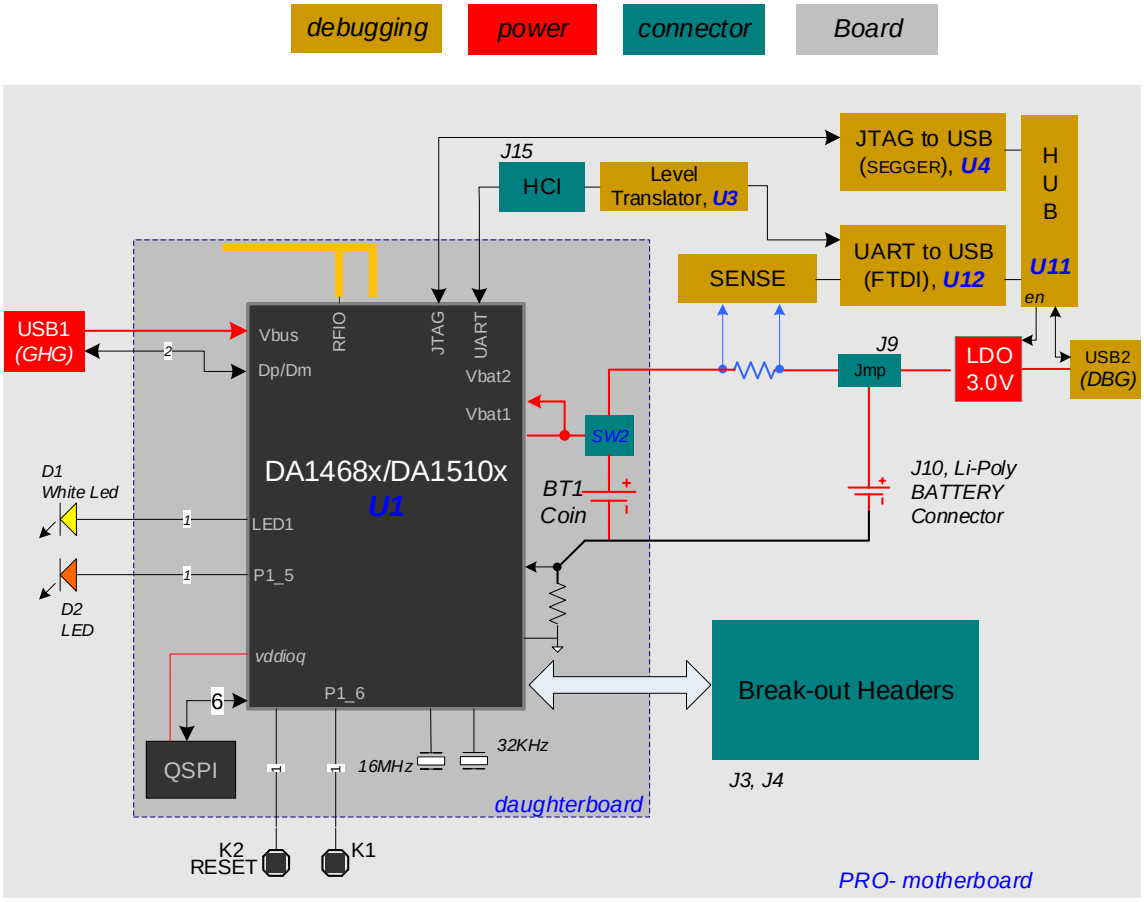

Figure 2: PRO development kit block diagram

DA1468x/DA1510x SoC is carried on the PRO daughterboard. PRO motherboard provides power supply options to SoC, external reset, JTAG, UART, power measurements, as well as configuring and monitoring capabilities. PRO motherboard and PRO daughterboard are the main components of the PRO development kit.

5 PRO motherboard

5.1 Overview

Board number

- 224-12-E

Ports

- USB1 (CHG) for charging purpose
- USB2 (DBG) for evaluation and debugging purposes

Interfaces

- UART
- JTAG

Connectivity – Expansion connectors

- AQFN/WLCSP daughterboards (J1, J2)
- Breakout headers (J3, J4)

Power source selection

- USB2 (DBG)
- Li-Poly battery

Figure 3: The PCBA of PRO motherboard (224-12-E)

PRO motherboard description can be separated into the following sections:

- Signal monitoring/interface (connector section): In this section the jumper settings are described.
- Evaluation / Debugging section: provides connectivity of the PRO Development kit to PC through UART and JTAG ports. Only the current that is drawn from the daughterboard is monitored and its value is fed into the PC via UART. Finally, user can *reset* the chip via the push button (K2).
- Power section: all power components available on the motherboard are described. Moreover, power supplying option of the AQFN and WLCSP daughterboards is presented.

5.2 Interface PRO motherboard / daughterboard

The PRO motherboard provides a detachable board interface and a pair of break out connectors. The interface is for a daughterboard, which comes in AQFN60 and WLCSP versions:

J1/J2: interfaces with DA1468x/DA1510x daughterboards

J3/J4: breakout connectors where DA1468x/DA1510x SoC signals can be accessed.

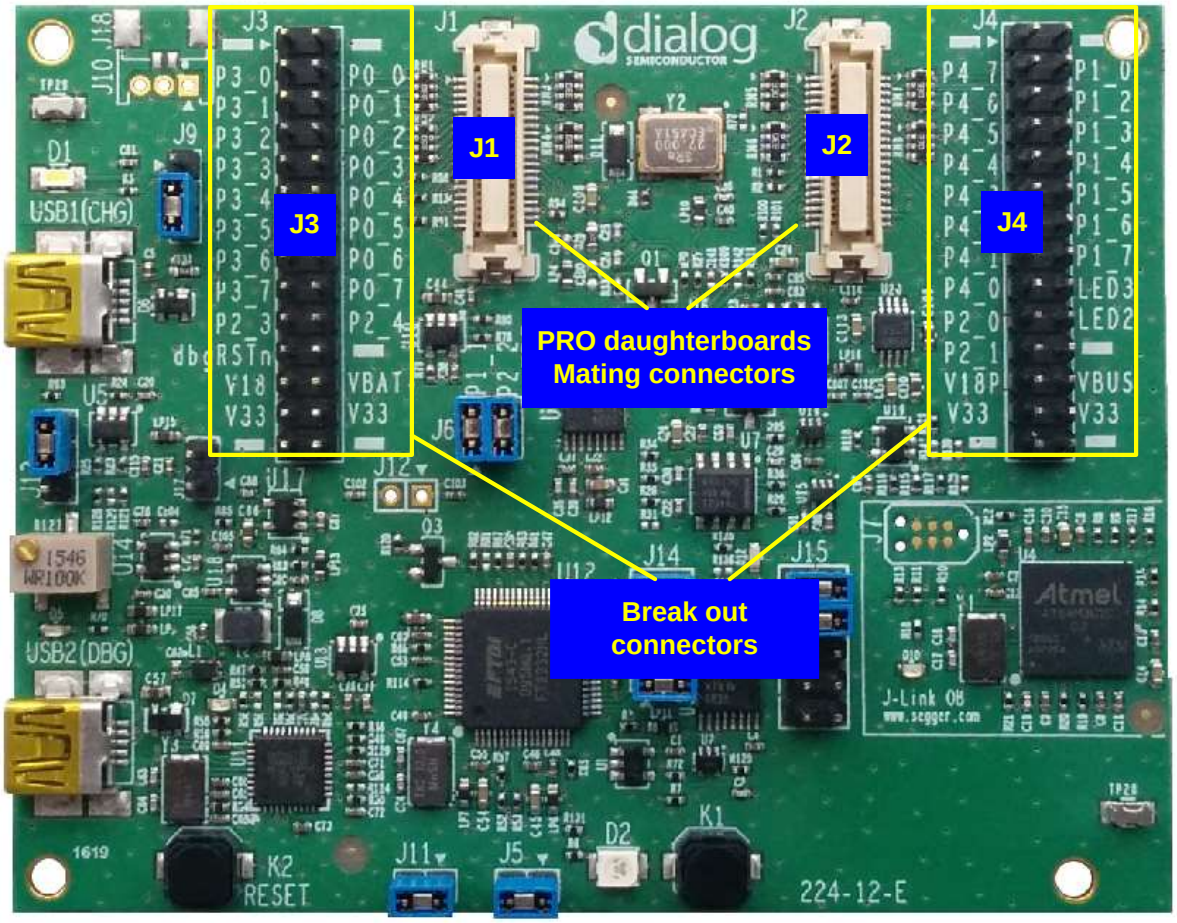

Figure 4: PRO motherboard mating connectors

5.2.1 PRO motherboard pin assignment

On table below, the pin assignment on the connectors of the PRO motherboard is provided. There are two columns, one for WLCSP and one for AQFN package of the DA1468x/D1510x SoCs.

Table 1: PRO motherboard / daughterboard pin assignment

Pin Name	WLCSP	AQFN60	Daughter Board	Breakout Headers	Comments
P0_0	FL_CLK		J1.4	J3.4	*Only for DA14681/ DA14683/DA15101* *For DA14680/ DA14682/DA15100 these pins are Not Connected*
P0_1	FL_D0		J1.6	J3.6	
P0_2	FL_D1		J1.8	J3.8	
P0_3	FL_D2		J1.10	J3.10	
P0_4	FL_D3		J1.12	J3.12	
P0_5	FL_CS		J1.14	J3.14	
P0_6	SWDIO		J1.16	J3.16	
P0_7	GPIO		J1.18	J3.18	
P1_0	GPIO		J2.4	J4.4	*Through header J5*
P1_1	USBN		J2.31		*Through header J6*
P1_2	GPIO		J2.6	J4.6	
P1_3	UTX		J2.8	J4.8	
P1_4	URTS(out) / LED (D2)		J2.10	J4.10	*Through header J5. Only one can be assigned*
P1_5	URXTS		J2.12	J4.12	*Through header J5*
P1_6	UCTS(in) / BUTTON (K1)		J2.14	J4.14	*Through header J5. Only one can be assigned*
P1_7	GPIO		J2.16	J4.16	
P2_0	Xtal32p		J2.23	J4.19	*Through no populated resistors on daughterboard*
P2_1	Xtal32n		J2.25	J4.21	*Through no populated resistors on daughterboard*
P2_2	USBP		J2.33		*Through header J6*
P2_3	URX		J1.19	J3.19	
P2_4	SWCLK		J1.28	J3.20	
P3_0		GPIO	J1.3	J3.3	*Only available with aQFN daughterboard*
P3_1		GPIO	J1.5	J3.5	
P3_2		GPIO	J1.7	J3.7	
P3_3		GPIO	J1.9	J3.9	
P3_4		GPIO	J1.11	J3.11	
P3_5		GPIO	J1.13	J3.13	
P3_6		GPIO	J1.15	J3.15	
P3_7		GPIO	J1.17	J3.17	
P4_0		GPIO	J2.17	J4.17	
P4_1		GPIO	J2.15	J4.15	
P4_2		GPIO	J2.13	J4.13	
P4_3		GPIO	J2.11	J4.11	
P4_4		GPIO	J2.9	J4.9	
P4_5		GPIO	J2.7	J4.7	
P4_6		GPIO	J2.5	J4.5	
P4_7		GPIO	J2.3	J4.3	
LED1	LED1		J1.27		*Not applied on Break-out headers*
LED2		LED2	J2.24	J4.20	*Only available with aQFN daughterboard*
LED3		LED3	J2.22	J4.18	

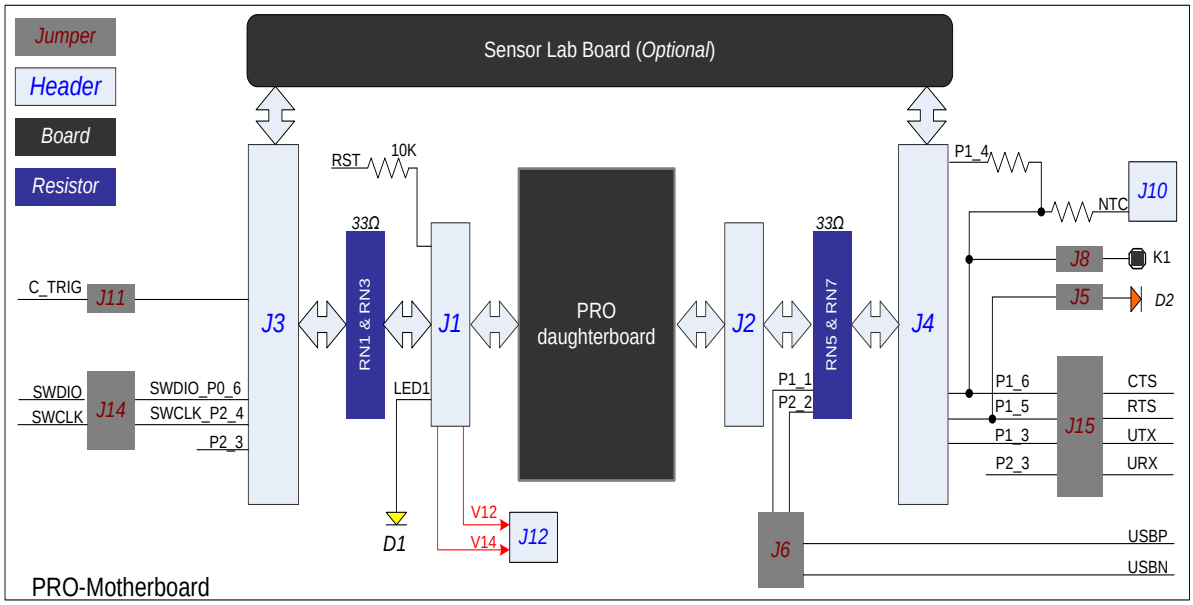

Figure 5: Signals interconnection of PRO Development kit

5.2.2 PRO motherboard Jumper settings

Table 2: Jumper settings on motherboard

header	Default Jumper position	function
J5	1-2	P1_5 to RTS
J6	Mounted 1-2 Mounted 3-4	USB1(CHG), signals Dp/Dm are connected to DA1468x/DA1510x
J8	1-2	P1_6 to CTS
J9	Mounted 2-3	DA1468x/DA1510x Daughterboard is supplied from 2-3: VLDO 1-2: Li-Poly
J11	Not mounted	Enables triggering from chip. To be used on current sense circuitry
J12	No jumper allowed	Monitoring V12 (pin1) and V14 (pin2)
J13	Mounted 1-2	Mounted 1-2 : VLDO produces 3.0V Mounted 2-3 : VLDO adjustable through R127 Not Mounted: VLDO produces 1.8V
J14	Mounted	JTAG connection to external PC is enabled
J15	Mounted 1-2 & 3-4	UART (TX, RX) connection to external PC is enabled. For enabling full UART, mount 5-6 and 7-8.
J17	Not mounted	Mounted: force Power Enable of PRO motherboard power devices (e.g., U5, U18 etc.)

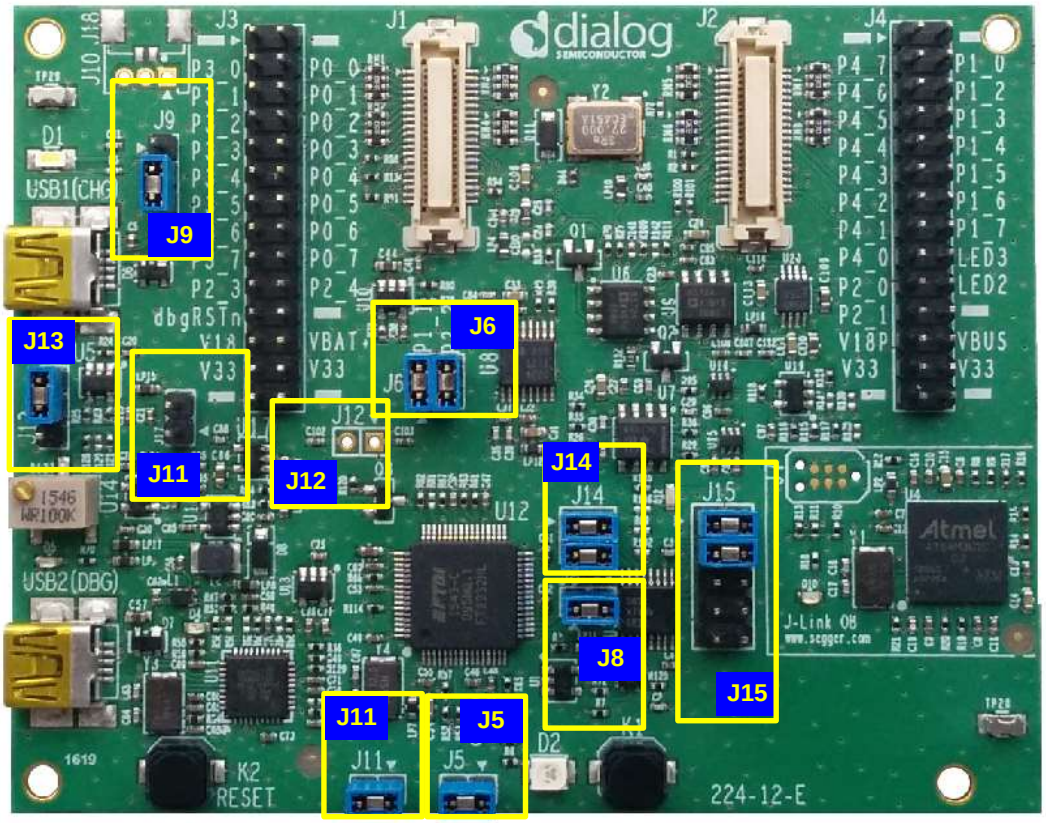

Figure 6: Jumper's placement on the motherboard

5.3 Evaluation / Debugging section

The evaluation debugging section of PRO motherboard consists of the JTAG, UART, current sense circuitries, as well as push buttons (including Reset) and Leds. This section is powered via USB2.

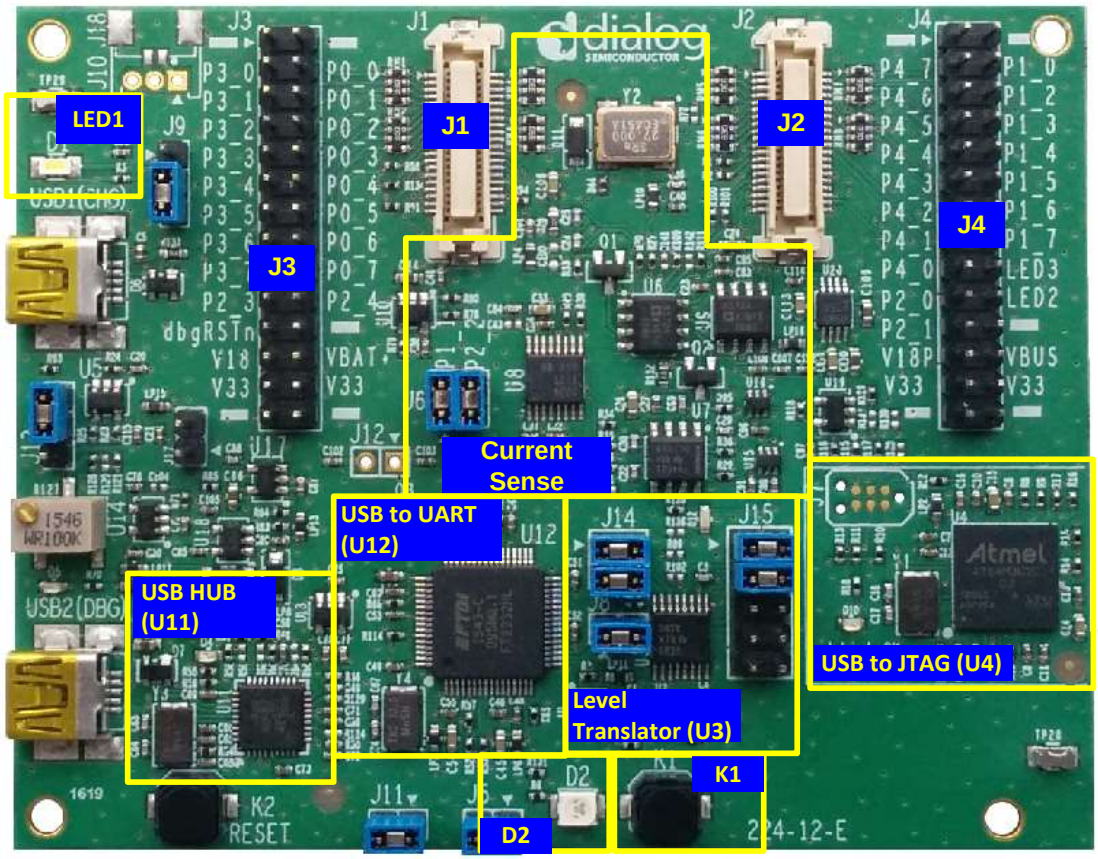

Figure 7: Evaluation/debugging section

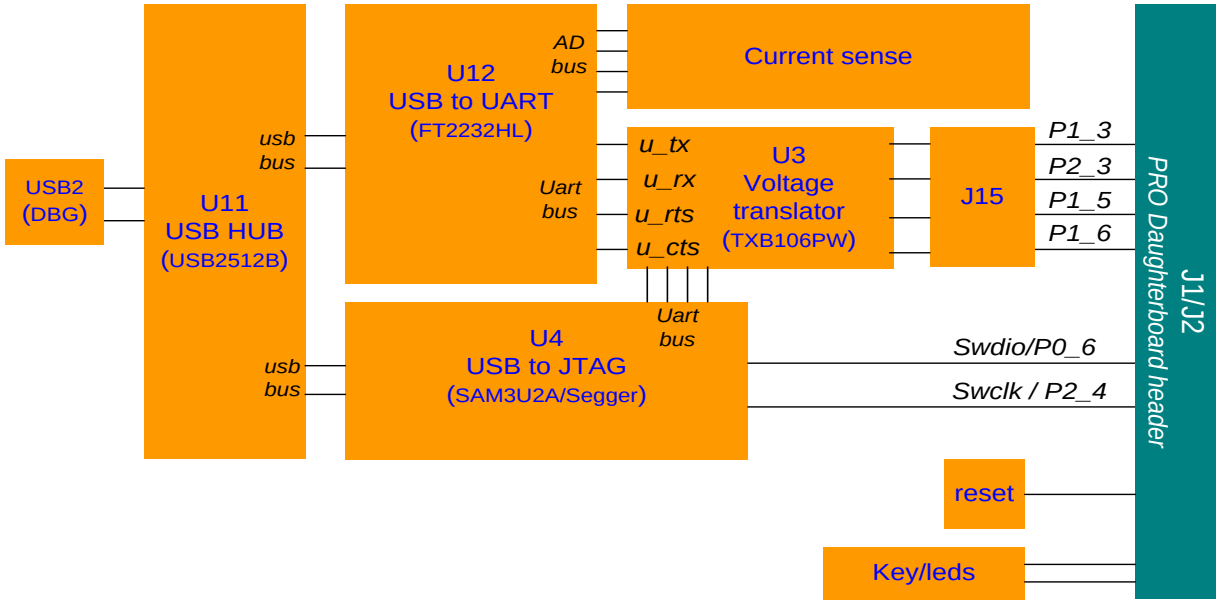

Figure 8: The block diagram of the debugging section

Table 3: Evaluation / debugging pins

	Function	DA1468x/DA1510x			BREAKOUT headers	Test points
		Pin name	AQFN60 Pin	WLCSP Pin	pins	
UART	UART transmit (TX)	P1_3	B23	B6	J4.8	TP48
	UART receive (RX)	P2_3	A35	B5	J3.19	TP50
	UART RTS	P1_5	A28	B2	J4.12	TP51
	UART CTS	P1_6	B12	E2	J4.14	TP52
JTAG	JTAG data (SWDIO)	P0_6	B8	F4	J3.16	TP49
	JTAG clock (SWCLK)	P2_4	A14	F5	J3.20	TP54
BUTTONs	RESET (K2)	RST	A21	G1	J3.21 (inverted)	
	K1 (multiplexed)	P1_6	B12	E2	J4.14	
LEDs	D1 (White LED)	LED1	B10	G2		TP35 (through R5)
	D2 (orange LED)	P1_5	A28	B2		TP34
	D3 (Segger green LED)					TP9
	D4 (USB HUB green)					TP36
	D5 (U14, green)					TP41

5.3.1 RESET

RESET pin of Da1468x/DA1510x is driven through inverter U2, from:

- USB to JTAG chip (U4)
- USB to UART chip (U12). This option is not enabled
- An active-low signal applied to J3-21

After inversion the reset signal (RST) is driven to daughter board connector (J1)

Reset button (K2) connects the RST pin directly with V33, therefore creates a hardware reset on the SOC regardless the state of other possible sources. This is useful in case the daughterboard is supplied from a battery while the PRO-Motherboard is not powered at all.

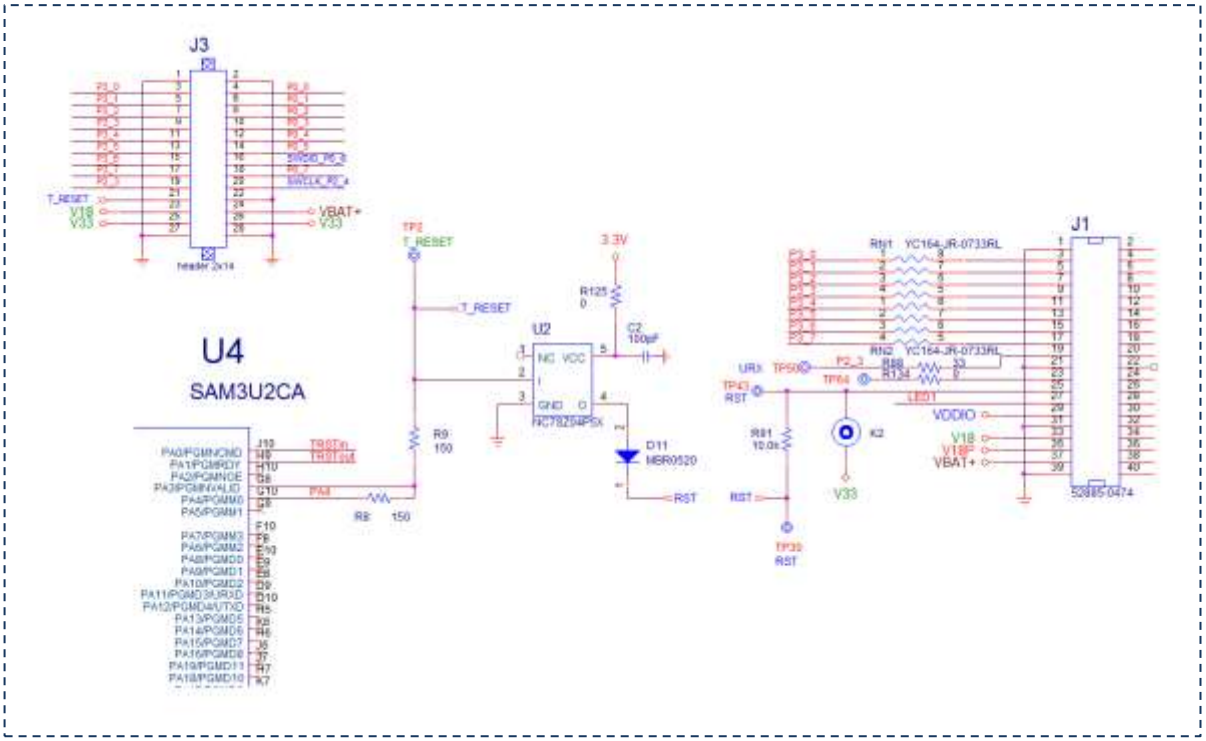

Figure 9: RESET connectivity on PRO Motherboard

5.3.2 Voltage level translation

DA1468x/DA1510x SoC is accessed from a PC through UART and JTAG (U12 and U4 respectively). U12 and U4 are supplied with 3.3V. In the case that the SoC IO voltage rail is significantly less than 3.3V a miscommunication may occur, e.g. a discharged battery supplies the SoC. For avoiding this, a voltage translation circuitry has been added.

The selected chip (TXB0106) is a 6-Bit Bidirectional Level-Shifting and Voltage Translator with automatic direction detection.

Table 4: Signals using a voltage level translation/isolation chip

Pin name	Signal name
P0_6	SWDIO
P2_4	SWCLK
P1_3	TX
P2_3	RX
P1_5	RTS
P1_6	CTS

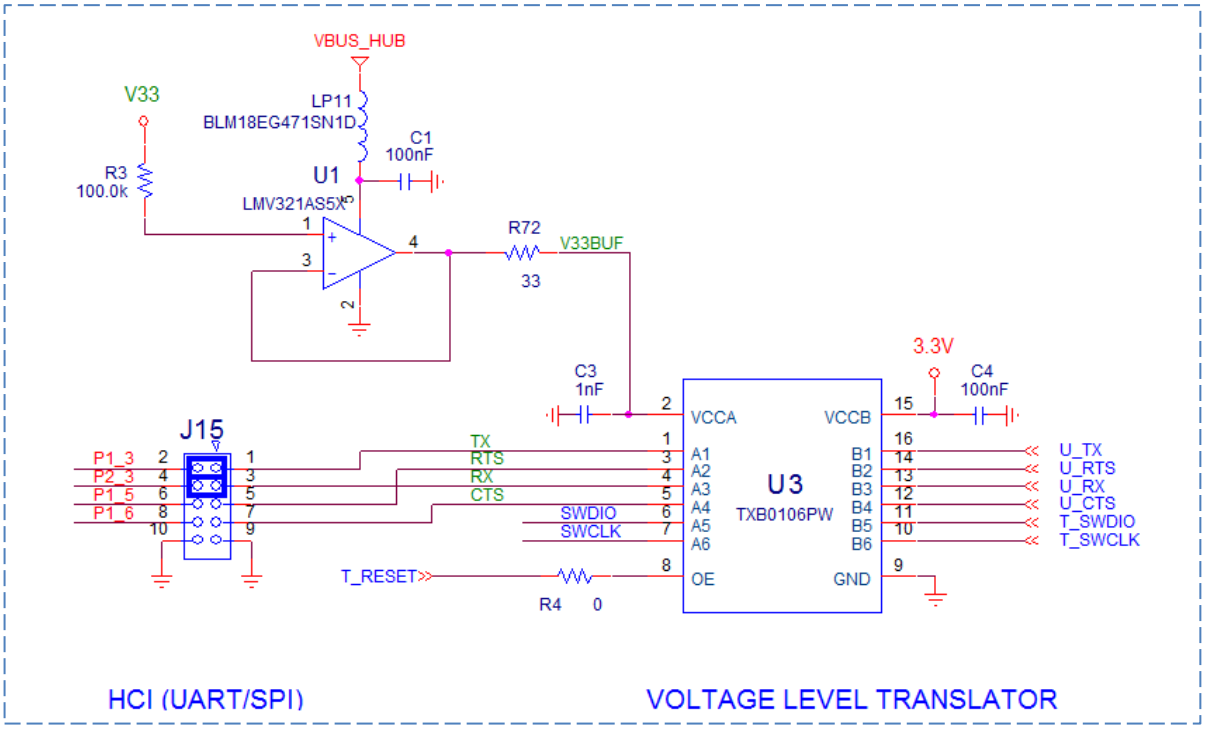

Figure 10: Level translator schematic

5.3.3 Leakages during power measurements

Current leakages occur through UART and JTAG interfaces during sleep mode. For measuring the real power consumption during sleep modes (especially Hibernation), UART and JTAG must be isolated from the rest of the (debugging) circuit. This is achieved by removing the jumpers from **J15** and **J14** for UART and JTAG respectively.

5.3.4 HCI / UART header (J15)

J15 interconnects DA1458x/DA1510x SoC UART signals with U12, USB to UART (FT2232HL) chip.

By removing jumpers, J15 can be used as a HCI header for other embedded hardware.

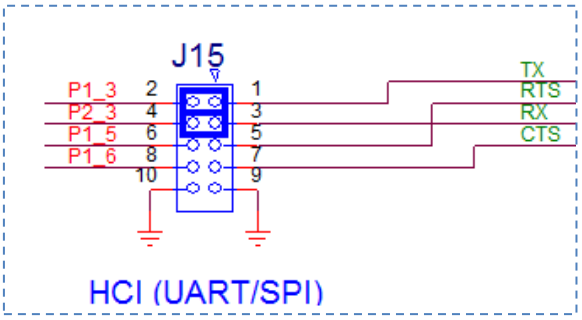

Figure 11: HCI/UART header (J15)

On-board USB/UART: by default, only TX and RX signals are connected with the jumpers placed. RTS and CTS are multiplexed with other functions. For a full UART functionality, jumpers need to be added between RTS – P1_5 and CTS – P1_6.

Table 5: DA1468x/DA1501x pin assignment of UART Signals

DA1468x/DA1510x Pin name	Signal name	Multiplexed with functions
P1_3	TX	
P2_3	RX	
P1_5	RTS	• LED, through J5
P1_6	CTS	• K1 push button through jumper J8 • NTC through R89

5.3.5 Full UART configuration HCI / UART header (J15)

Full UART configuration is supported by enabling RTS and CTS. In this configuration:

- Jumpers in red must be placed in J15 between pin 5-6 and pins 7-8 for RTS and CTS respectively. (Figure 12)
- Jumpers should be removed from J5 and J8. By this way signal P1_5 and P1_6 are not connected anymore to LED D2 and key K1, respectively (Figure 12)

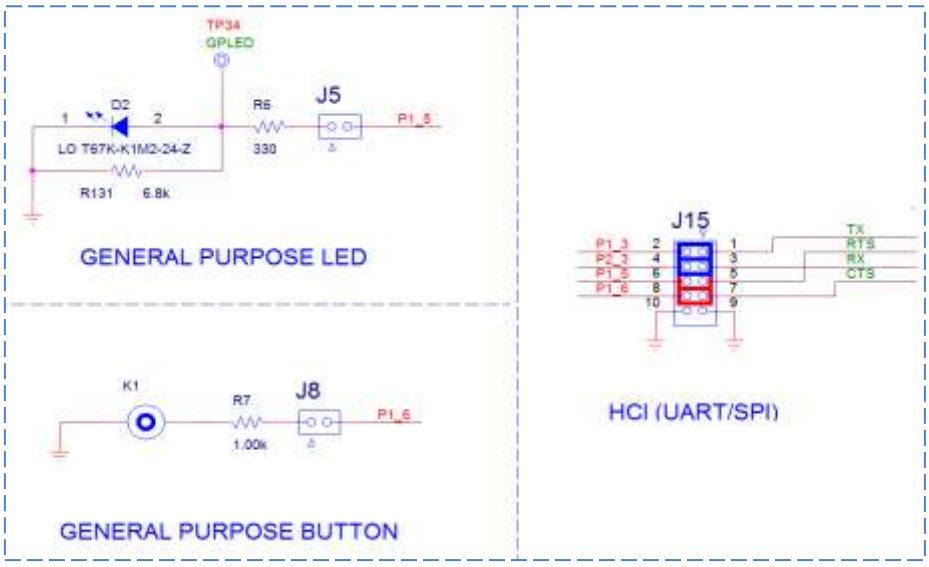

Figure 12: Full UART signals connectivity

Figure 13: Jumper's placement for Full UART functionality

5.3.6 USB HUB (U11)

USB HUB is implemented by U11, USB2512B. This chip is supplied with 3.3V from U13.

The signal PWR_ENABLE is generated from U11 and it is an active high signal. It enables the power components (LDOs and dc/dc converter), for UART, JTAG and current sensing circuit.

Operation is indicated via green LED D4. A 24MHz crystal (Y3) is required for the chip operation.

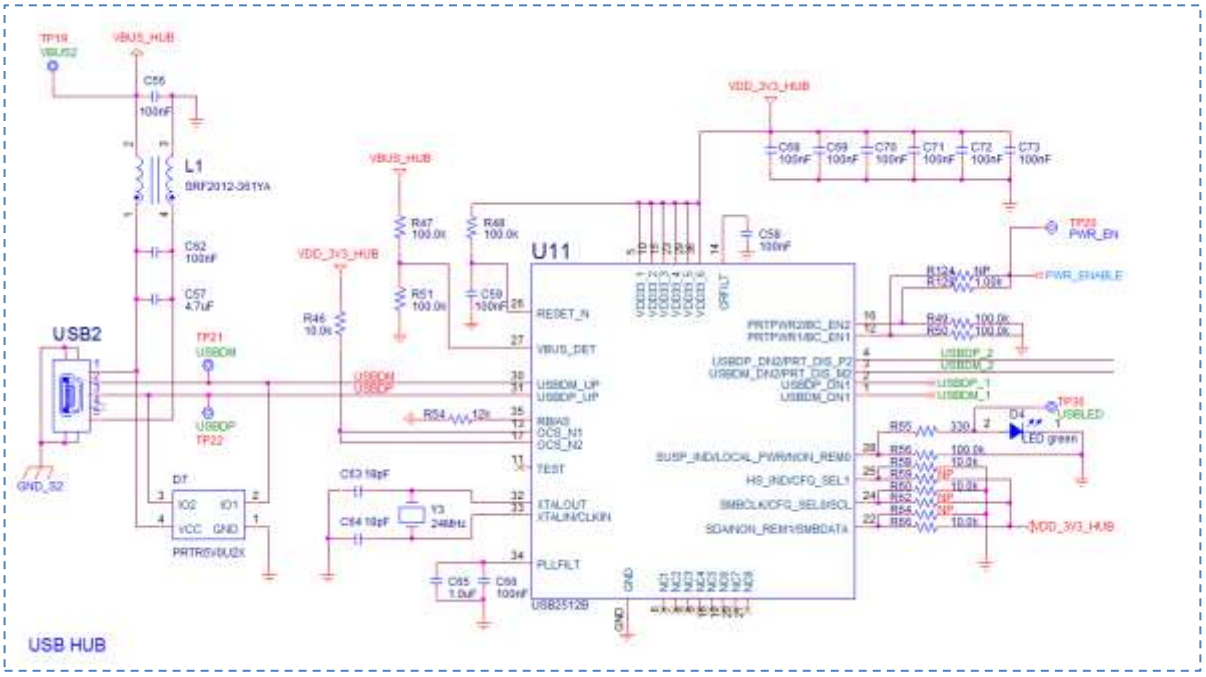

Figure 14: USB HUB circuitry

5.3.7 USB to UART (U12)

The USB to UART function is implemented by U12 FT2232HL.

Functions served by U12 are the following:

- Connectivity of PC to the DA1468x/DA1510x SoC UART port
- Connectivity of PC to current sense circuitry.
    - SPI connection with ADC (U8)
    - Software cursor triggering, (U_TRIG)
- Reset capability through T_RESET signal (***not enabled***)

The chip is supplied with a 3.3V from U14. A 12MHz crystal (Y4) is required for the chip operation.

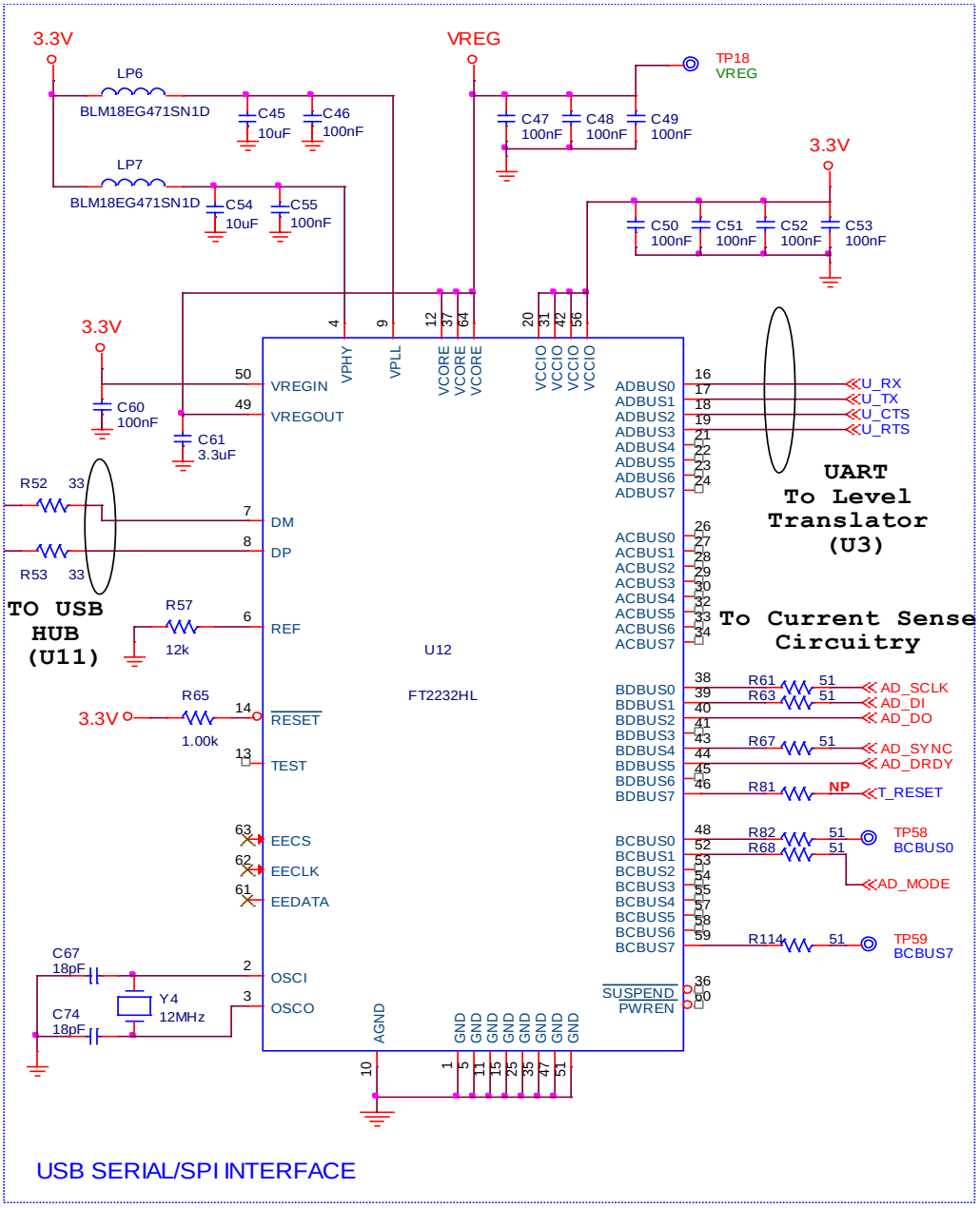

Figure 15: USB to UART (U12)

5.3.8 USB to JTAG (U4)

The USB to JTAG function is implemented by U4 SAM3U2CA. On the ROM of U4, software from Segger is loaded. Functions served by U4:

- Connectivity of PC to DA1468x/DA1510x JTAG port
- Reset capability through T_RESET signal

Operation is indicated via red LED D3.

This chip is supplied with a 3.3V from U14. U14 is enabled from PWR_ENABLE signal.

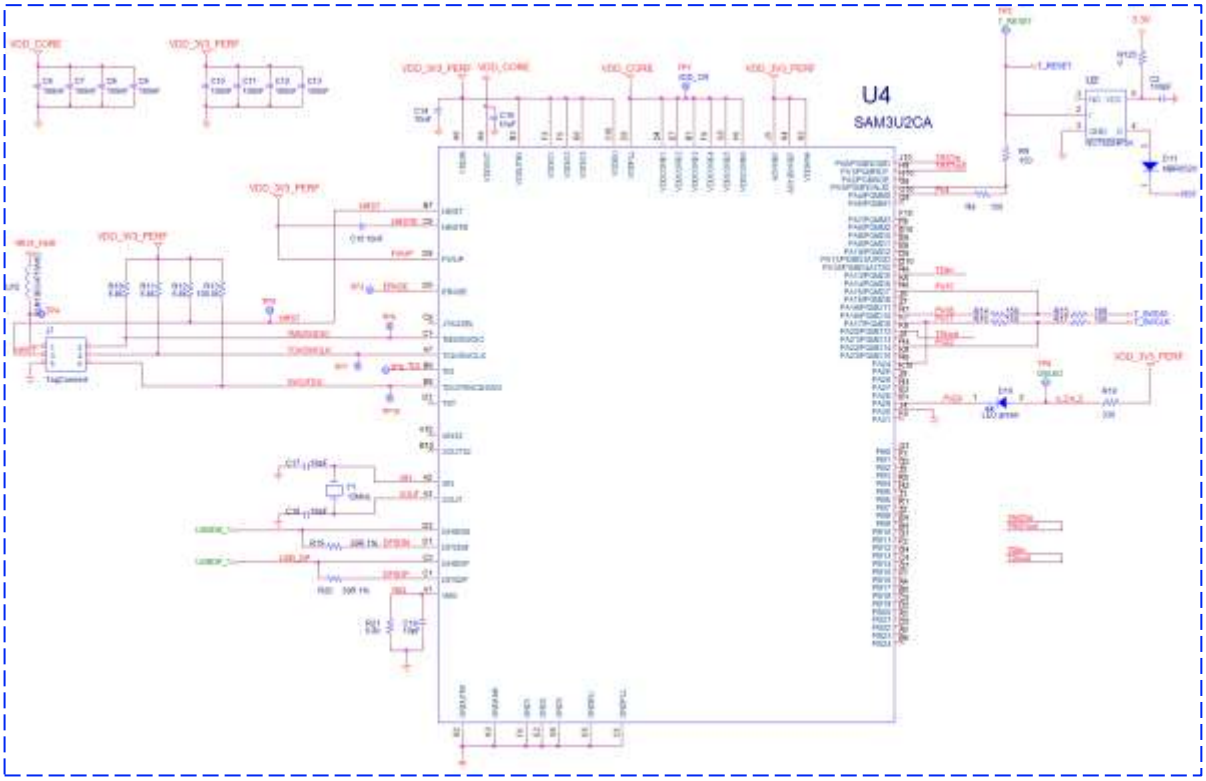

Figure 16: USB to JTAG (U4)

5.3.9 Push buttons and user controlled leds

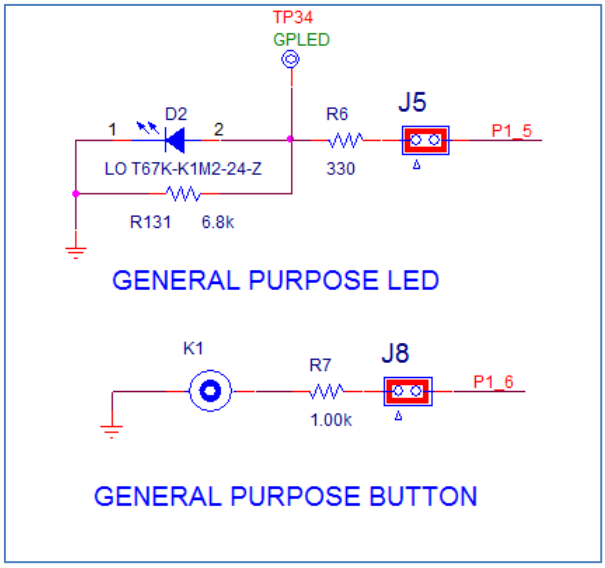

Figure 17: Push button and general purpose LED schematic

- K1 is connected to P1_6 through a jumper on header J15. Please notice that via header J13, P1_6 is also connected to CTS.
- K2 is connected to Reset line of SoC.
- D1 (White Led): driven from LED1. LED1 is controlled directly from the DA1468x/DA1510x SoC. LED1 is not available on the J3/J4 expanding headers.
- D2 (Orange Led): driven from P1_5 through header J14. Please notice that via header J13, P1_5 is connected also to RTS.

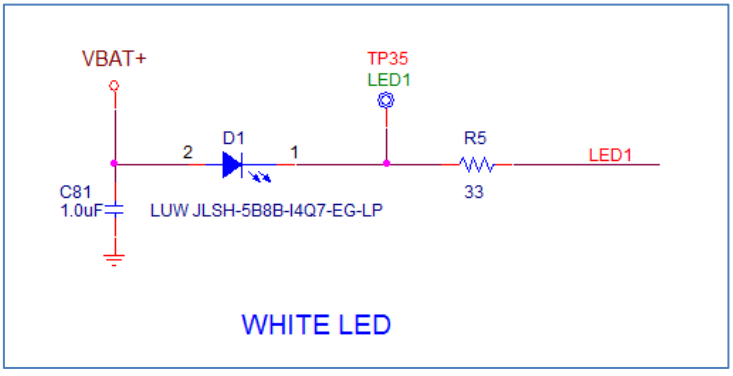

Figure 18: White LED

5.3.10 Current sense circuitry

The supply current to PRO daughterboard (AQFN60 or WLCSP53) is monitored and measured by the current sense circuitry. The current measurement samples are fed to PC through U4. The most important components:

- Current sense resistor (R20=2.37 Ω, 1%) : This adds a voltage drop to the voltage supplied to the system
- Opamp section (U6, U7, U9, U15, U16, and U17): The monitored voltage is amplified simultaneously by U6 and U9 with a gain of 10 and 5000 respectively. U19, accompanied by U15 and U16 decides which of the two measurements will be fed to Analog to Digital converter. In this way, a wide range, from very low currents (sub-micro range) to higher than 100mA can be measured

- Conversion to a Differential Analog output (U7): converts signal to differential over reference voltage and feeds this to the A/D converter (U8)
- Bleeding resistor (C100). This adds a small permanent leakage to aid in low-current accuracy. This leakage is subtracted automatically when using the PowerProfiler software

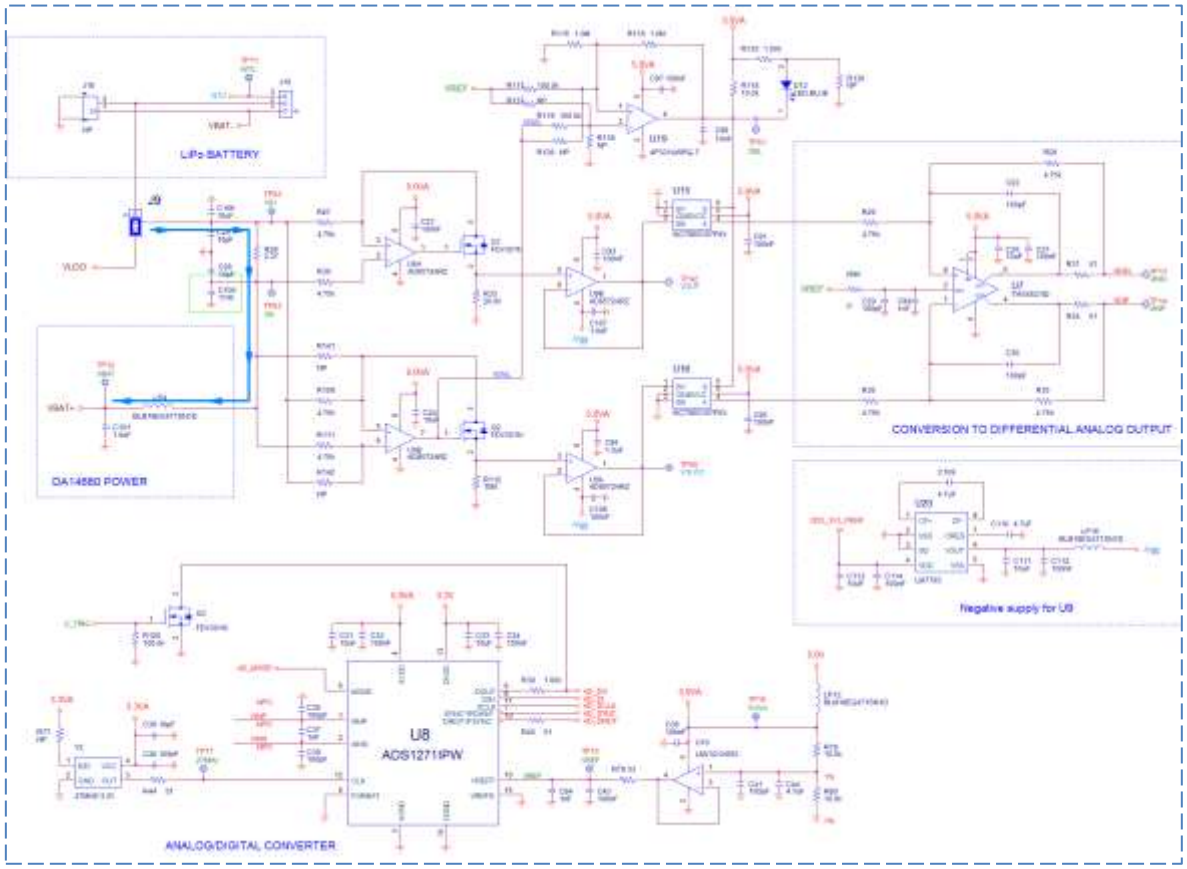

Figure 19: The current sense circuitry

5.4 Power section

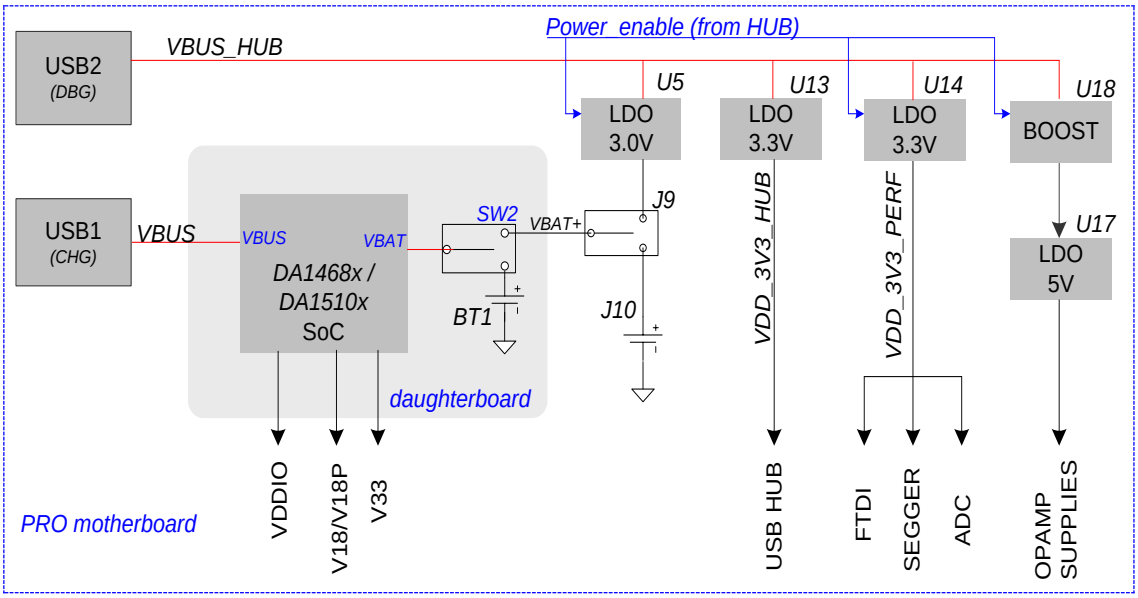

Figure 20: PRO development kit power components

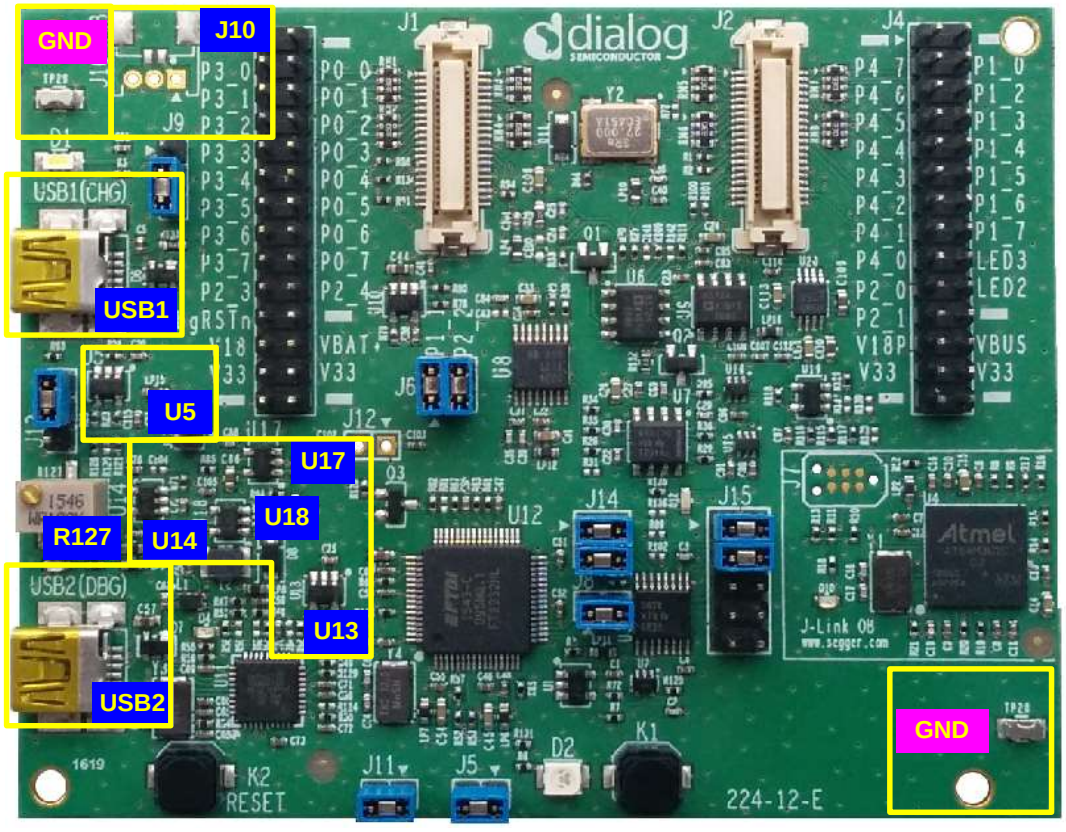

Figure 21: Power components location on PRO motherboard

The following power components are placed on the PRO motherboard:

USB1 (CHG): micro-USB connector. It is dedicated to the charger of DA1468x/DA1510x SoC. USB1 (CHG) does not supply any other circuit on the development kit.

USB2 (DBG): micro-USB connector. It is the evaluation and debugging port of the development kit. It provides the power and the data bus. If not connected, no debugging ports (UART, JTAG) or power consumption indications are available.

U13: 3.3V/LDO. It generates VDD_3V3_HUB voltage rail that supplies the USB HUB. If no USB cable plugged on USB2 (DBG) port, then the LDO is not enabled.

U5: 3.0V, 1.8V or adjustable / LDO. It generates VLDO voltage rail that supplies the DA1468x/DA1510x daughterboard. It is enabled from USB Hub, through PWR_ENABLE or by applying a jumper on **J17**. If no USB cable is plugged in USB2 (DBG) port, then the LDO is not enabled. For generating 1.8V, remove jumper on header J13. Finally, VLDO is adjusted from 1.9V to 4.3V through variable resistor R127 (shown in Figure 22).

By default VLDO generates 3.0V

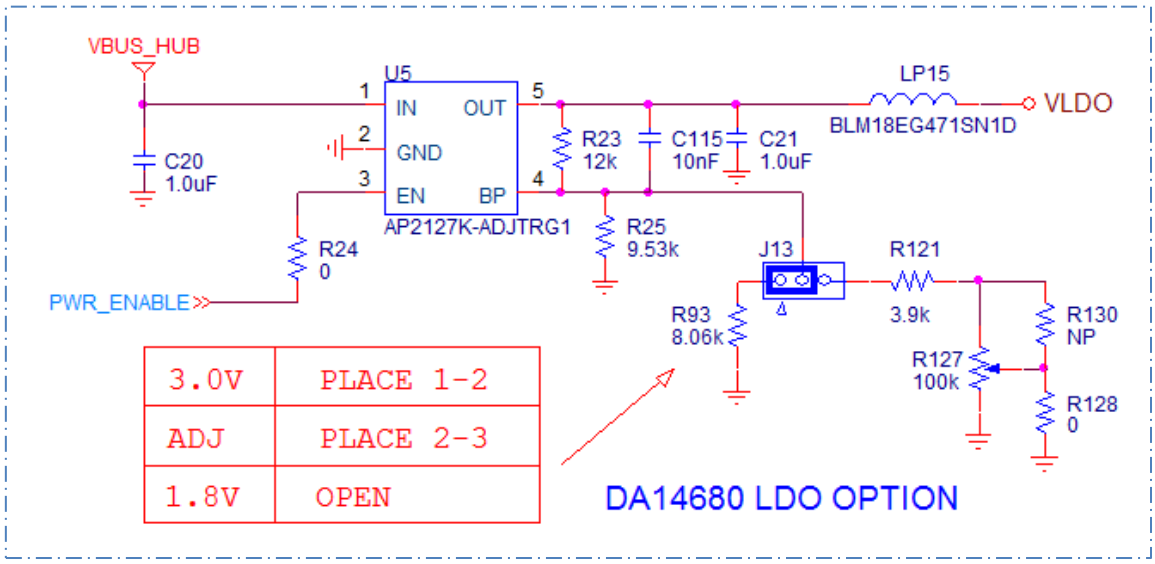

Figure 22: VLDO linear voltage regulator, supplied from USB2 (DBG)

U14: 3.3V/LDO. It generates VDD_3V3_PERF voltage rail that supplies the USB to UART transceiver (U12, FT2232L), the USB to JTAG chip (U4, SAM3U2CA/Segger) and the ADC (U8). It is enabled from USB Hub, through signal PWR_ENABLE or by placing a jumper on **J17**. If no USB cable plugged in USB2 (DBG) port, then the LDO is not enabled. Consequently the debugging circuit is not functional.

U18: 6V/BOOST and U17 5V/LDO. The two components are cascaded. The generated 5V drives the current sense circuitry (OPAMPs). If no USB cable plugged in USB2 (DBG) port, the 5V voltage rail LDO is not enabled. Consequently the current sense circuit is deactivated.

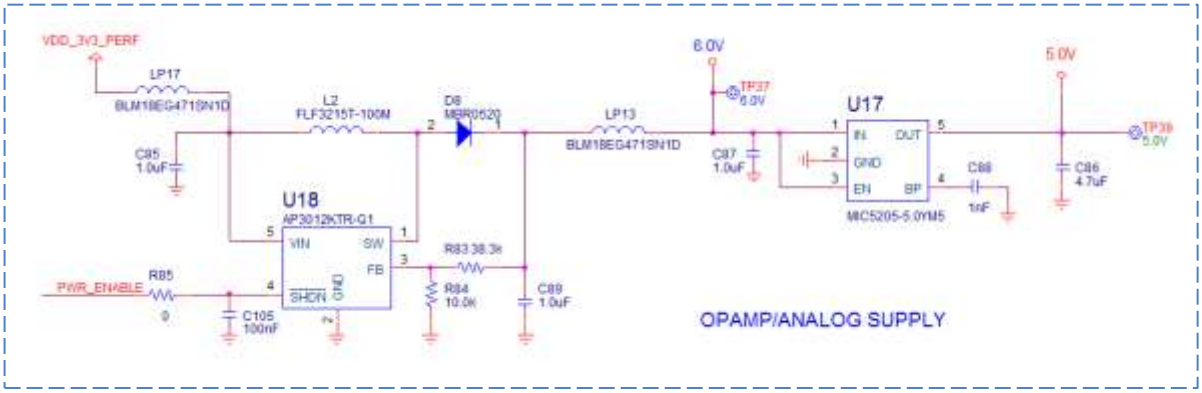

Figure 23 : OPAMP/Analog power supply

6 PRO-daughterboards

There are two daughterboards currently available:

- PRO AQFN60 daughterboard: 224-14-D
- PRO WLCSP53 daughterboard: 224-15-E

6.1 Overview of DA1468x/DA1510x daughterboards

The daughterboard is designed to be used in conjunction with the PRO motherboard. Figure 24 presents PRO AQFN60 board. The basic features of the daughterboards are:

SoC

DA1468x/DA1410x AQFN60 for PRO AQFN60 / *224-14-D*

DA1468x/DA1410x **WLCSP53** for PRO WLCSP53 / *224-15-E*

Flash Memory

- W25Q80EW (8Mbit) QSPI Flash Memory, WLCSP package - **default**
- W25Q16DW (16M-bit) QSPI Flash Memory, (not populated) - *optional*
- 1.8V power supply - **default**
- 3.0V power supply – optional
- Signals connected to the PRO-Motherboard through 0-ohm resistors

Clock Inputs

- 16MHz crystal
- 32KHz crystal

Two 40-pin expansion connectors

- DA14680 I/O pins as well as ground and power lines are brought out to two expansion connectors
- The expansion connectors are placed at bottom

Coin cell holder

- Compatible with a standard CR2032 coin cell battery

Power source selection

- Between PRO-Motherboard and coin cell battery

RF Interface

- SMD RF switch used for evaluation/ testing
- Integrated IFA antenna
- Matching network

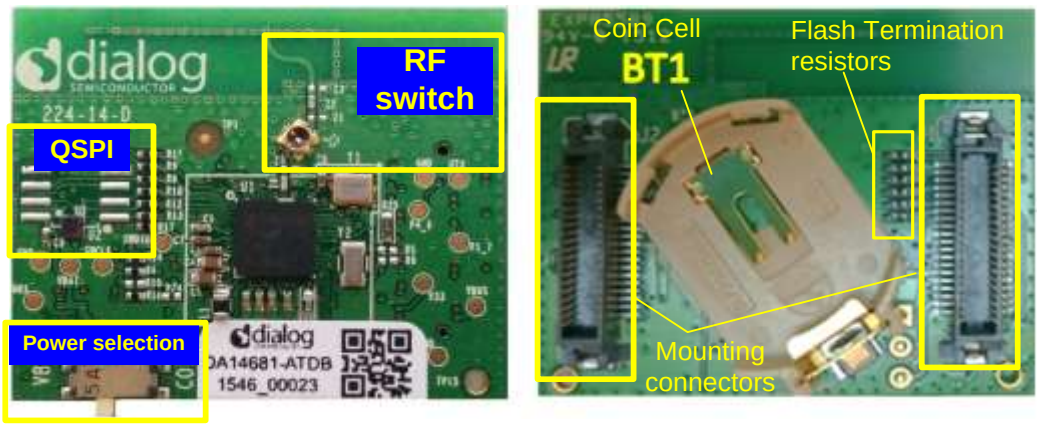

Figure 24: PRO AQFN60 daughterboard top view and bottom view

The daughterboard is plugged on top of the PRO motherboard via two low-profile 40-pin SMD connectors which are placed at the bottom side of the PCB. Daughterboard has a mount option for a coin cell battery holder. Power supply selection is available between the PRO-Motherboard and the coin cell battery through switch SW2. This allows the daughterboard to operate as a standalone device once programmed (Figure 24).

The daughterboard is also equipped with an external QSPI data flash from Winbond. The W25Q80EW flash supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2 clocks instruction cycle Quad Peripheral Interface (QPI), Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1(D0), I/O2 (/WP) and I/O3(/HOLD). A 0 Ohm resistor is placed in series with QSPI supply to allow measurements with the QSPI switched off. QSPI supply is selectable (V33 or V18) and the same supply voltage is connected to VDDIO on DA1468x/DA1510x (Figure 25). A network of 0 ohms termination resistors is placed in series with the QSPI bus to allow isolation of QSPI data flash from the rest of the system in case the flash is not used (Figure 26).

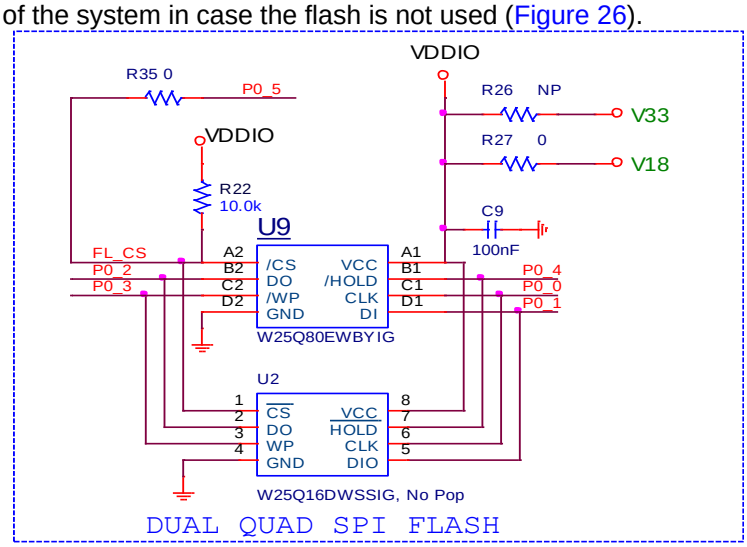

Figure 25: QSPI Data Flash V33 or V18 Selectable Power Supply

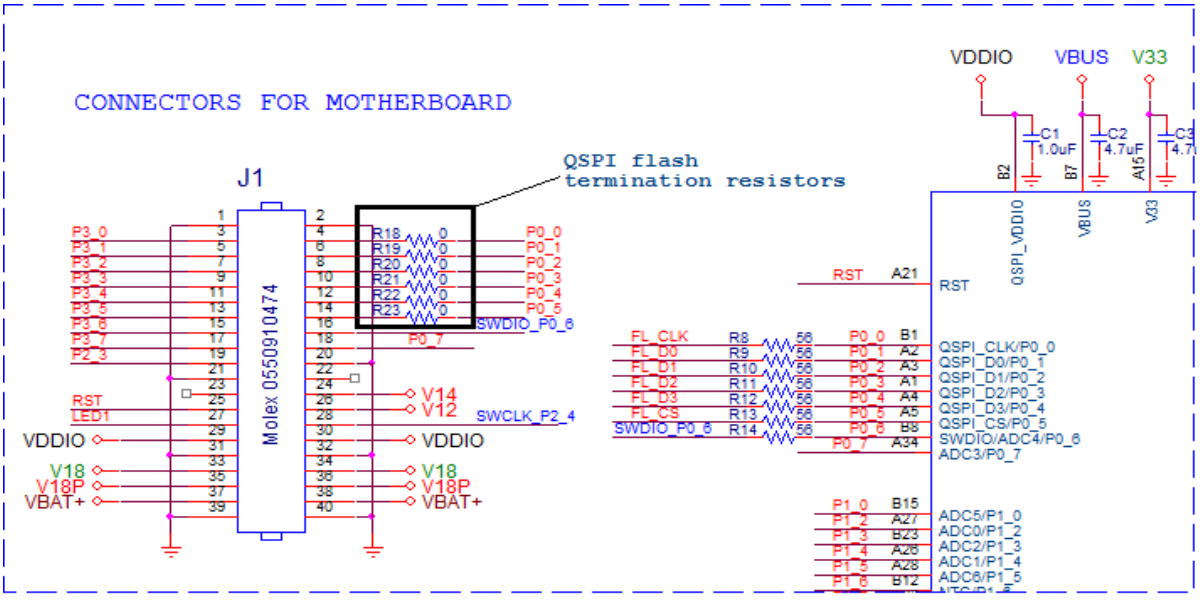

Figure 26: QSPI Data Flash 0 Ohms termination resistors

The daughterboard provides an SMD RF switch and an integrated printed IFA antenna. The SMD RF switch is used for RF evaluation/testing. The RF switch is MM8130-2600 supplied by Murata. Verification of the circuit performance is accomplished by simply inserting an external plug in the

board mounted receptacle. This action re-directs the circuit from normal condition to the plug side. Removing the plug restores circuit back to its normal condition. Murata offers several options for mating plugs, MXHS83QH3000 is such an option[1].

[1] *It is in preproduction phase and can be supplied from particular suppliers*

6.2 Pin assignments

The pin assignment of the two 40-pin connectors to the WLCSP/AQFN SoC can be seen below:

Table 6: Connector J1 pin assignment to WLSP/AQFN SoC

Connector Pin Number	Signal Name	WLCSP Pin Assignment	AQFN Pin Assignment	Comments
1, 2	GND			
3	P3_0		A37	
4	P0_0	B8	B1	FL_CLK
5	P3_1		A12	
6	P0_1	A7	A2	FL_D0
7	P3_2		A10	
8	P0_2	B7	A3	FL_D1
9	P3_3		A7	
10	P0_3	A8	A1	FL_D2
11	P3_4		A9	
12	P0_4	C8	A4	FL_D3
13	P3_5		A20	
14	P0_5	C7	A5	FL_CS
15	P3_6		A22	
16	P0_6	F4	B8	SWDIO
17	P3_7		B14	
18	P0_7	A6	A34	
19	P2_3	B5	A35	RX
20, 21	GND			
22, 23	-			
24	V14			
25	RST	G1	A21	
26	V12			
27	LED1	G2		
28	P2_4	F5	A14	SWCLK
29. 30	VDDIO			
31, 32	GND			
33, 34	V18			
35, 36	V18+			
37, 38	VBAT+			
39, 40	GND			

Table 7: Connector J2 pin assignment to WLSP/AQFN SoC

Connector Pin Number	Signal Name	WLCSP Pin Assignment	AQFN Pin Assignment	Comments
1, 2	GND			
3	P4_7		A36	GPIO
4	P1_0	C2	B15	***ML8511_OUT (analog in)***
5	P4_6		B22	GPIO
6	P1_2	C1	A27	I2C_SDA
7	P4_5		A33	GPIO
8	P1_3	B6	B23	TX
9	P4_4		A32	GPIO
10	P1_4	D1	A26	***PDM_DATA***
11	P4_3		A31	GPIO
12	P1_5	B2	A28	***RTS(out)/LED***
13	P4_2		B17	GPIO
14	P1_6	E2	B12	***CTS(in)/BUTTON***
15	P4_1		B16	SPI_CS
16	P1_7	D2	A25	PDM_CLK
17	P4_0		A24	GPIO
18, 19	-			
20, 21	GND			
22	LED2		A19	
23	P2_0	E1	A23	Xtal32p
24	LED3		B11	
25	P2_1	F1	B13	Xtal32n
26	GND			
27	VBAT-			
28	VBAT-			
29, 30	GND			
31	P1_1	F3	A17	USBN
32	-			
33	P2_2	G3	A16	USBP
34	-			
35, 36	GND			
37, 38	V33			
39. 40	VBUS			

6.3 Booting from UART

There is only one bootloader option for booting from UART is the indicated pins pair P1_3 and P2_3. Please notice that booting does not use UART handshaking. Default settings for booting:

- 57.6KBaud
- 8 bits
- No Parity
- 1 –stop bit

6.4 Crystals

Table 8: Y1, 16MHz, Crystal characteristics

Reference Designator	Value
Part Number	7M-16.000MEEQ-T
Frequency	16MHz
Accuracy	±10ppm
Load Capacitance (C_L)	10pF
Shunt Capacitance (C_0)	3pF
Equivalent Series Resistance (ESR)	100 Ω
Drive Level (P_D)	50µW

Table 9: Y2, 32 KHz, Crystal characteristics

Reference designator	value
Part Number	ABS07-32.768KHZ-7-T
Frequency	32.768KHZ
Accuracy	±20ppm
Load Capacitance (C_L)	7pF
Shunt Capacitance (C_0)	0.9 ~ 1.2pF
Equivalent Series Resistance (ESR)	70 KΩ
Drive Level (P_D)	0.5µW

6.5 Battery Options

There are two different battery types that can be used in conjunction with the pro daughterboard:

- A coin cell battery (rechargeable or non-rechargeable)
- A rechargeable Li-Po battery

Figure 27: Typical CR2032 (non-rechargeable) coin cell battery

This battery is placed at the bottom of the daughterboard in the dedicated battery holder as shown in Figure 34. The battery needs to be inserted by sliding in first the part that will fit inside the metallic clip of the battery holder.
However, extra attention is needed when removing the coin cell battery from its holder, if this is not done properly then the plastic battery holder can be subject to breaking.
The recommended way of removing the coin cell battery is shown at Figure 28.

Figure 28: Recommended way of removing the coin cell battery from the battery holder

A slotted screwdriver needs to be inserted at the point shown in Figure 28 between the metallic clip of the battery holder and the coin cell battery itself, then by lifting the screwdriver up the coin cell battery will pop out without damaging the plastic surroundings of the battery holder.

A rechargeable battery can also be used by following the procedure described at section 6.7.

A 3x1 through-hole male header (J10) or a two pins JST-PH Series header (J18) can be soldered on PRO-Motherboard for connecting the Li-Po battery.

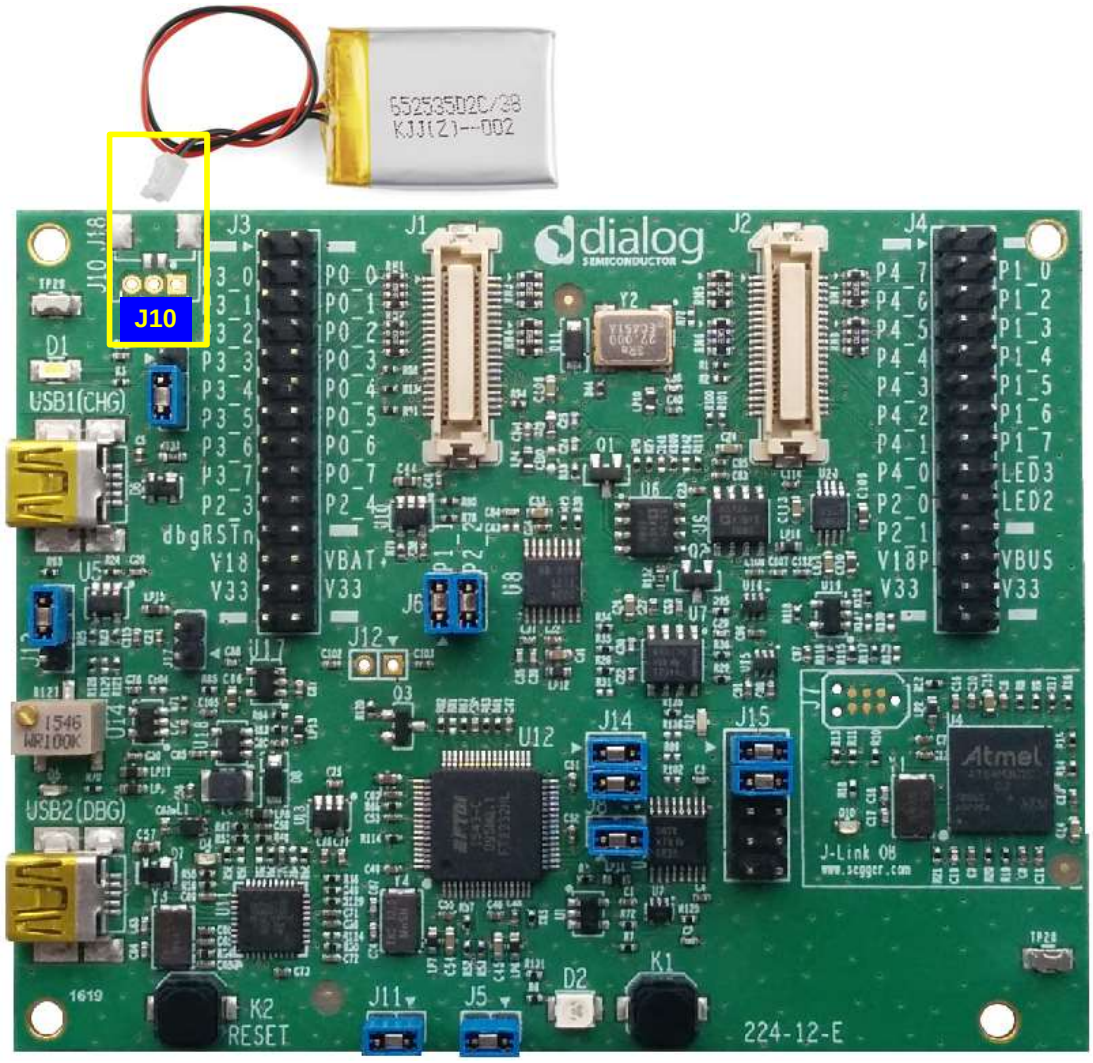

Figure 29: Connection of the Li-Po battery

6.6 Switch SW2 Settings

Same settings are applied for the two daughterboards (WLCSP and AQFN).

Switch SW2:
Move switch to indication COIN for coin cell battery selection

Move switch to indication VBAT for power supply selection

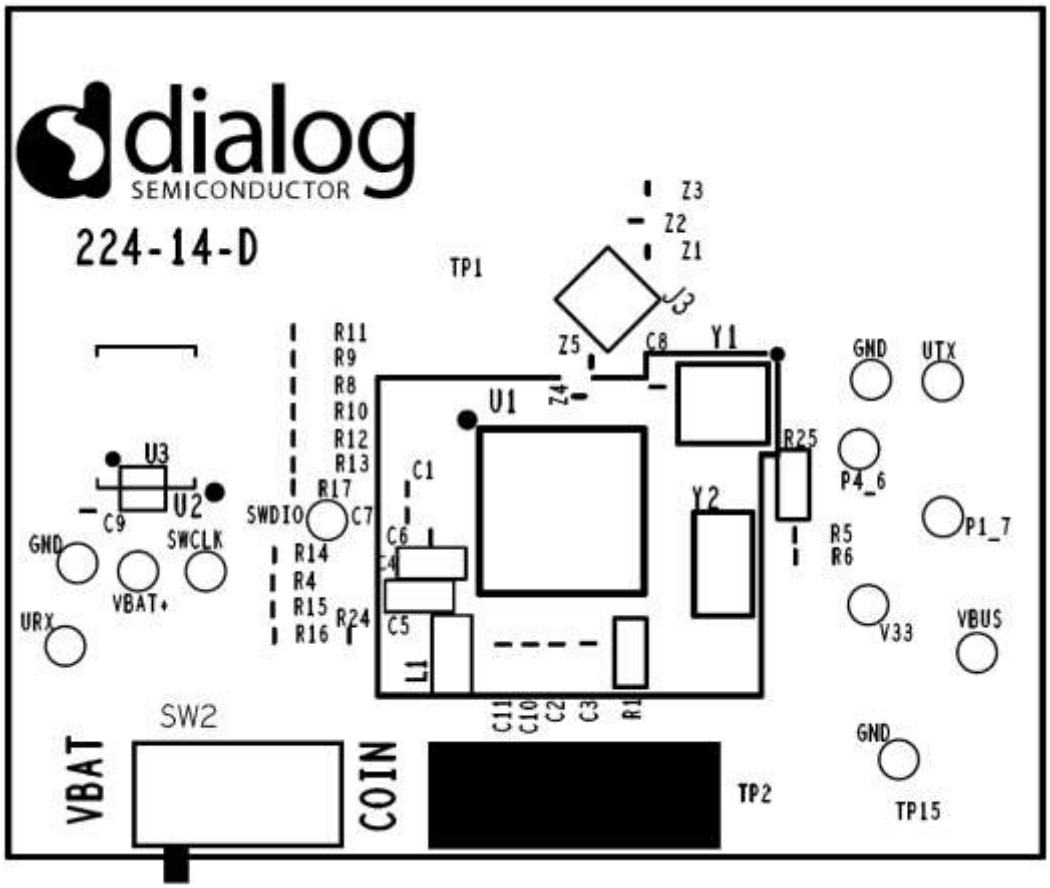

Figure 30: DA1468x_AQFN_vD Daughterboard switch SW2 Setting

6.7 DA1468x / DA1510x daughterboard power supply options

USB1 port/charger input (USB1/CHG): the SoC VBUS pin is supplied directly from the USB port. Please notice that on this Pro Kit, only the DA1468x/DA1510x SoC is supplied from this port. J6 connects the USB port pins to USBN (P1_1/J2.31) and USBP (P2_2/J2.33). Before hardware Rev.E1 a value of 33 ohm was used for the USB termination resistors in series with the USB signals, in the latest Rev.E1 these have been replaced with 0 ohm for improved compatibility with certain USB host controllers and USB cables. It is advised for customers having a Rev.E board to replace the USB termination resistors (R100, R101 which are located near J2) with 0 ohm.

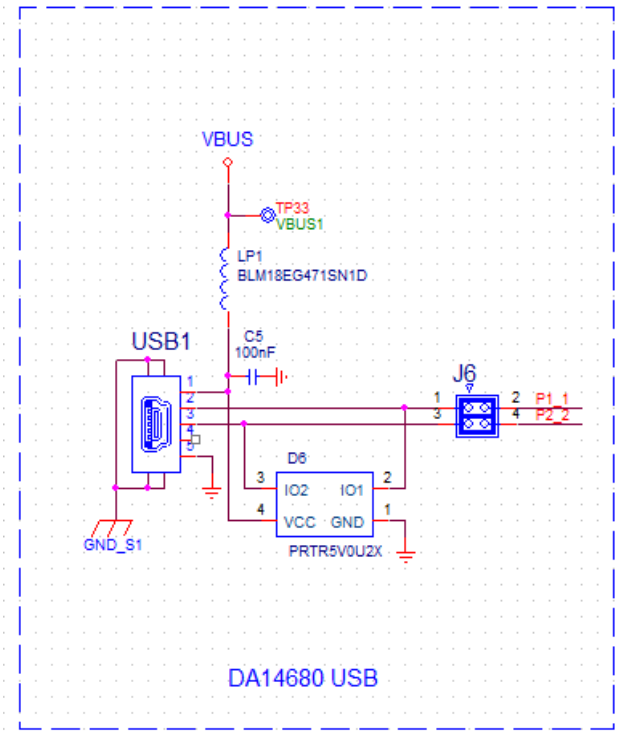

Figure 31: USB1 (CHG) port

For enabling this option:

:: Plug USB cable in the USB1(CHG)

Notice Avoid having a *non-rechargeable* coin cell battery plugged on daughterboard. In case that a *non-rechargeable* coin cell battery is plugged on daughterboard, ensure that switch SW2 on **daughterboard**, is located on COIN indication making sure that the charger is not enabled

1. Li-Poly battery: a dedicated header (J10) on motherboard is used for connecting the Li-Poly battery. For enabling this option please follow the procedure below:
   :: On **daughterboard** move switch SW2 to VBAT indication
   :: Place jumper on header J9, bridging positions 1 -2 (this is not the default setting for J9)
   :: Connect a Li-Poly battery on header J10
   :: For using it with the charger , plug a USB cable in the USB1(CHG)

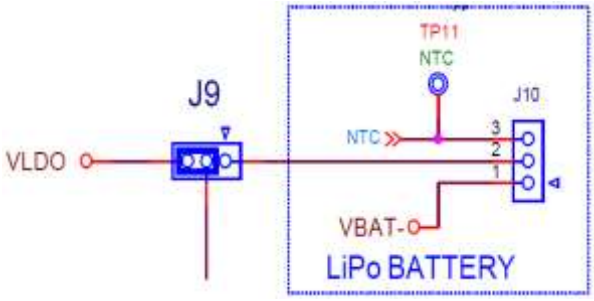

Figure 32: LiPoly battery connection diagram

Please notice that by connecting USB1 (CHG) port ***only***, JTAG, UART and current sensing circuits are both deactivated. Notice that unless battery has overcharge protection, NTC must be enabled.

NTC is enabled by populating resistors R89 and R102 and make use of a proper software.

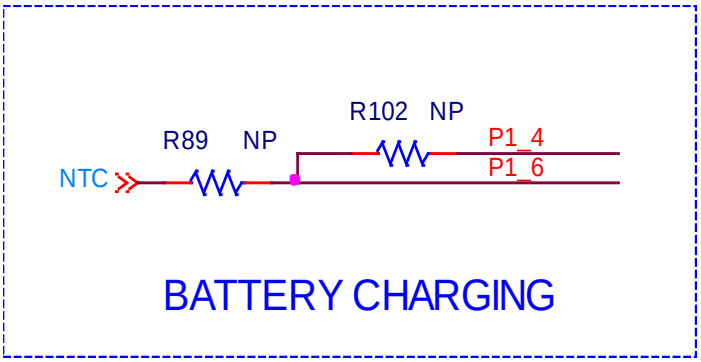

Figure 33: For enabling NTC hardware option

2. Coin cell battery: is located on the daughterboard and is placed on the socket existed on the bottom side of the daughterboard (BT1). Coin cell battery is connected to VBAT1 and VBAT2 pins of DA1468x/DA1510x via switch SW2 on daughterboard. For enabling the coin cell battery, please proceed as following:
   - On **daughterboard** move switch SW2 to COIN indication
   - For not rechargeable batteries, do not enable the Charger (by not plugging USB charger on the USB1(CHG))

VBAT+ voltage rail is isolated from the coin cell battery.

The coin cell battery is a 2032 type. It can be either rechargeable or non-rechargeable battery type. In case that a non-rechargeable coin cell battery is used, **do not** use the battery charger.

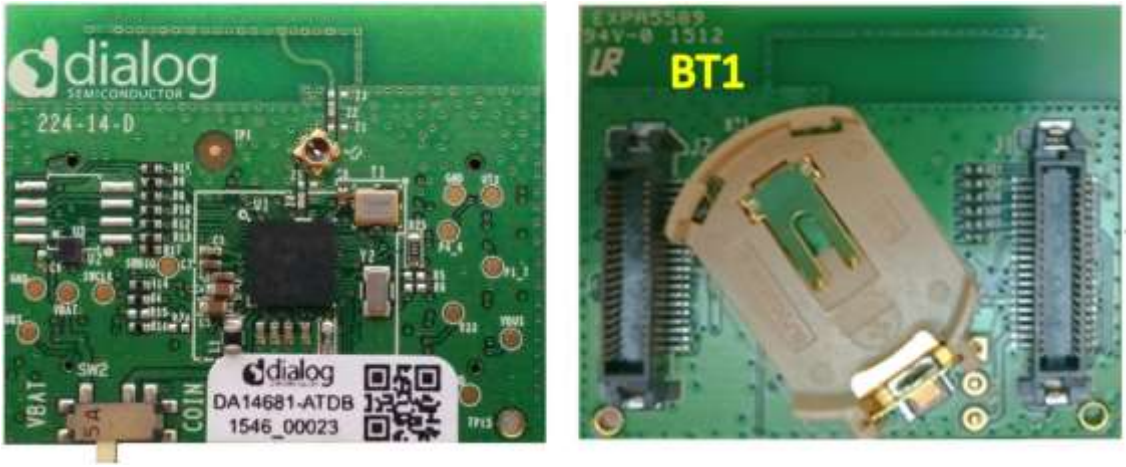

Figure 34: DA1468x/DA1510x daughterboard power source selection

3. USB2 (DBG), through LDO 3.0V - **default**

   The VLDO (=3.0V) voltage rail, is connected to VBAT+ via header J9.

   For enabling the power supplying from VLDO (U5), proceed as following:

   :: Ensure that a jumper is placed on header J13.
   :: On **daughterboard** move switch SW2 to VBAT indication
   :: Place jumper on header J9, on positions 2-3
   :: Plug a USB cable on the USB2 (DBG) port.

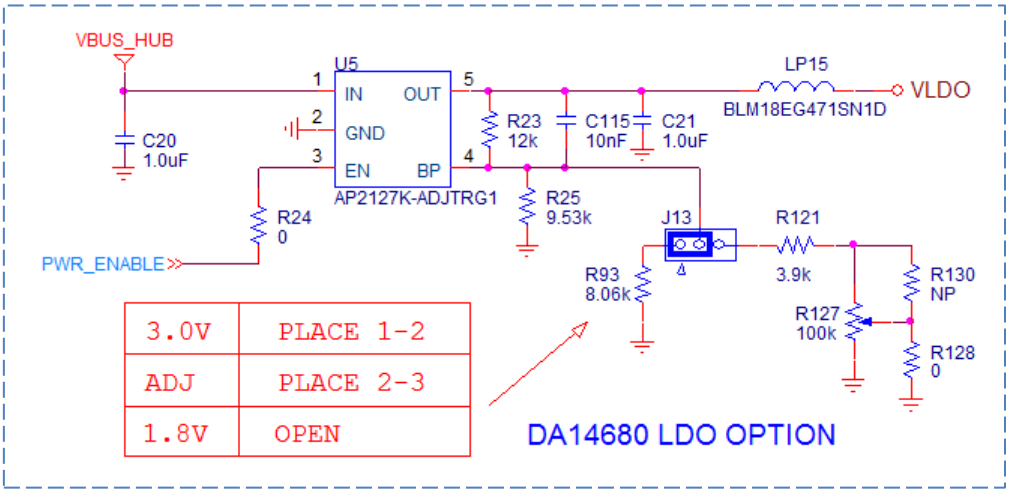

Figure 35: VLDO (=3.0V) Power supply to RPO AQFN/WLCSP daughterboards

7 Known Limitations

7.1 Development Kit operation with only USB1 is connected

7.1.1 Reset (older versions)

In older hardware versions of the PRO-Motherboard, before the current rev.E, the operation of Reset function through push button K2 can't be performed.

7.1.2 Charging a "0V Li-Poly battery"

Several types of Li-Poly battery are equipped with a protection circuit. The circuit protects batteries from deep discharging, by disconnecting them from the circuit. On this state, battery presents 0V across its terminals.

Charging a 0V Li-Poly battery when only USB1 is connected (USB2 is not connected) might not operate, due to leakages from DA1468x/DA1510x daughterboard to debugging section of PRO-Motherboard. This can be avoided by removing jumpers J11, J14 and J15.

7.1.3 Coin Cell Battery

Coin cell battery is applied on DA1468x/DA1510x daughterboard and it is of 2032 type. In case that a non-rechargeable coin cell battery is used, **do not** connect USB1 unless you have ensured that the battery charger is not enabled in the firmware.

7.1.4 Current measurements

When USB1 power is connected, power consumption measurement is not possible because the current on VBAT+ pin becomes either negative (when charging) or zero (when idle).

7.2 RF performance degradation in certain RF channels

7.2.1 RF-VCO related degradation

A loss up to 1dB in receive sensitivity can be randomly seen in channels 7,15,23,31 and 37, due to RF VCO leakage on harmonics of the system clock (16MHz).

7.2.2 RF degradation on CH14

A loss up to 1dB in receive sensitivity can be observed in channel 14, due to digital noise originating from the 27MHz oscillator on the PRO-Motherboard (the clock for the ADC converter in the current measurement circuit).

7.3 Current measurement circuit limitations

7.3.1 Measuring below 1.9V

When operating DA1468x/DA1510x daughterboards with VBAT ≤ 1.9V, the power management of SoC switches to bypass mode. In this case, a "smoothing" effect is observed on the measured current waveforms. To avoid this, it is recommended to place additional jumpers on J3/J4, shorting together V18/V18P/VBAT+/V33.

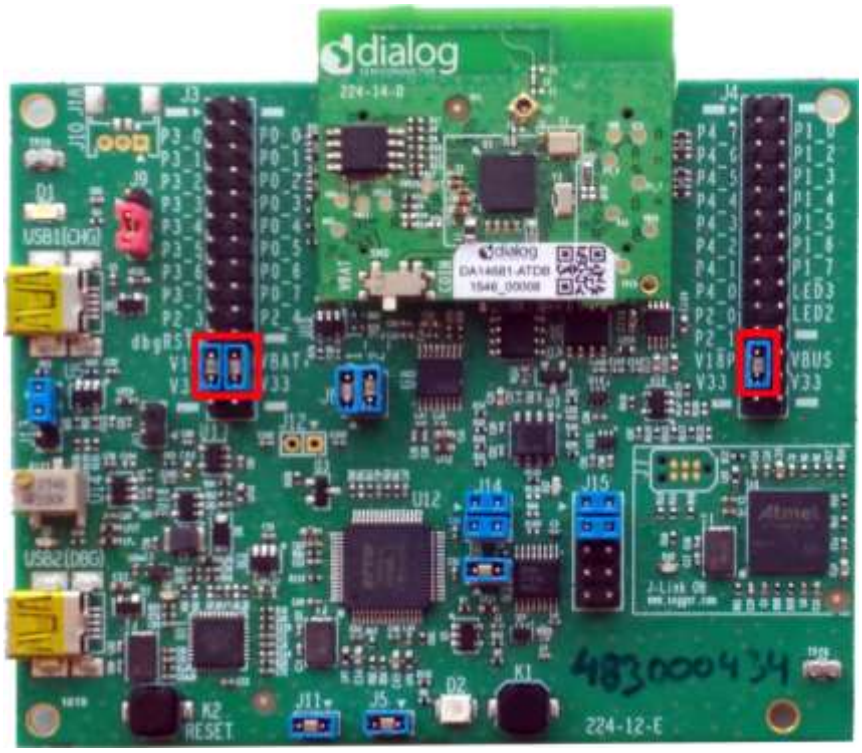

Figure 36 Shorting jumpers for lower VBAT

7.3.2 Full-scale measurement is voltage-depended

The full scale current for voltages (VBAT) higher than 2.5V is 250mA. For voltages 2.5V to 1.7V, the full scale is proportionally reduced. For example, for 2.1V and 1.8V supply the maximum current we can measure is 210mA and 180mA respectively.

7.3.3 Voltage drop due to series resistance

The current sense resistor (2.37Ω) plus the additional resistance of PCB tracks creates a significant voltage drop for large currents. Keep this in mind when measuring systems that handle currents larger than the typical 20-30mA.

7.3.4 Calibration

A simple calibration procedure should be applied in the PowerProfiler software for each PRO-Motherboard, for optimum performance. The steps are:

- Set calibration offset on Power Profiler configuration to zero.
- Remove the daughterboard and any other load that may be connected to VBAT+ (on J3)
- Measure the current for a short period, e.g. 1 second
- Place the measured average value on the related Config setting “Calibration Offset (mA)”, while negating the sign
- Measuring again should return an average value very close to zero

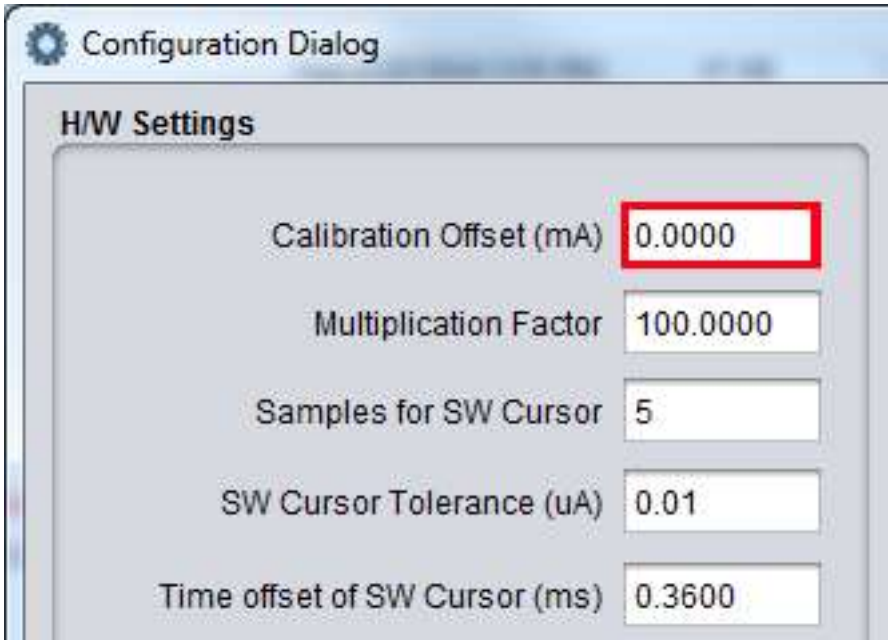

Figure 37 PowerProfiler Calibration Offset

Please note that the calibration value depends on the voltage level of VBAT+, so repeat the procedure after changing the voltage to a different value.

If the current needs to be measured with external ampere-meter or power source, the instrument should be nulled, using a similar procedure.

7.3.5 Fixed offset current (bleeding resistor)

A resistor was added on VBAT+, in place of the unpopulated capacitor C100. This adds a small fixed leakage, which improves the accuracy when measuring very low currents (below 10μA). In order to obtain this accuracy, the offset on PowerProfiler just needs to be calibrated, as described in sd.

As the fixed leakage current depends on the supply voltage (VBAT), for the default 3.0V, it is approximately equal to 17.24μA.

7.3.6 Leakage when the system is powered only from VBAT

In case that a daughterboard runs on a battery or external supply and it is plugged on the PRO-Motherboard while the PRO-Motherboard itself is not powered, a leakage of the order of 1.5mA can be measured.

8 Appendix A: Revision history

8.1 PRO-Motherboard

Table 10: PRO Motherboard revision history

Version	Comments
B00	Initial Release
B01	Changed R72, R79 to 33 ohm Changed R121 to 3.9k Changed R112, R113 to 10M Changed R128 to 0 ohm
C00	Added space for version control label
C01	Changed LP1 to 0.56 ohm resistor
D00	Optimizations on the current measurement circuit Changed reset button logic (so that it will work independent from the presence of power in the support circuits) Added D11 in series with RST (avoid leakage on RESET pressing) Added U20 (negative bias for U9)
D01	Changed R119 to 100k Changed R118 to 10k Changed C43 to 100nF Changed C43 to 100nF
E00	Added option for battery charging analysis (not populated) Added D12 (blue LED sleep/awake status) Changed TP28, TP29 to 1206 probe pins (cost reduction) Modified power input of U18 to VDD_3V3_PERF Added C115, LDO FC cap Added R134,TP64 (option for future expansion) Added J18 (option for battery connector) Modified power input of U20 to VDD_3V3_PERF Changed LP1 part reference to R133 Changed R71 to 10k Changed R85 to 0 ohm

8.2 PRO- AQFN Daughterboard (DA1510x/DA14680x_ DB_AQFN_vD)

Table 11: PRO-AQFN daughterboard revision history

Version	Comments
A	Initial Release
B	Add R24=2.2K for V14 rail power at power up Change value of C4 to 10uF Replace SW2 pin header connector with slide switch CUS-12TB Replace J3 RF Switch with Murata MM8130-2600 Add second choice for QSPI FLASH , U3, W25Q80EW Replace L1 part number (L2012 , lower DC Resistance) Change C8 from 1uF to 4.7uF Change C3 from 10uF to 4.7uF Connect R24 to V18 instead of VDDIO Change pin assignment for UTX (P1_3) URX (P2_3)
C	Add Resistor R25=10MOhm to XTAL32Kp Make Resistor R24=2.2K NP Make W25Q80EW populated
D	Modify silkscreen to add label

Please notice that revC and revD are functionally identical. Only difference is marking.

8.3 PRO- WLCSP Daughterboard (DA1510x/ DA14680x_DB_WLCSP_vE)

Table 12: PRO-WLCSP daughterboard revision history

Version	Comments
A	Initial Release
B	Add R24=2.2K for V14 rail power at power up Change value of C4 to 10uF Replace SW2 pin header connector with slide switch CUS-12TB Replace J3 RF Switch with Murata MM8130-2600 Add second choice for QSPI FLASH , U3, W25Q80EW Change C8 from 1uF to 4.7uF Replace L1 part number (L2012 , lower DC Resistance)
C	Connect R24 to V18 instead of VDDIO Change pin assignment for UTX (P1_3) URX (P2_3)
D	Add Resistor R25=10MOhm to XTAL32Kp Make Resistor R24=2.2K NP Make W25Q80EW populated
E	Modify silkscreen for label

Please notice that revD and revE are functionally identical. Only difference is marking.

9 Appendix B: Schematic and pcb silkscreen

9.1 PRO Motherboard Schematics and pcb silkscreen

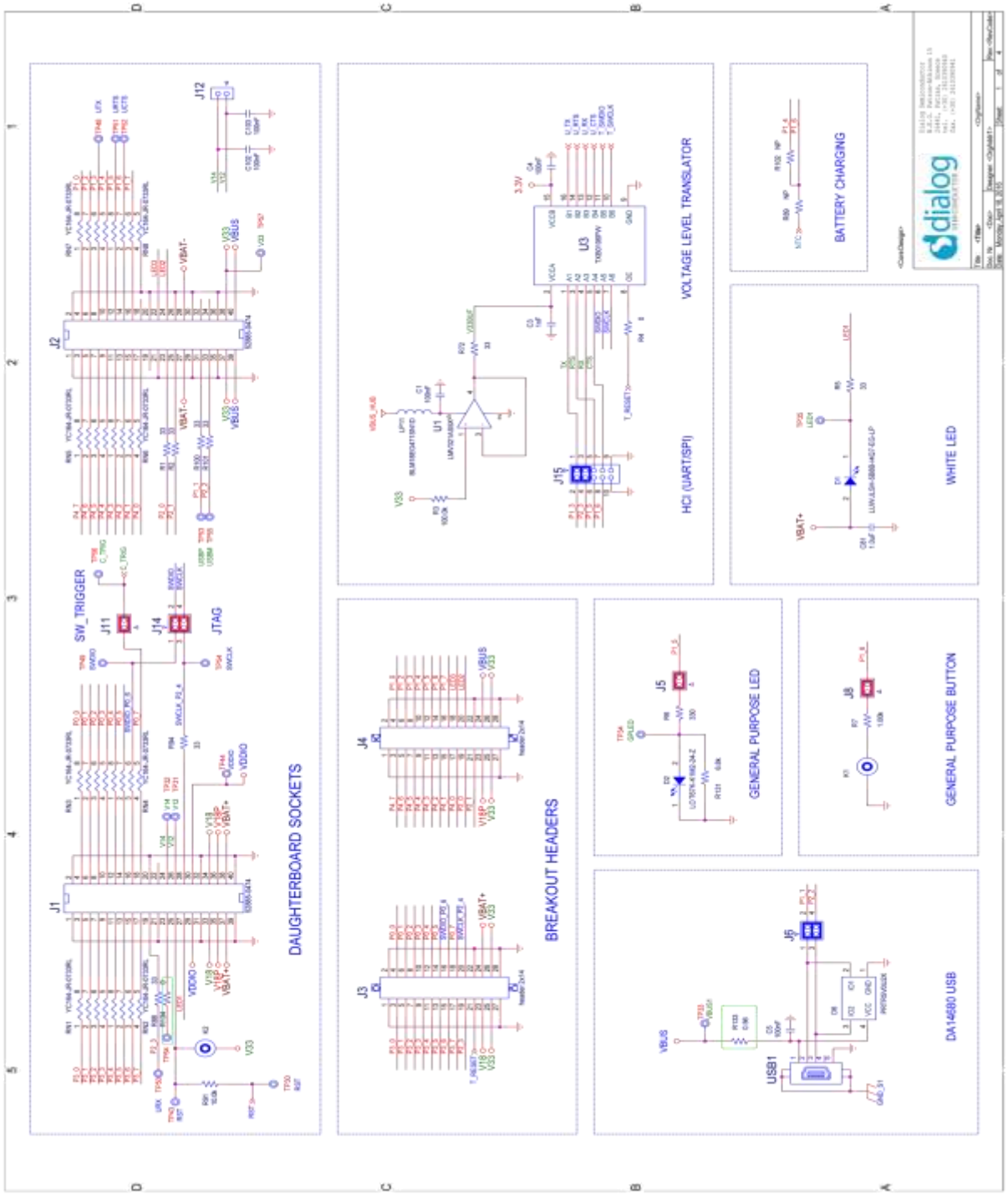

Figure 38: PRO motherboard, interconnection to PRO daughterboard

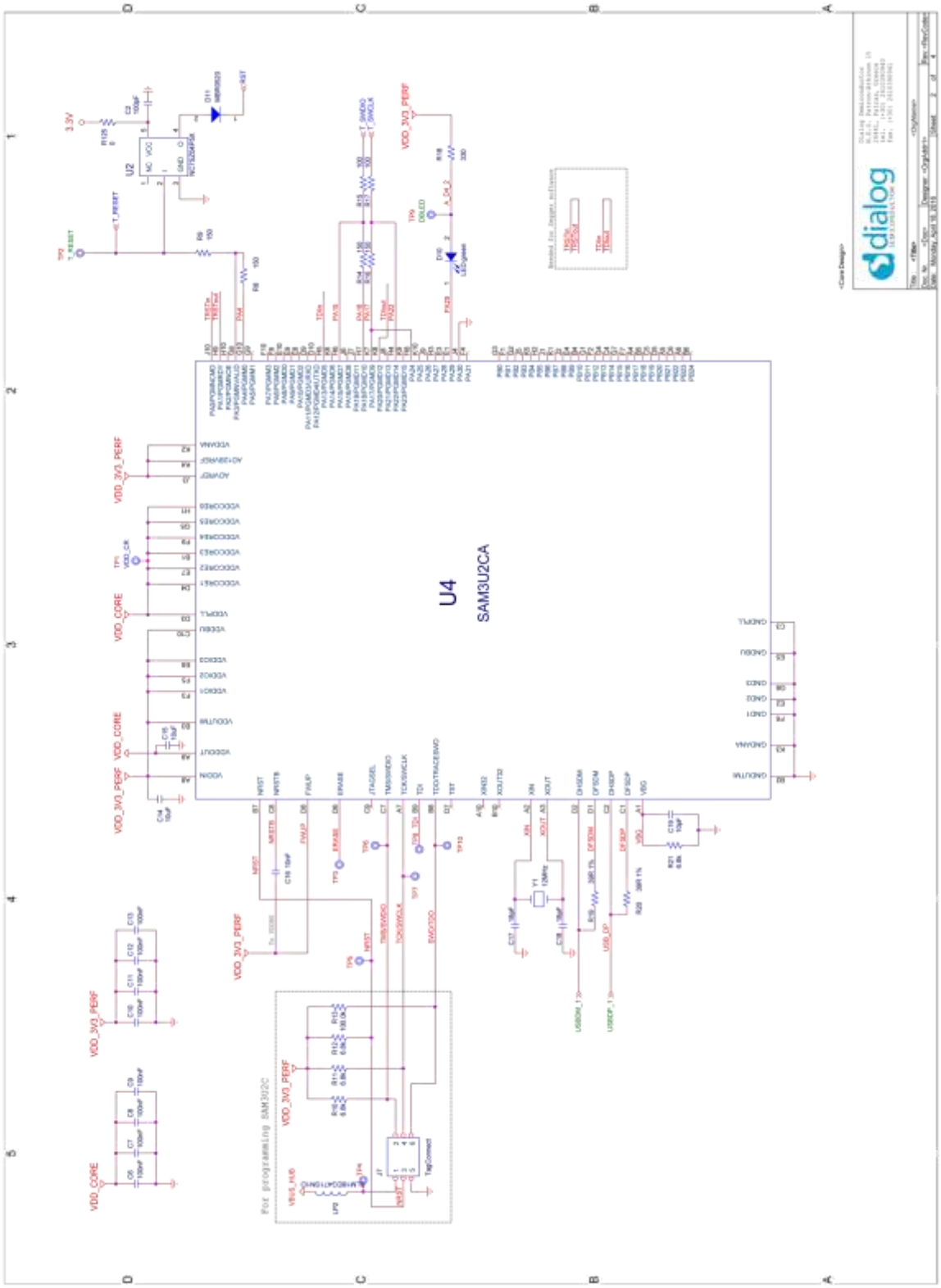

Figure 39: PRO motherboard, Segger ON J-link

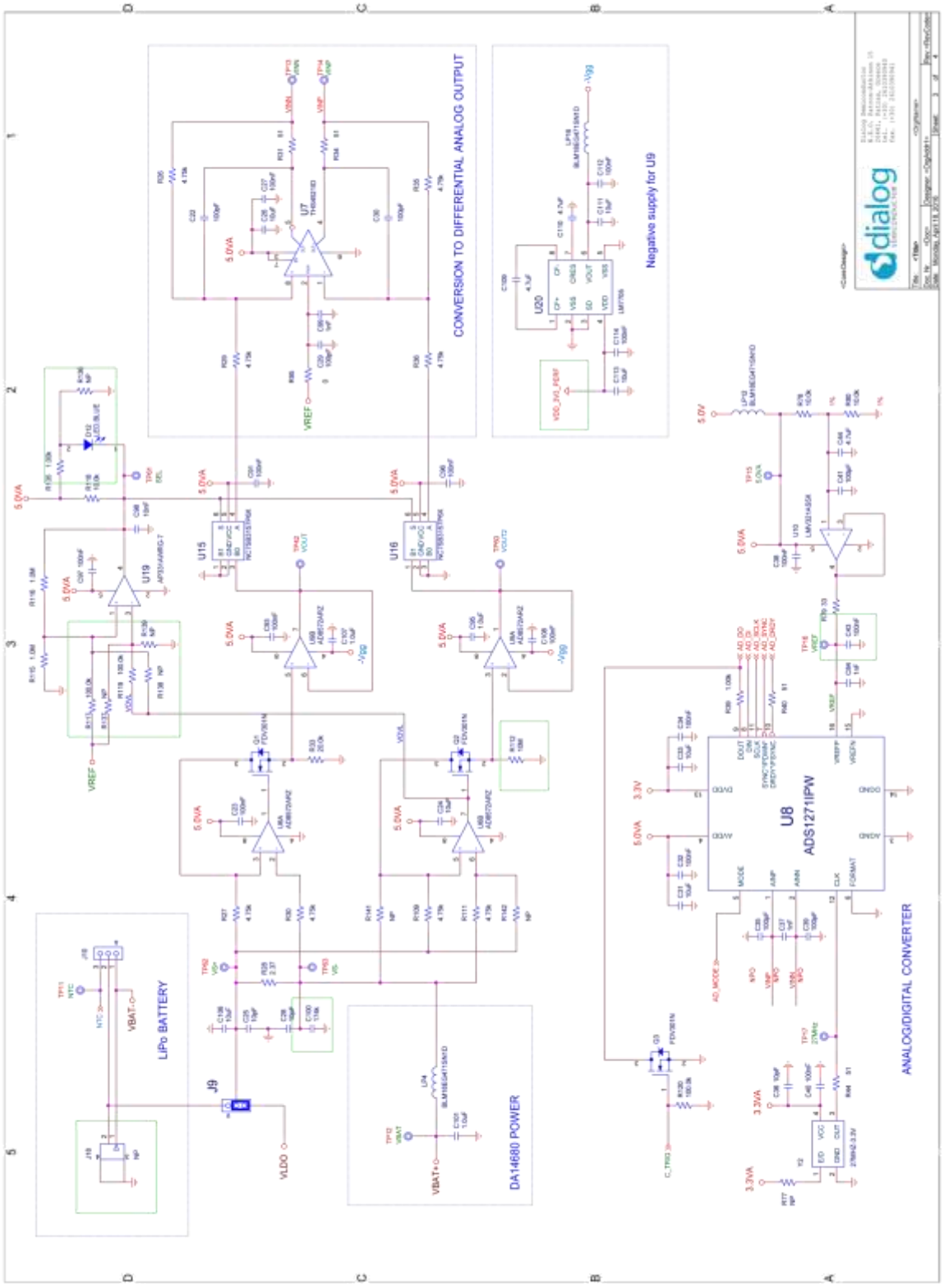

Figure 40: PRO motherboard, power measurement

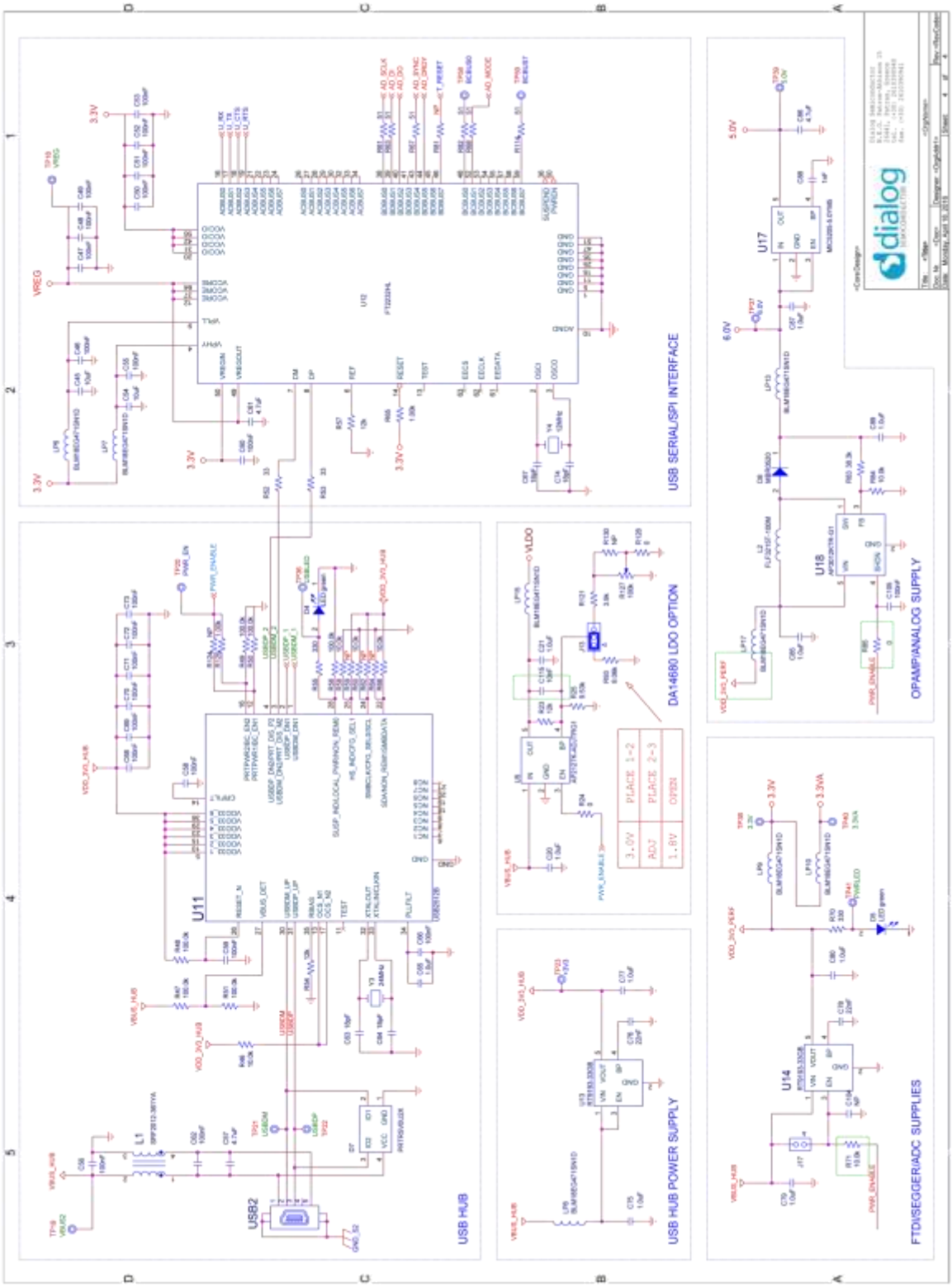

Figure 41: PRO motherboard, power section

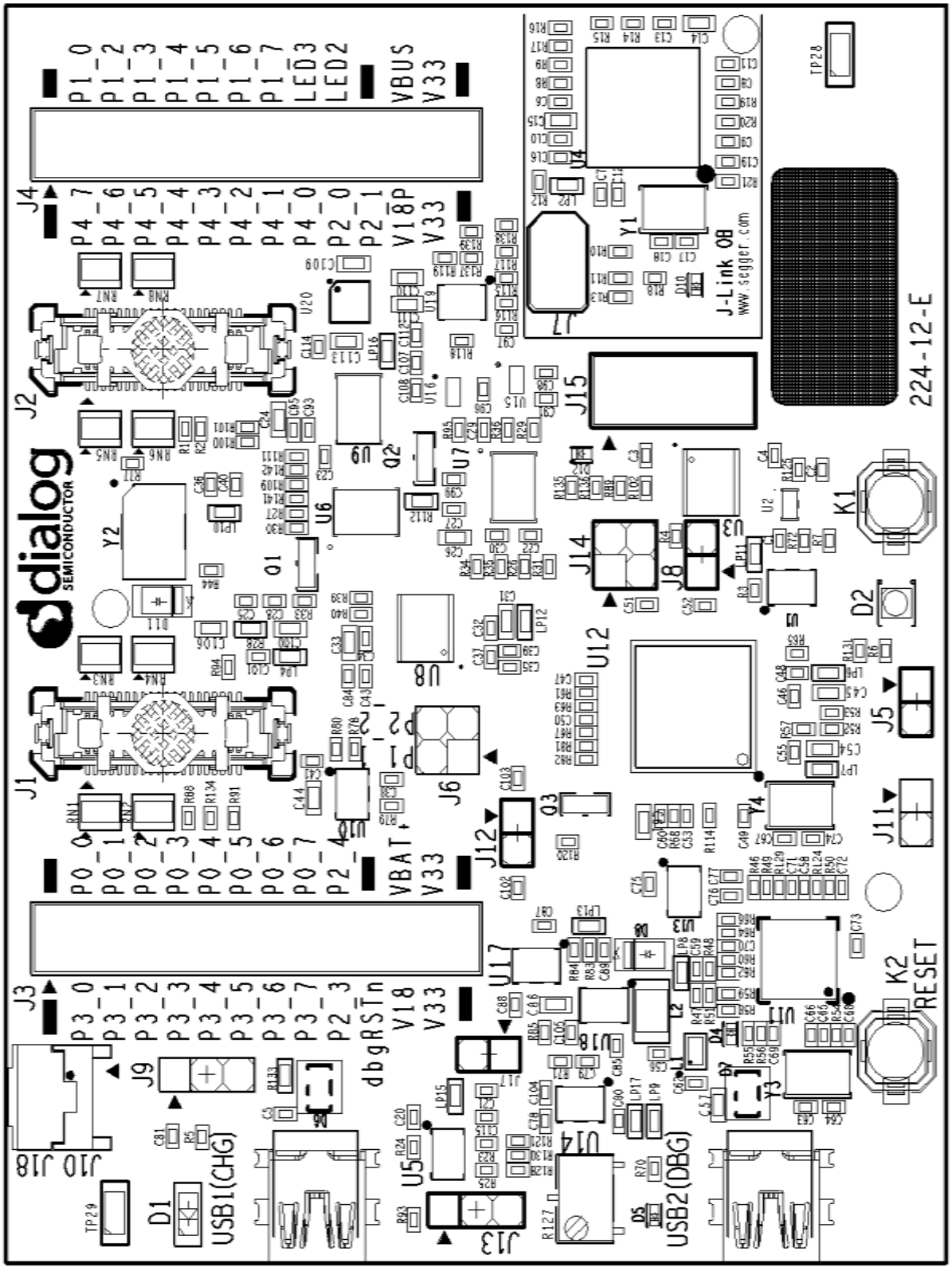

Figure 42: PRO motherboard SILKSCREEN

9.1 PRO AQFN60 daughterboard Schematics and pcb silkscreen

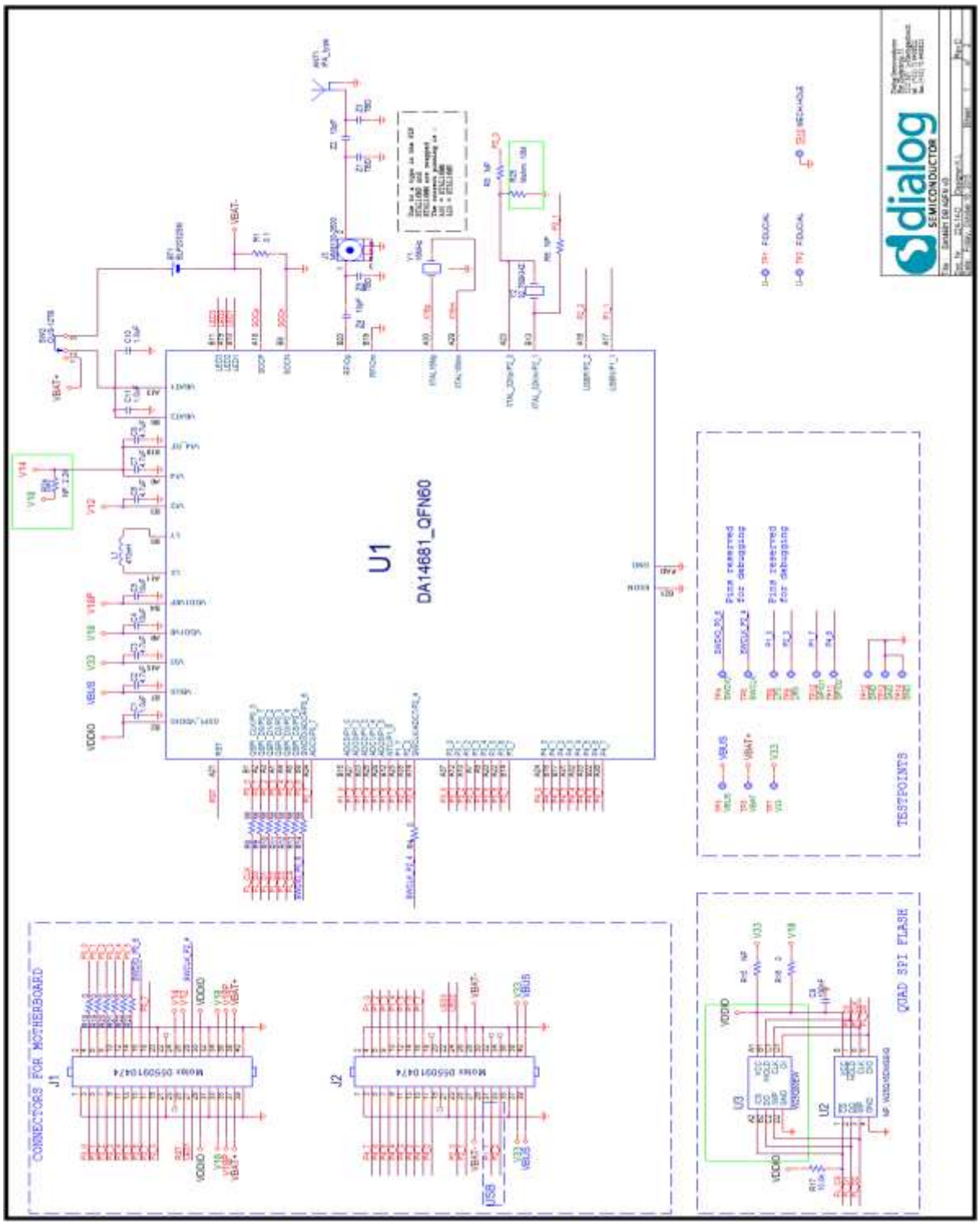

Figure 43: PRO AQFN schematic

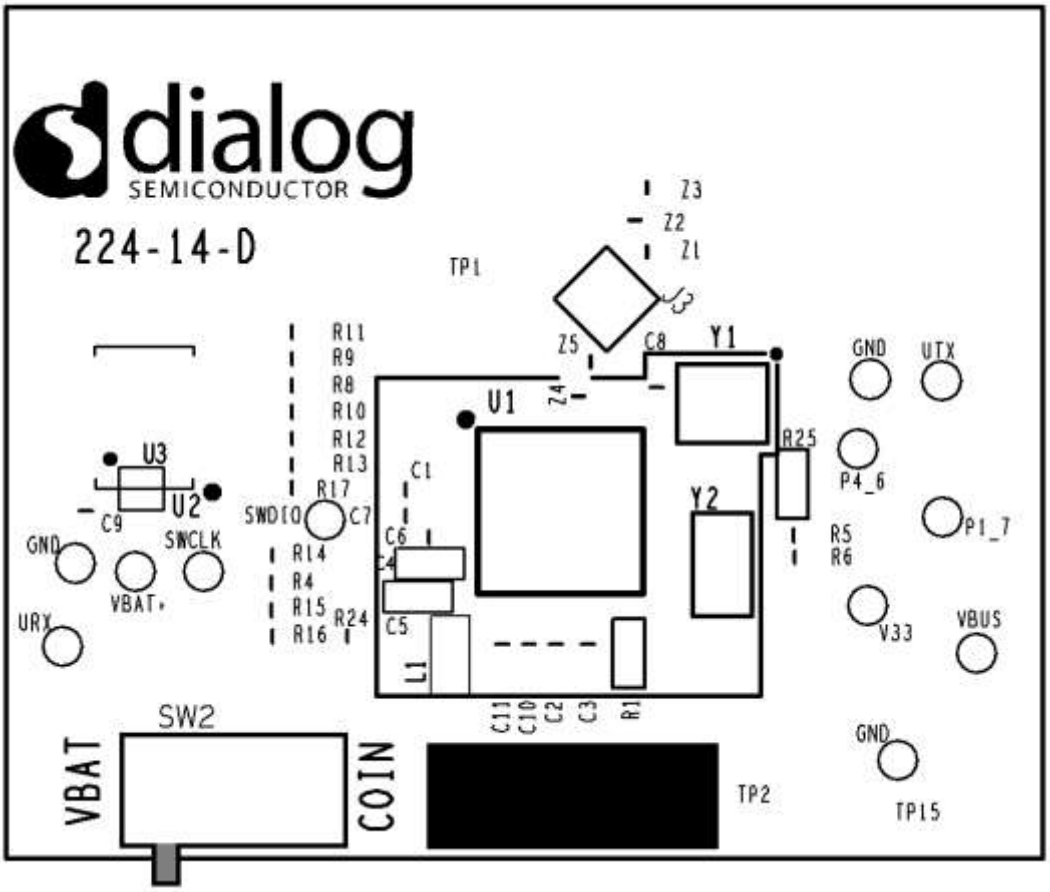

Figure 44: PRO AQFN60 SILKSCREEN

9.2 PRO WLCSP daughterboard Schematics and pcb silkscreen

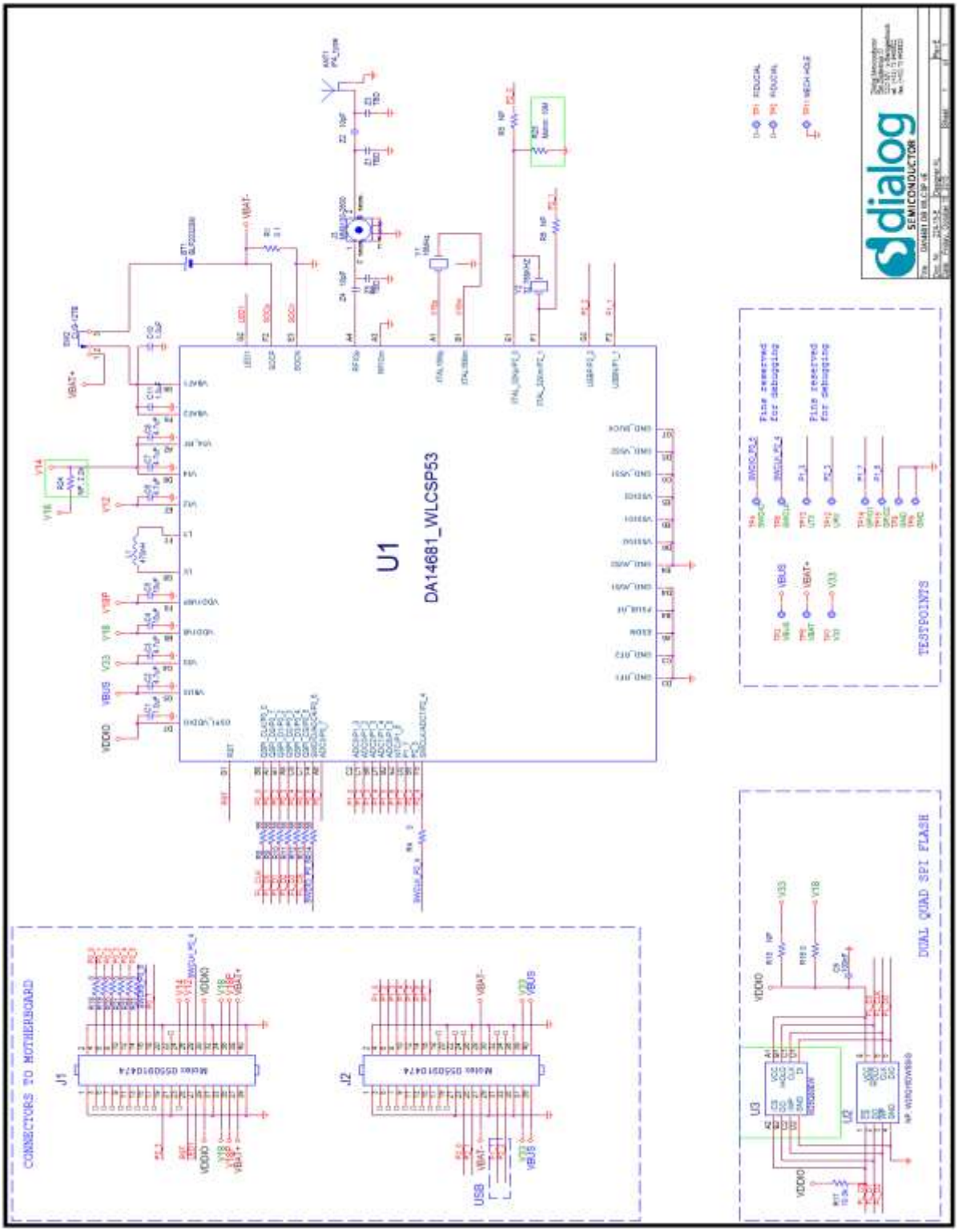

Figure 45: PRO WLCSP53 SCHEMATIC

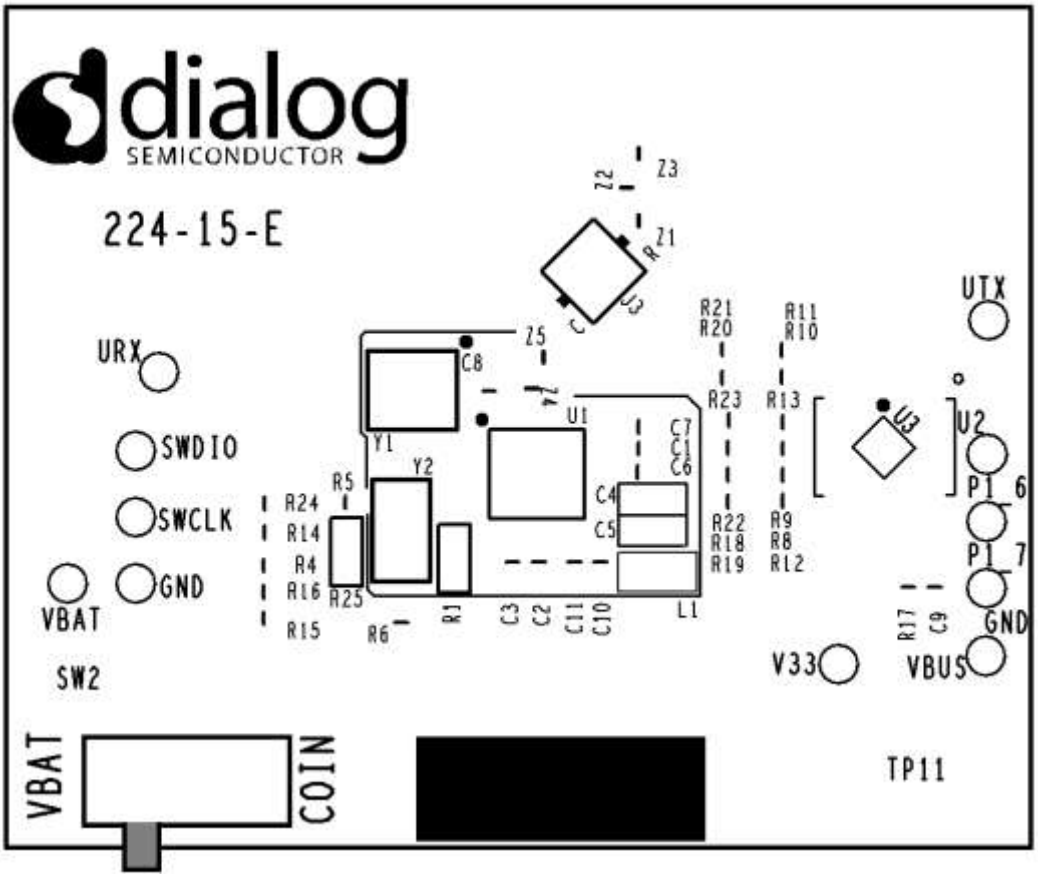

Figure 46: PRO WLCSP53 SILKSCREEN

Revision history

Revision	Date	Description
1.0	9-July-2015	Initial version.
1.1	26-May-2016	Text corrections
1.2	12-July- 2016	Update PRO-Motherboard data (revE). Remove USB dongle
1.3	25-July- 2016	Added revision history
1.4	16-Sept-2016	USB termination resistors note
1.5	11-Sept-2017	Table 3 corrections
1.6	30-Nov-2017	Remove Sensor Lab
1.7	28-Dec-2021	Updated logo, disclaimer, copyright.

Status definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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