Y-ASI4U-V5-DB

Hardware User Manual

Introduction

This document explains the hardware design of the Y-ASI4U-V5-DB, its main features and the necessary hardware setup in order to implement an ASi-5 slave.

Contents

1. Overview

1.1 ASI4U-V5 ASSP Features

The Y-ASI4U-V5-DB is a Development Board for the ASI4U-V5 ASSP Renesas silicon solution that implements an Actuator-Sensor-Interface version 5 (ASi-5) fieldbus transceiver. It reduces the integration effort of an ASi-5 interface to a minimum. The implementation of the complex transmission process is optimally distributed between hardware and firmware components.
Both slave options outlined in the ASi-5 specification are easily implemented. In simple slave mode, the chip is only supplied with process data via digital I/O pins. For complex slave implementations, process data and acyclic communication are handled via a serial interface. The compact, power-saving design enables the development into small form factors.

The ASI4U-V5 ASSP offers the following features.

- Silicon solution implementing an ASi-5 transceiver
- ASi-5 supports the integration of up to 96 devices, operation down to 1.27 ms cycle time and up to 200-meter cable length.
- Up to 32 bytes of cyclic data per device.
- Diagnostics and event handling for industry 4.0 applications
- Backwards compatibility with ASi-3 devices
- Exceptional robustness against electromagnetic disturbers
- Supports simple slave and complex slave applications
- Operating Temperature: -40°C to +85°C
- Supply voltages: 5V & 3.3V
- Package: 64-pin Quad Flat No-lead (QFN), 9 x 9 mm, 0.5 mm pitch

For more information, please refer to the ASI4U-V5 ASSP Datasheet.

1.2 Y-ASI4U-V5-DB Capabilities

The Y-ASI4U-V5-DB integrates all the necessary components in order to quickly evaluate the ASi-5 Fieldbus technology.

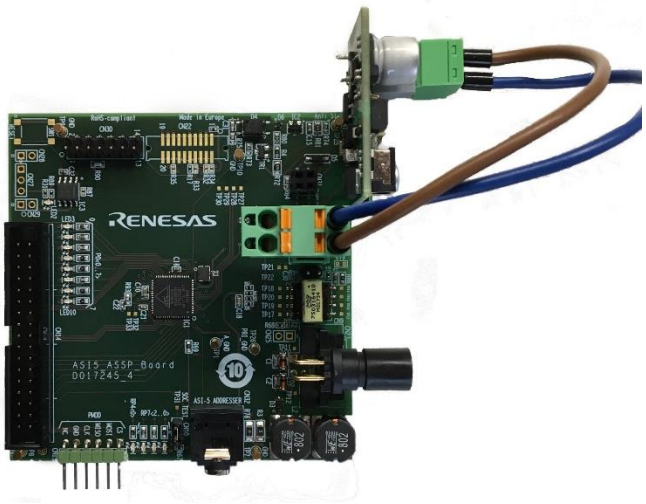


Figure 1: Y-ASI4U-V5-DB picture

2. Getting Started

2.1 System Block Diagram

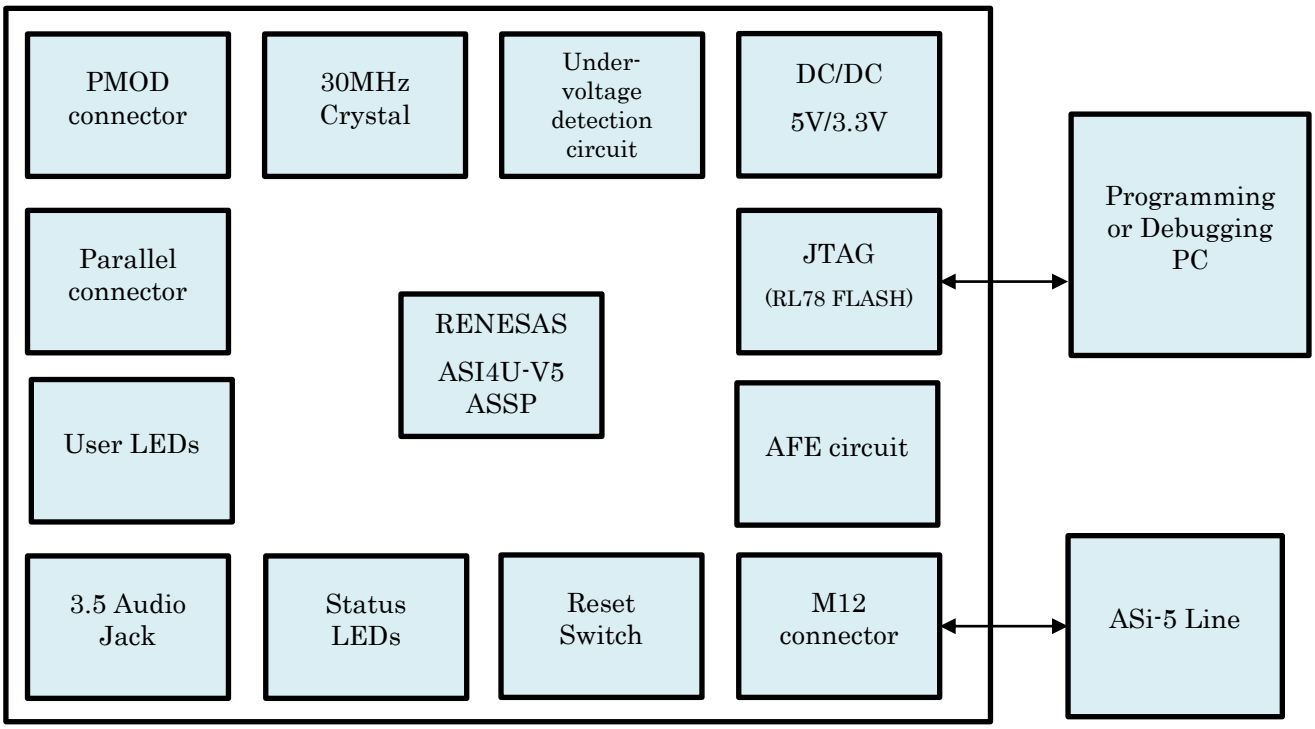


Figure 2: Y-ASI4U-V5-DB block diagram

2.2 Default Board Configuration

Make sure that the provided cable set (brown and blue) is connected from CN11 to the DC/DC Module power input. Also, close CN12, to enable the DC/DC Module to produce the 5 and 3.3 Volts from the ASi line voltage.

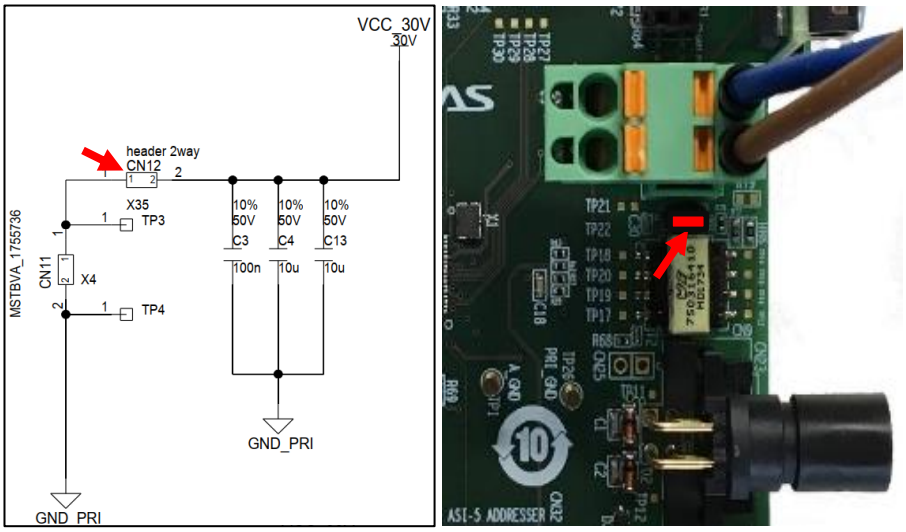


Figure 3: CN12 jumper connection

3. Y-ASI4U-V5-DB Components

3.1 Power Requirements

Y-ASi4U-V5-DB is designed to operate under 30-24V, 5V and 3,3V. The onboard DC/DC circuit regulates the 30-24V to a stable 5V and 3.3V.

The Y-ASi4U-V5-DB's typical power consumptions is around 0,8 Watt. (35 mA under 24V). Please refer to the datasheet for the typical current consumption of the ASI4U-V5_ASSP.

3.1.1 Power Supply Options

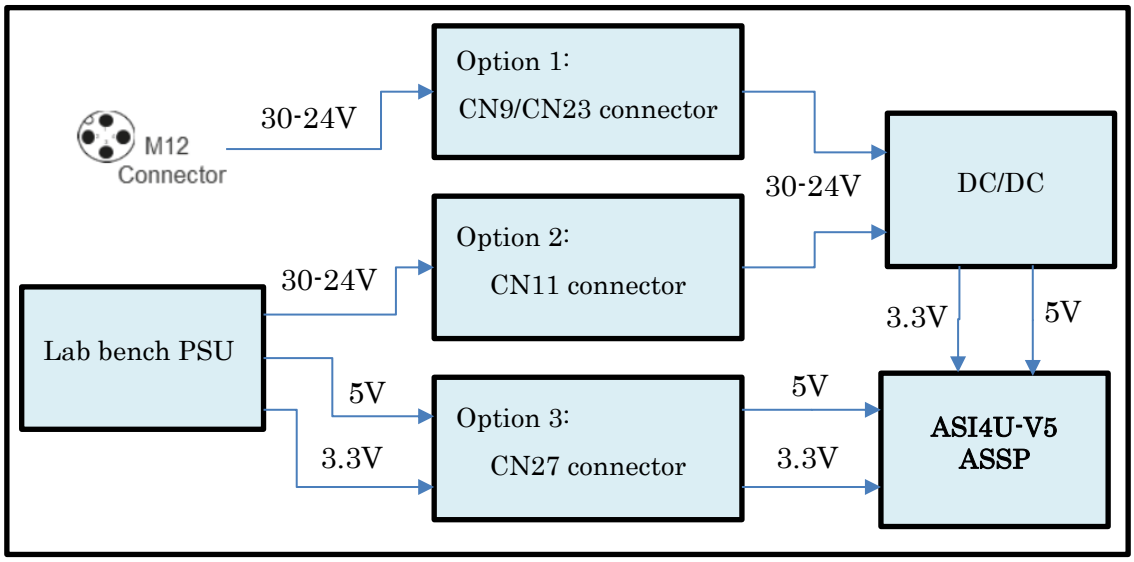


Figure 4: Y-ASI4U-V5-DB power options

The ASi4U-V5_ASSP requires 5V and 3.3V to operate, a 24-30V voltage can be delivered by the ASi line, then converted to the appropriate values by a DC/DC converter. The Voltage of the ASi line can vary between 24-30V depending on the total length of the ASi cable, the number of operating slaves and the potential additional power delivered by an ASi certified power supply.

3.1.1.1 Option 1A: CN9 Connector

The CN9 is a male right-angle 4-pin M12-A-coded connector. It enables an easy connection between the Y-ASi4U-V5-DB and the ASi line. From this connector, only 2 pins are used to connect to the ASi signal and the power supply.

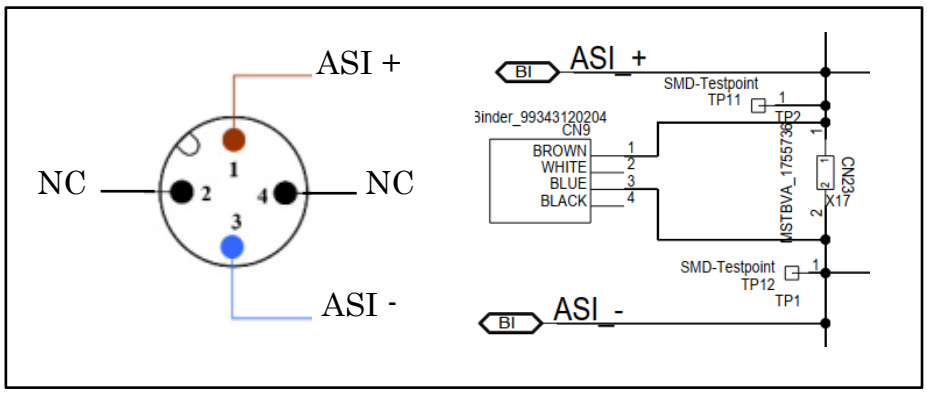


Figure 5: CN9 connector

3.1.1.2 Option 1B: CN23 Connector

The CN23 (not mounted) can also be used if you do not dispose of a splitter piercing the ASi cable. Then, solder another type of connector at the backside of the PCB but **be careful to respect the polarity!** (blue is ASI- and brown is ASI+).

3.1.1.3 Option 2: CN11 Connector

The Board can also be powered using a Laboratory Bench PSU. Therefore, you can input 30-24V directly to CN11. Again, **make sure to respect the polarity!**

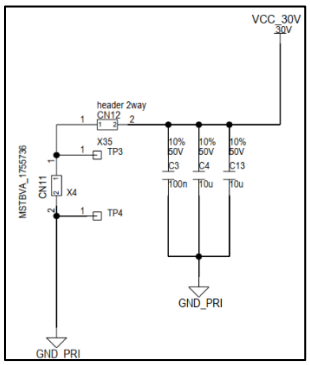


Figure 6: CN11 connector

3.1.1.4 Option 3: CN27 Connector

The Board can also be powered using a Laboratory Bench PSU or an external power module from CN27. Therefore, input 5V on pin 1, 3.3V on pin 2 and GND on pin 3. Make sure to close CN28 and CN29.

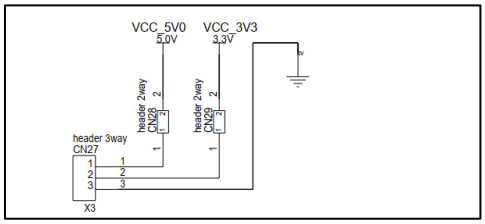


Figure 7: CN27 connector

3.1.2 DC/DC Passive Power Supply

Here is the schematic of the DC/DC Module mounted on connector CN26 of the Y-ASI4U-V5-DB. This is a passive components-based isolated power supply containing a shut-down and auto-recovery short circuit protection feature.

This design shall be replaced by the 2 following Renesas **isolated or non-isolated** power supply introduced chapter 3.1.3.

Please check with Renesas staff for an optimized power supply fitting your design requirements.

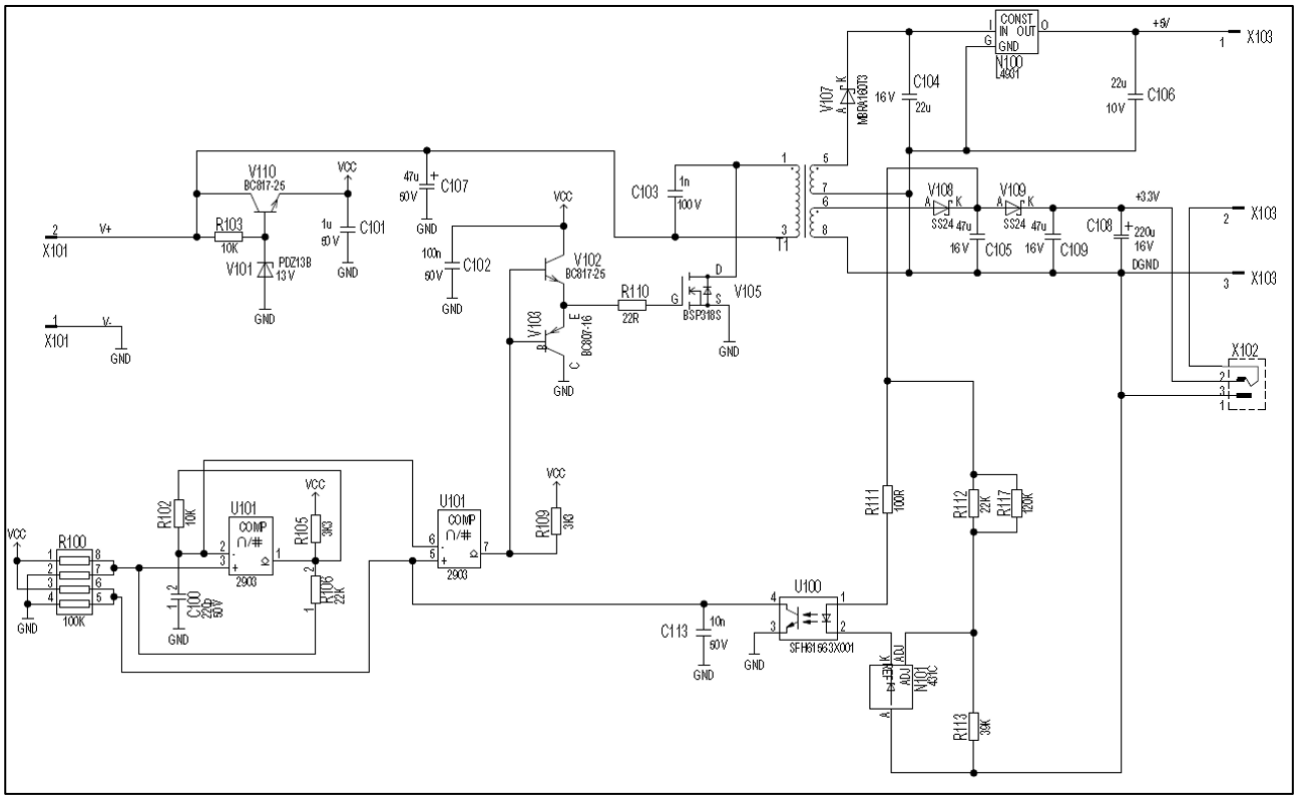


Figure 8: Onboard DC/DC schematic

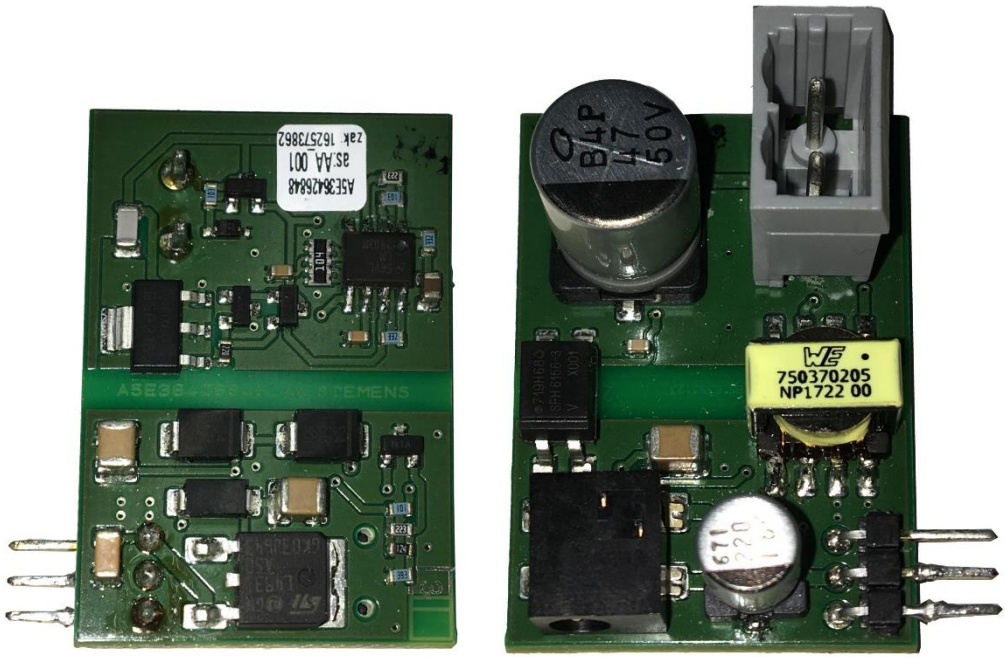


Figure 9: Onboard DC/DC picture

3.1.3 Renesas ASi-5 Slave Power Supply Reference

In order to replace the existing DC/DC module assembled on connector CN26. Renesas recommends the 2 following designs: These were implemented according to the 2 following use cases:

- **Isolated** if your design requires more than one power source. This will allow you to have 2 different ground potential, in the case you need to exceed the power supplied by the dedicated ASi-5 power supply.
- **Non isolated** if your design does not require any additional power source.

The power supply specifications for the ASI4U-V5_ASSP are the following:

- Input voltage range: 14-31V
- Output Voltage: 5V and 3,3V
- Output voltage ripple: 100mV max
- Output ripple frequency: 100kHz max

Please refer to the ASI4U-V5_ASSP datasheet for more information regarding the current consumption.

The 2 following power supply reference designs have been checked by the ASi accredited laboratory (HTWK University in Leipzig) and successfully passed all power supply related tests an ASi-5 end product has to pass in order to obtain the certification.

3.1.3.1 Isolated power supply

Renesas developed an isolated power supply for ASi-5 based on the following ICs:

- ISL854102
- RAA214220
- RAA214250

The following design was developed to comply with the ASi-5 power specifications.

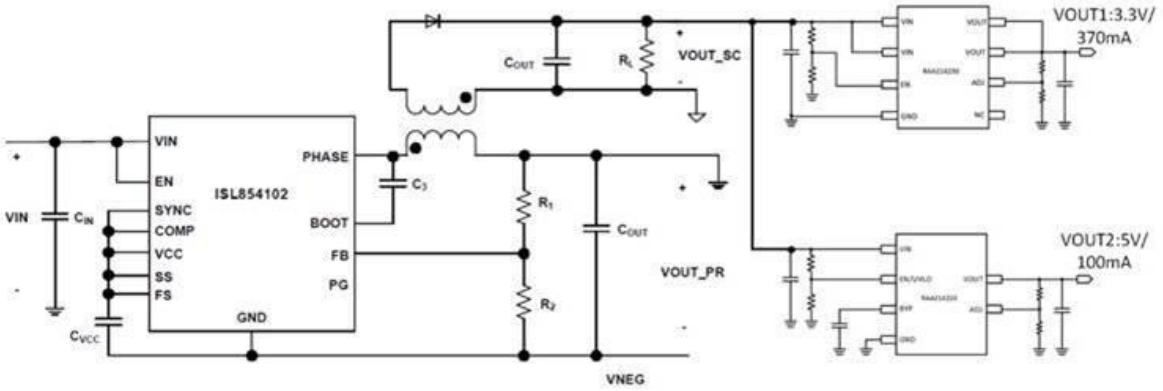


Figure 10: RTKA_ASI5ISOPOWSUP1Z schematic

Here is the Evaluation Board:

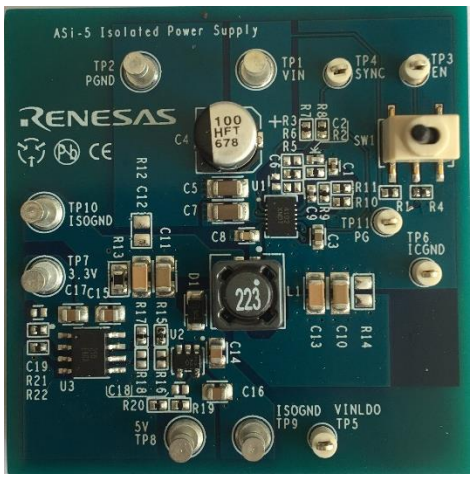


Figure 11: RTKA_ASI5ISOPOWSUP1Z EVB

All documents can be found under the folder: *Y-ASI4U-V5-DB\HW\ASI5_Power_Supply\Isolated*

Please check with your Renesas representative or the Renesas website on how to obtain the **RTKA_ASI5ISOPOWSUP1Z** evaluation board.

3.1.3.2 Non-isolated PSU

Renesas recommends using the following configuration to provide the necessary voltage to power the ASSP.

IC	EVB	Component
RAA211605	RTKA211605DR0010BU	DC/DC step-down regulator
ISL80505	ISL80510EVAL1Z	LDO
RAA214220	RTKA214220DR0000BU	LDO

Figure 12: ASi-5 NON-Isolated power supply BOM

All documents can be found under the folder: *Y-ASI4U-V5-DB\HW\ASI5_Power_Supply\non_Isolated*

These EVBs are orderable via the Renesas website.

3.1.4 Analog/Digital Decoupling

In the following block diagram and in the board schematic, a distinction is made between the signals:

- **VCC_A**xxx powering the ASSP AFE related inputs
- **VCC_D**xxx powering the Digital portion of the ASSP

Digital and Analog supply voltages, although coming from the same source, should be separated in the PCB layout early to minimize degradation of the voltage characteristics due influences from the other path.

It is possible to isolate the voltage powering these 2 portions by removing R29, R62 or R63.

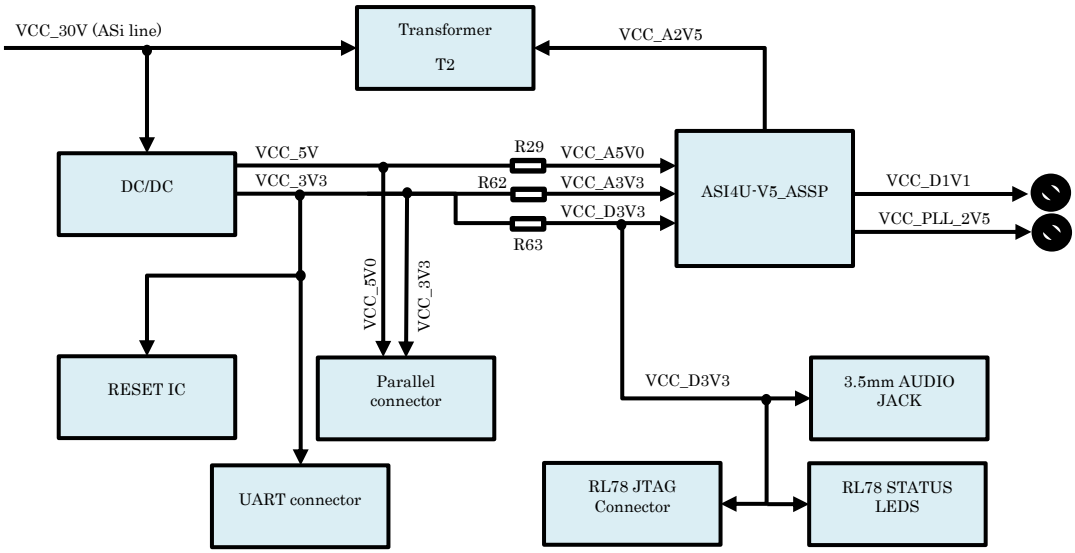


Figure 13: Y-ASI4U-V5-DB power distribution

3.1.5 Power Up Behaviour

When powered for the first time, the LED2 lights up. Then, the factory sample program will run, the device will be configured as an 8 I/O device.

3.2 Firmware Update Probe connectors

3.2.1 RL78 Firmware Update Connector

Use a Renesas Debug probe in order to update the Firmware the ASI4U-V5_ASSP.

We recommend using the “Renesas E2 lite” for this operation; Please check with your Renesas representatives or the Renesas website on how the probe can be obtained.
The probe can be connected to the following port for the purpose of updating the firmware.

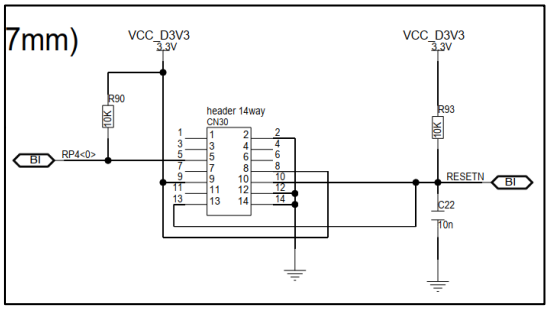


Figure 14: RL78 JTAG connector

3.2.2 MIPI20 Debug Connector

The CN22 is only for Renesas internal use.

3.3 Communication Interfaces

3.3.1 CN9 to the ASi Line

Connection to the ASI line. Both, power and the data signal, is transported using the same 2 wires of the ASi cable.

3.3.2 Parallel Connector for GPIO access

The connector CN14 enables an easy access to the ASSP IOs. These IOs can be configured to acquire your sensor's data, for example. The digital signals inputted/outputted to the ASSP GPIOs via CN14 can then be processed according to a Simple or Complex slave use case. The SPI interface can also be accessed via CN14 enabling an easy and unique cabling for both modes.

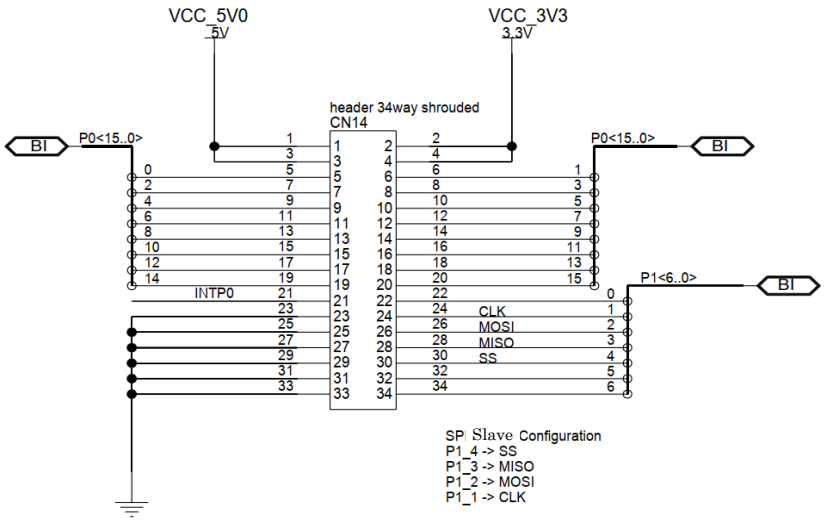


Figure 15: ASi-5 to Multisensorboard parallel connector

Mapping of ASI4U-V5_ASSP signals/voltages to the Y-Multisensorboard_1:

Y-ASI4U-V5-DB CN14	ASI4U-V5_ASSP	Y-Multisensorboard_1 J33
1	5V	5V
2	3V3	3V3
3	5V	5V
4	3V3	3V3
5	P0_00	BIT0
6	P0_01	BIT1
7	P0_02	BIT2
8	P0_03	BIT3
9	P0_04	BIT4
10	P0_05	BIT5
11	P0_06	BIT6
12	P0_07	BIT7
13	P0_08	BIT8
14	P0_09	BIT9
15	P0_10	BIT10
16	P0_11	BIT11
17	P0_12	BIT12
18	P0_13	BIT13
19	P0_14	BIT14
20	P0_15	BIT15
21	P2_1 / INTP0	BIT21

22	P1_00	BIT16
23	GND	GND
24	P1_01	BIT17 / SPI CLK
25	GND	GND
26	P1_02	BIT18 / SPI MOSI
27	GND	GND
28	P1_03	BIT19 / SPI MISO
29	GND	GND
30	P1_04	BIT20 / SPI SS
31	GND	GND
32	P1_05*	BIT23 / UART0 RX/TX
33	GND	GND
34	P1_06	BIT22 (DSR signal)

Figure 16: Parallel connector pin mapping

*Note: P1_05 can be accessed on BIT23 and via the UART Connector.

3.3.3 PMOD Connector for SPI access

This PMOD connector is connected to the SPI interface of the ASSP. This can typically be used in the “Complex Slave” configuration.

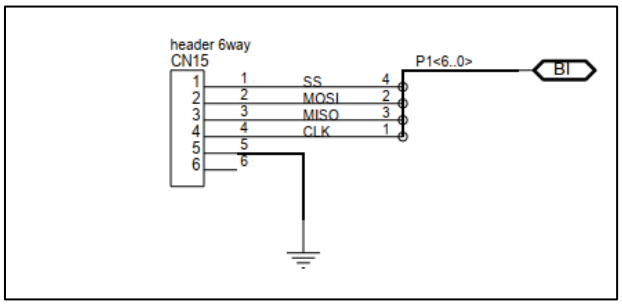


Figure 17: PMOD connector

The Pins allocated to the SPI interface (P1_1...P1_4) are also accessible via CN14.

3.4 UART Connector

3.4.1 3.5mm Audio Jack Connector

The Connector CN32 is used to enable an easy connection with the VCP-HH5-01 Bluetooth addresser, using a multiplexed UART interface.

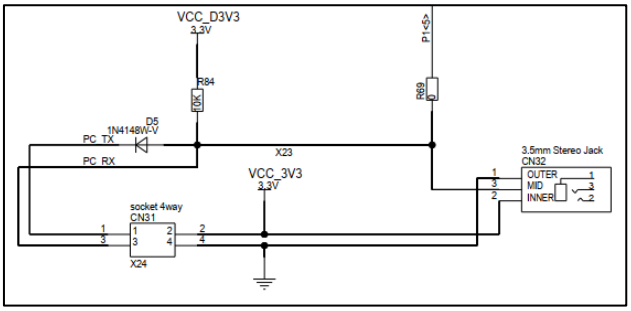


Figure 18: 3.5mm Audio Jack connector

3.4.1.1 VCP-HH5-01 Bluetooth Addresser

ASi-5 offers the possibility for the Master to configure the slave address and other parameters directly. **Alternatively, ASi-5 slaves can be configured using an ASi-5 addresser tool in combination with an ASi-5 addresser app.**

This device allows the user to read the ASi-5 Slave configuration data and change its address. Be aware that only the **User page** can be red and modified by the device, the **Factory page** is not concerned.

Here is the HW setup in order to be able to communicate between the Tool and the ASi-5 slave.

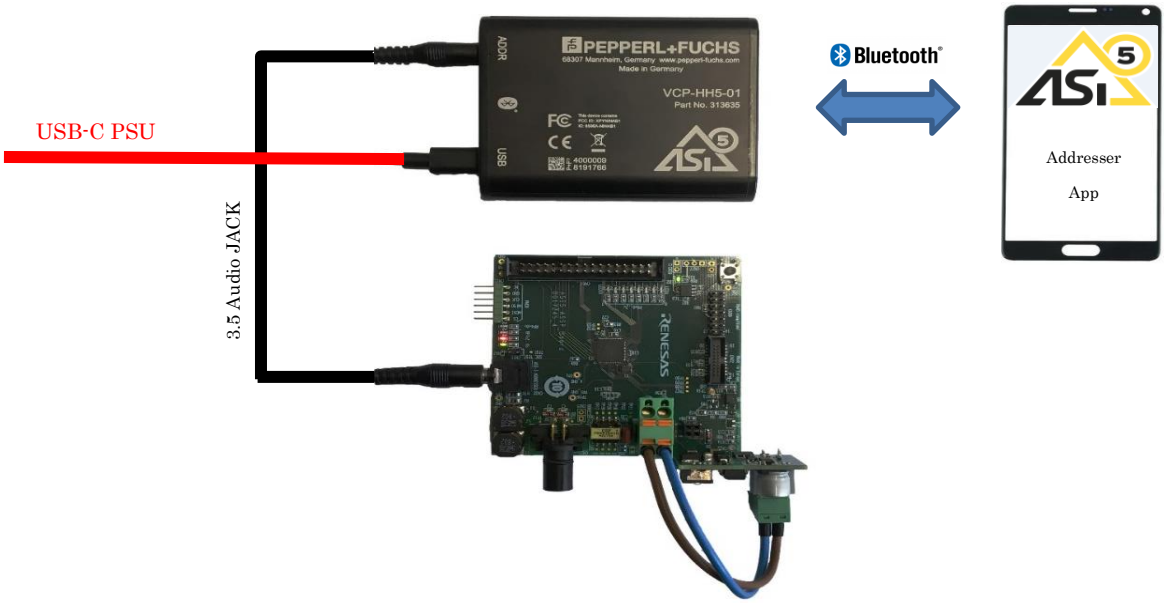


Figure 19: ASi-5 Addresser setup

Refer to chapter 8.4 of the *ASi-5_Specification.pdf* for more information.

3.4.1.2 iOS/Android/PC Addressing App

The control applications of the VCP-HH5-01 are available for windows, android and IOs. Therefore, search for “ASi-5” in Microsoft App Store, Google Play or App Store.

3.4.2 UART Access

For more flexibility, the UART RX/TX signals mapped to P1_5 can also be separately accessed via CN31

3.5 LEDs

3.5.1 RL78 Status LEDs

The 4 LEDs indicate the current state of the ASI4U-V5_ASSP.

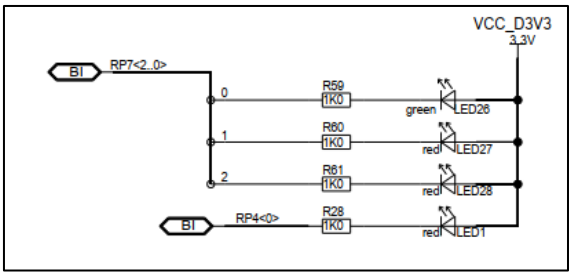


Figure 20: RL78 Status LEDs

- RP7_0 and RP7_1 are the status LEDs related to the table page 10 of the “ASi5-Device_ImplementationGuide.pdf”
- RP4_0 lights ON when the RL78 NVRAM content is written by the probe.
- RP7_2 will light ON if the RL78 NVRAM content is red. This only appends in very specific use cases.

The following table represents the LED pattern of RP7_0 and RP7_1 according to the various states the ASi-5 Slave can face. This pattern represents these 2 LEDs status during 1 second. So, each brick represents 125 milliseconds.

In the case a Dual LED is used, the colour “Yellow” is displayed when both Red and Green LEDs are ON.

Status	Status indication ASi-5	
	Two LEDs	Dual LED
Normal operation		
Energy Saving State		
No data exchange (Address = 0)		
No data exchange (Address > 0)		
Diagnostic Request (Warning)		
Periphery fault (Critical)		
Serious Periphery fault (Defect)		
Identification		

Figure 21: RL78 Status LEDs diagnostic

3.5.2 I/O Status LEDs

The following LEDs can be used to monitor the output signals of P0_00...P0_07.

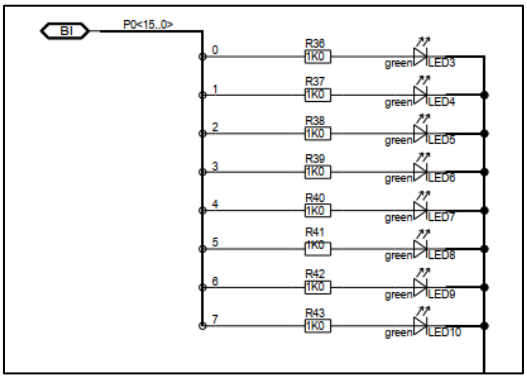


Figure 22: I/O status LEDs

These 8 LEDs can be used to visualize the outputs of P0_00...P0_07 in the case these GPIOs are configured as outputs.

3.5.3 Power Status LED

LED2 is used as a status LED, it lights OFF when SW1 is pressed, otherwise it stays ON to signal that the board is powered.

3.6 Under Voltage Detection Circuit

The following circuit is used as an Under-Voltage Detection Circuit. The output signal INP0 is raised to HIGH if the voltage feeding the DC/DC falls under 8V. Then, INP0 fells back to LOW when the voltage exceeds 23V.

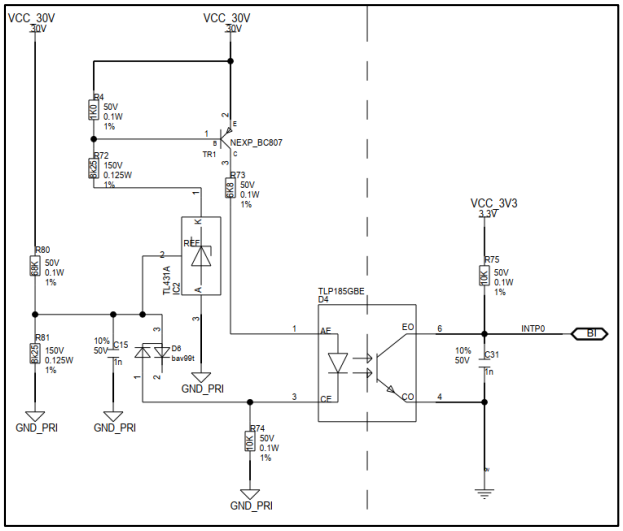


Figure 23: Under voltage detection circuit

This circuit is used to detect a significant voltage drop on the ASi line. The INP0 status can be accessed via the diagnostic data in order to get debug information.

3.7 Reset Circuit

3.7.1 Push Button

SW1 Push button is used to perform a “soft reset” of the ASI4U-V5_ASSP.

3.7.2 Reset Monitoring IC

The following circuit is used to send a clean logical signal to the ASI4U-V5_ASSP when SW1 is pressed.

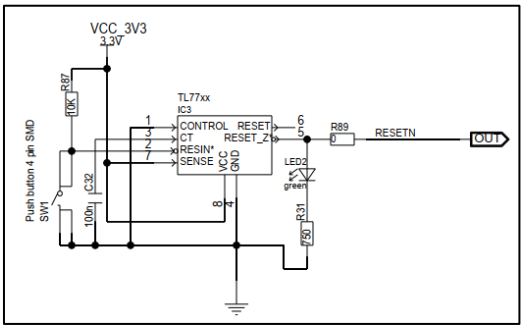


Figure 24: Reset monitoring IC

3.8 Analog Front End coupling/Decoupling Circuit

The Analog Front End (AFE) of the ASi-5 Slave with the external decoupling unit and supply of the ASI4U-V5_ASSP is shown below.

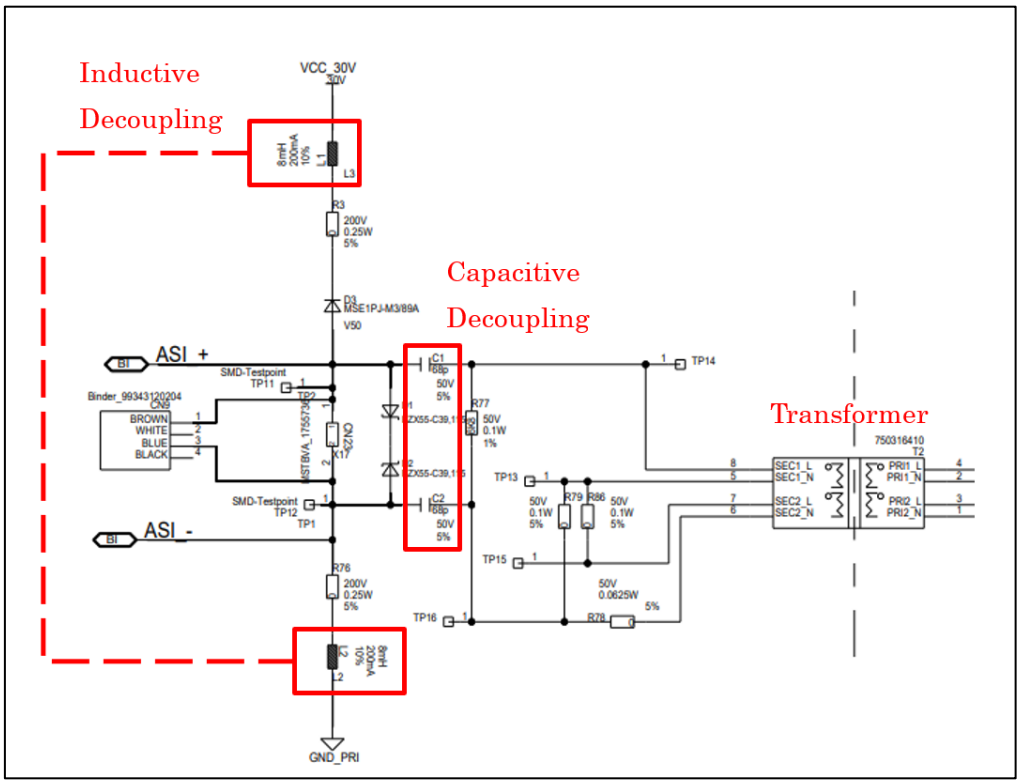


Figure 25: Analog Front End coupling/Decoupling Circuit

Every communication partner in the AS-interface network need to decouple the data signals from the power. For the ASi-5 signal, it consists of a capacitive decoupling unit and a transformer.

The power supply for the ASI4U-V5_ASSP consists of an inductive decoupling unit and a DC/DC converter. It supports an internal LDO (Low Drop Output) for the power supply of the MDS.

The AFE itself is divided into three functional paths, the auxiliary power path, the transmitting path and the receiving path.

The dimensions of the Transformer, the Inductive and capacitive decoupling circuit are essential in order to ensure the reliability of the ASi-5 Slave.

3.8.1 Transformer Dimensions

The transformer T2 needs to respect the ASi-5 specification regarding the AFE of the ASi-5 signal.

The transformer parameter set is shown below. All ASi-5 qualification tests have been performed using this very transformer:

- **WE 750316410** from Würth Electronics.

ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	4-1	tie(2+3), @20ºC	0.249 ohms ±10%
D.C. RESISTANCE	8-5	@20ºC	0.421 ohms ±10%
D.C. RESISTANCE	7-6	@20ºC	0.520 ohms ±10%
INDUCTANCE	4-1	tie(2+3),100kHz, 10mV, Ls	22.00uH ±10%
INDUCTANCE	8-6	tie(7+5),100kHz, 10mV, Ls	350.00uH ±10%
INDUCTANCE	8-5	100kHz, 10mV, Ls	55.30uH ±10%
DIELECTRIC	1-8	tie(2+3, 7+5), 1875VAC, 1 second	
TURNS RATIO		(8-6):(4-1), tie(2+3, 5+7)	4:1, ±2%
TURNS RATIO		(8-5):(4-1), tie(2+3)	1.6:1, ±2%

Figure 26: WE 750316410 spec

3.8.2 Coils Dimensions

Here is the specification of the coil used for the Y-ASI4U-V5-DB design:

- **WE 744776381**

Properties	Test conditions		Value	Unit	Tol.
Inductance	1 kHz/ 250 mV	L	8.0	mH	± 10%
Capacitance		C	13	µF	ref.
DC Resistance	@ 20°C	R_{DC}	16.0	Ω	max.
DC Resistance	@ 20°C	R_{DC}	15.4	Ω	typ.
Rated current	ΔT = 40K	IR	0.20	A	max.
Saturation current	|ΔL/L| < 10%	I_{sat}	0.20	A	typ.
Self resonant frequency		f_{res}	500	kHz	min.

Figure 27: WE 744776381 spec

Depending on hardware characteristics, additional series inductances may be needed to ensure that the impedance requirement described in the following document are met:

Y-ASI4U-V5-DB_StarterKit\Y-ASI4U-V5-DB\HW\ASI5_Power_Supply\R05AN0010ED0100_Renesas_PSU_Conformance_Tests_application_note.pdf

3.9 ASI4U-V5 ASSP

3.9.1 Cristal Oscillator

The ASI4U-V5_ASSP requires a 30 MHz Cristal Oscillator with a very precise specification. This crystal is not only used to provide a clock signal to the ASSP but also to tune the whole system by switching the internal capacitors connected to X1 and X2.

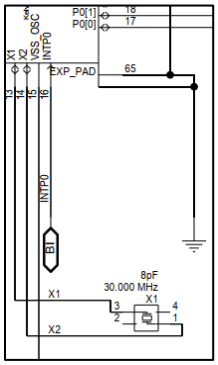


Figure 29: Crystal Oscillator circuit

Renesas strongly recommends using the **DSX321G 30MHZ** from KDS DAISHIKU CORP (spec number: **7AD03000A05**). Using another Crystal could lead to inconsistencies of the data transmission of the slaves (especially for high frequencies).

3.9.2 Internal Low Dropout regulators

The ASI4U-V5_ASSP requires 5V and 3.3V. Additionally, 4 internal LDOs are producing the following voltages used as internal supply voltage for the AFE.

- 2.5 Volts
- 1.1 Volt

Be careful, 2.5V and 1.1V must not be used to drive any external peripherals of your hardware, the sustainability of the AFE conversion highly depends on the precision of these voltage references.

3.10 PCB Characteristics

3.10.1 PCB Manufacturing Characteristics

The Y-ASI4U-V5-DB is a 4-layer PCB. The following table represents the PCB manufacturing characteristics of the board regarding the cooper and dielectric thickness:

Primary

Objects		Types >>		Thickness >>	Physical >>		Embedded >>	Signal Integrity >>		
#	Name	Layer	Layer Function	Value mm	Layer ID	Material	Embedded Status	Conductivity mho/cm	Dielectric Constant	SI Ignore
*	*	*	*	*	*	*	*	*	*	*
		Surface							1	
1	TOP	Conductor	Conductor	0.035	1	Copper	Not embedded	595900	4.5	
		Dielectric	Dielectric	0.15		Fr-4		0	4.5	
2	2_LAYER_GND	Plane	Plane	0.035	2	Copper	Not embedded	595900	4.5	
		Dielectric	Dielectric	1.2		Fr-4		0	4.5	
3	3_LAYER	Plane	Plane	0.035	3	Copper	Not embedded	595900	4.5	
		Dielectric	Dielectric	0.15		Fr-4		0	4.5	
4	BOTTOM	Conductor	Conductor	0.035	4	Copper	Not embedded	595900	4.5	
		Surface							1	

Info | Lock | Embedded layers setup | Unused pads suppression | Refresh materials

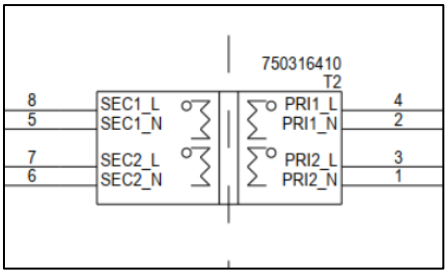
Total thickness: 1.64 mm
Total thickness without masks: 1.64 mm
Layers: 4

Figure 30: PCB manufacturing spec

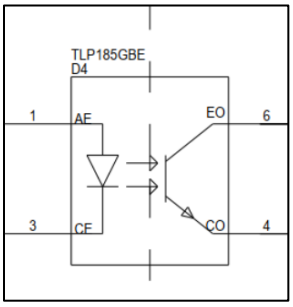
Such parameters must be adapted according to your hardware design and requirements in order to respect the Impedance and Symmetry specification values.

3.10.2 Galvanic Isolation

The galvanic isolation between the primary (30 Volts from the ASi line) and the secondary is ensured by the transformer T2.



The Isolation of the **undervoltage detection circuit** is ensured by the photodiode D4.



Additionally, the Isolation of the primary (30 Volts from the ASi line) and the 3.3V and 5V powering the ASI4U-V5_ASSP is ensured by the DC/DC's transformer T1 (See schematic chapter 3.1.2).

3.10.3 Ground Connection

On the Y-ASI4U-V5-DB, all the AFE and digital related grounds are connected between each other with R30, R95 and R96.

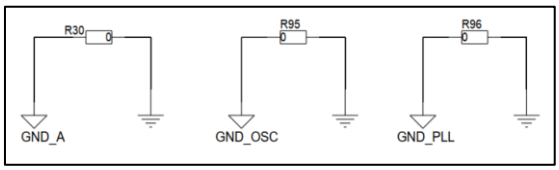
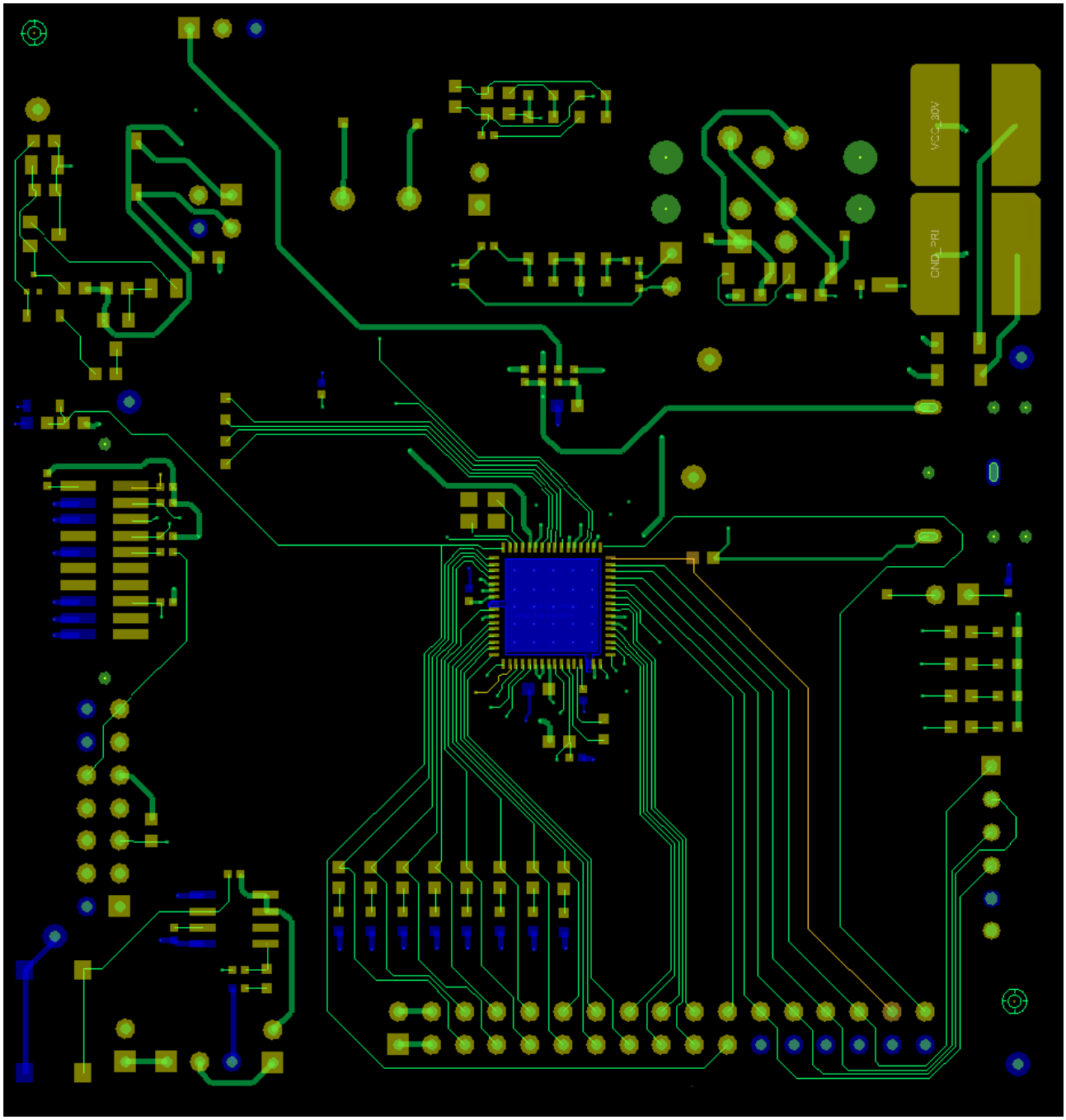


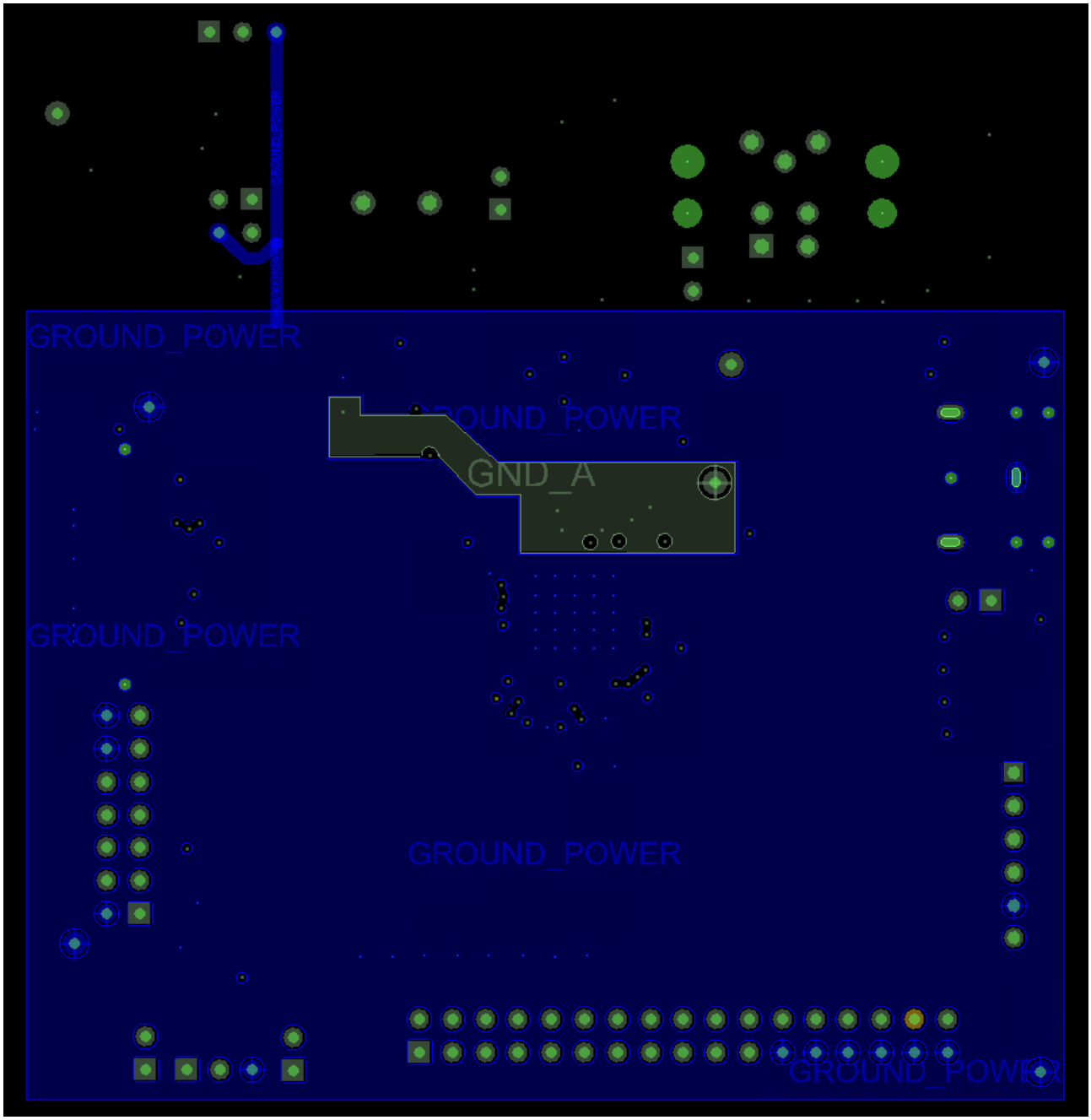
Figure 31: Ground connection of the different power rails

3.10.4 Y-ASI4U-V5-DB Layout

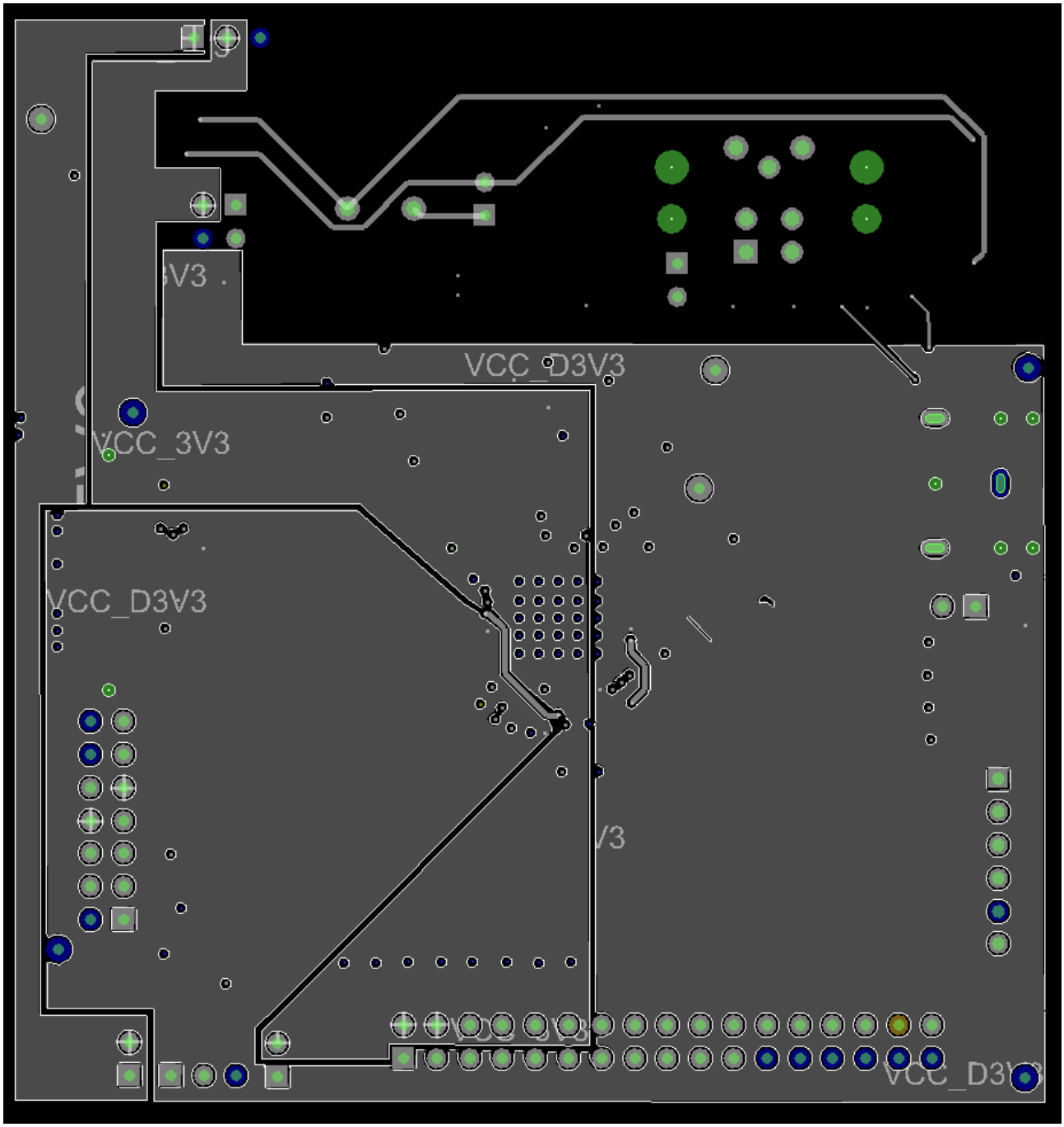
TOP LAYER:



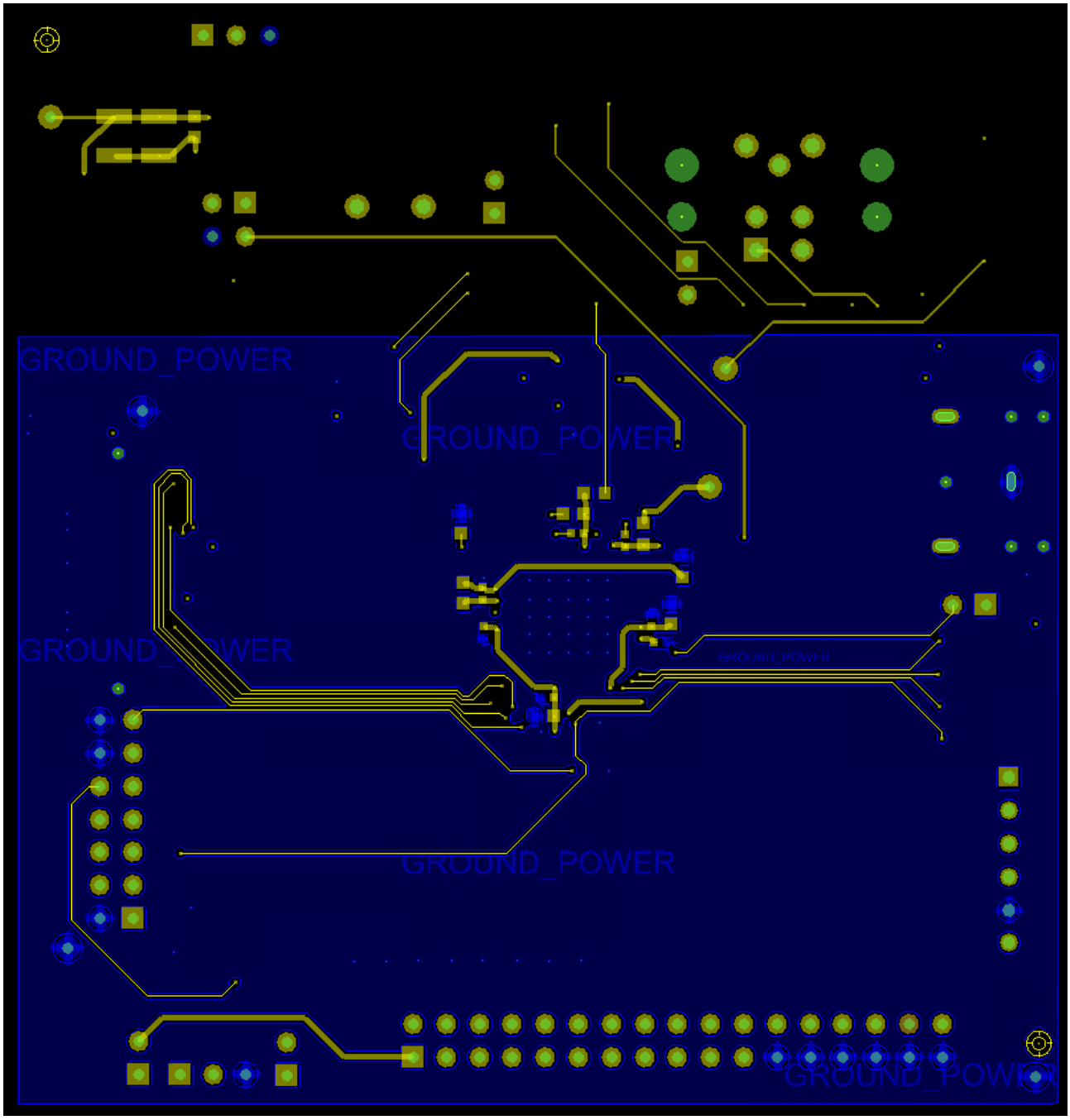
GND LAYER:



POWER LAYER:



BOTTOM LAYER:



Revision History

Rev.	Date	Description	
		Page	Summary
1.0	05.05.20		Release
1.1	28.07.20		Update Isolated PSU EVB reference
1.2	27.10.20		Impedance/Symmetry described in a separated document
1.3	14.01.22		Update NON isolated PSU reference due to EOL

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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