User's Manual

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RH850 Evaluation Platform

RH850/U2B 292pin

User's Manual: Piggyback Board

Y-RH850-U2B-292PIN-PB-T1-V1

The newest version of this document can be obtained from the product homepage:
Y-RH850-U2B-292PIN-PB-T1-V1

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems.

The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

The RH850/U2B 292pin piggyback board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics' 32-bit RH850/U2B 292pin microcontrollers.

Notes

1. This document describes the functionality of the piggyback board and guides the user through its operation.
   For details regarding the operation of the microcontroller, refer to the device's Hardware User's Manual.
2. In this document low active signals are marked by an appended 'Z' or '#' to the pin or signal name. E.g. the reset pin is named RESETZ or RESET#.
3. In this document following abbreviations are used:
   – H level, L level: high or low signal level of a digital signal, the absolute voltage value depends on the signal

1.1 Package Components

The Y-RH850-U2B-292PIN-PB-T1-V1 product package consists of the following items. After you have unpacked the box, check if your Y-RH850-U2B-292PIN-PB-T1-V1 package contains all of these items. *Table 1.1 Package Components for the Y-RH850-U2B-292PIN-PB-T1-V1* shows the packing components of the Y-RH850-U2B-292PIN-PB-T1-V1 package.

Table 1.1 Package Components for the Y-RH850-U2B-292PIN-PB-T1-V1

Item	Description	Quantity
D018567	RH850/U2B 292pin piggyback board	1
D010816-24	China RoHS document	1
D018175-24	Product contents List	1
Jumpers (2-way, 0.1")	In the bag	38 [1)] 39 [2)]
D018487	Y-RH850-DEBUG-ADAPTER-F14T46	1
Red Hirschmann 4 mm power lab sockets	In the bag	1
Resonator, HC49, 16 / 24 / 25 / 40 MHz	In the bag	4
Resistors, 100 Ohm	In the bag	20 [3)]

[1)] For board version D018567_06_V01
[2)] For board versions other than D018567_06_V01, min. quantity
[3)] For board versions other than D018567_06_V01

Note

Please keep the Y-RH850-U2B-292PIN-PB-T1-V1 box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original box when transporting the Y-RH850-U2B-292PIN-PB-T1-V1. If packing of your product is not complete, it may be damaged during transportation.

1.2 Supported Main Boards

This piggyback board can be used as a standalone board, or it can be mated with a main board. The following main boards are supported:

- Y-RH850-X1X-MB-T1-V1
- Y-RH850-X1X-MB-T2-Vx
- Y-RH850-X2X-MB-T1-V1
- Y-COMMON-MB-T1-V1

1.3 Main Features

- Burn-in socket for mounting of the device
- Several power set-up options
  - Combined operation with powering from main board
  - Stand-alone operation with single power supply (e.g. 3.3 V or 5.0 V only)
  - Stand-alone operation with flexible, individual power supply (typ. 1.12 V, 3.3 V, 5.0 V)
    Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
- Debugging and programming interface:
  - 46-pin Aurora Debug Connector (e.g. for using E2 OCD Emulator using the 46 pin to 14 pin adapter Y-RH850-DEBUG-ADAPTER-F14T46, included)
- Pin headers for direct access to each device pin
- Reset switch
- External clock circuit with an exchangeable 16/20/24/25/40 MHz Crystal Resonator
- General purpose signaling LEDs
- Jumpers for device mode selection and other configuration options
- On-board interface connector for
  - Renesas High-Speed Serial I/F (RHSIF)
  - Renesas High Speed Bus (RHSB)
  - Multichannel Serial Peripheral Interface (MSPI)
- Operating temperature from 0 °C to +40 °C

1.4 Piggyback Board Versions

The following versions of the piggyback board are available:

Table 1.2 Y-RH850-U2B-292PIN-PB-T1-V1 board versions

Board Version	Schematic Version
D018567_06_V01	D018567_04_V0100
D018567_06_V02	D018567_04_V0210
D018567_06_V03	D018567_04_V0300

Table 1.3 Differences between board versions V01, V02 and V03 on the next page lists all modifications that have been implemented in board revision V02 and V03.

Table 1.3 Differences between board versions V01, V02 and V03

Item	Modified Function	Detailed Description of Changes	D018567_06_V01	D018567_06_V02	D018567_06_V03
1	Improved signal quality when using P22_5 either for onboard functionality or offboard function on pin header or mainboard.	– Changed signal of CN14.25. See chapter *7.3.2* for details. – Changed signal of CN3.24 See chapter *7.1.3* for details	P22_5	CN_P22_5	CN_P22_5
2	RESET will not be triggered when the device enters DeepSTOP mode.	Added circuitry for DeepSTOP support during Reset.	-	Yes	Yes
3	Access to 5.0V and GND is improved for measurements.	Added 5.0V and GND pin headers JP8 and JP9	-	Yes	Yes
4	Improved signal quality when using device ports either for differential signals or single ended signals.	Changed circuitry for differential interfaces: – Changed multiplexers for LVDS signals – Added SW2 for RHSB/MSPI/RHSIF multiplexer enable/disable – Added (auxiliary) termination resistors for LVDS signals	-	Yes	Yes
5	More flexible usage for EVTO signal source.	Added P32_0 as EVTO signal on AURORA connector.	-	Yes	Yes
6	Changed port control signal for Ethernet0 Reset on the MainBoard to Ethernet0 control signal on PiggyBoard.	Changed Ethernet0 RESET control signal on CN1.69.	P12_3	P10_8	P10_8
7	Improved signal quality for Ethernet 0 clock signal.	Update for Ethernet0 clock signal: – Changed port control signal for signalling LED 6. – Changed signal on CN1.89 (DIGIO_4)	P11_4	P22_0 Implemented by factory rework. For details refer to *9.2 Factory Rework on Board Marked D018567_06_V02*	P22_0
8	Pin numbers on CN5, CN14, CN15	There are different pin numberings on the device port connectors CN5, CN14 and CN15. One way is to use characters A/B/C/D/E/F for different rows and numbering in the rows.	Uses characters A/B/C/D/E/F for different rows in the device port	Uses only numbers on the device port connectors	Uses only numbers on the device port connectors

Item	Modified Function	Detailed Description of Changes	D018567_06_V01	D018567_06_V02	D018567_06_V03
		The other way is to use only numbering on all pins.	connectors		
9	Access to 5.0V and GND is improved for measurements.	Added TP1 on SVRPGATE, TP2 on SVRNGATE, TP3 on SVR	-	Yes	Yes
10	Signal buffer for RESET# input	Due to device availability the single buffer IC has been replaced by a single transistor circuit.	Uses SN74LV1T125 buffer IC (IC9)	Uses SN74LV1T125 buffer IC (IC9)	Uses circuit with transistor BC847C (TR4)
11	Signal buffer for EVTO0 output	Due to device availability the single buffer IC has been replaced by a dual transistor circuit.	-	Uses SN74LV1T126 buffer IC (IC11)	Uses circuit with 2 transistors SSM6N7002KFU (TR11)
12	Signal buffer for AURORES# input	Due to device availability the single buffer IC has been replaced by a dual transistor circuit.	Uses SN74LV1T125 buffer IC (IC6)	Uses SN74LV1T125 buffer IC (IC6)	Uses circuit with 2 transistors SSM6N7002KFU (TR2)
13	Signal buffer for FLMD0 input	Due to device availability the single buffer IC has been replaced by a dual transistor circuit.	Uses SN74LV1T126 buffer IC (IC13)	Uses SN74LV1T126 buffer IC (IC13)	Uses circuit with 2 transistors SSM6N7002KFU (TR5)

1.5 Piggyback Board Views

Following figures provide the top and bottom views of the piggyback board.

Note: The figures show the board with all assembled components. Not all components are assembled at all board versions at shipment.

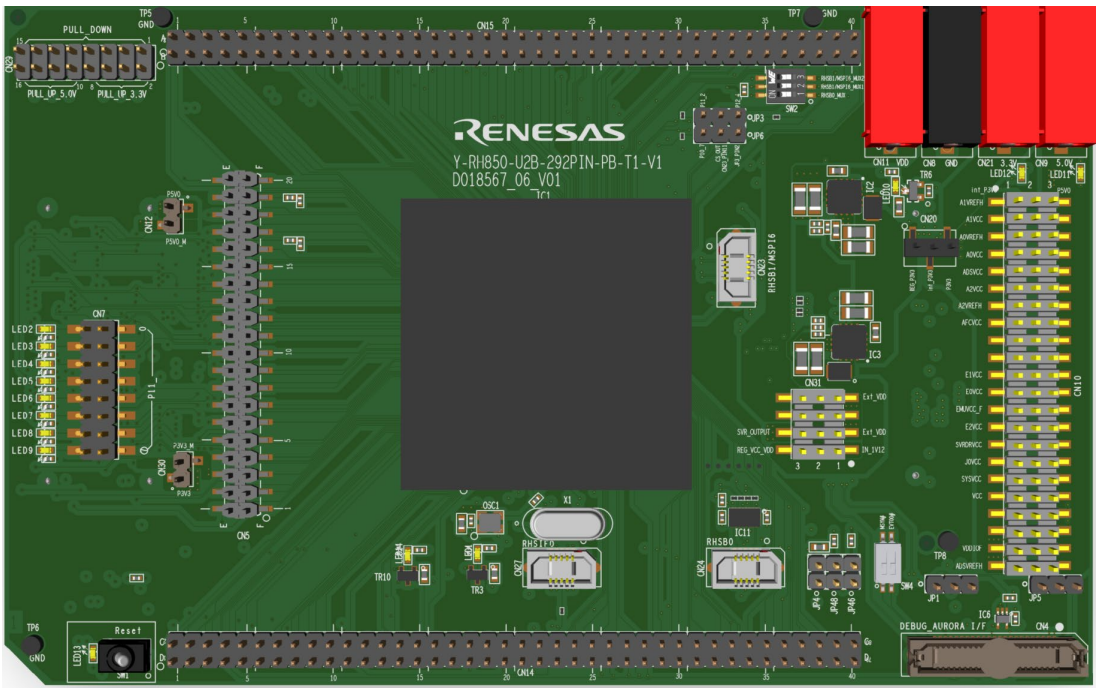


Figure 1.1 D018567_06_V01 Piggyback board top view

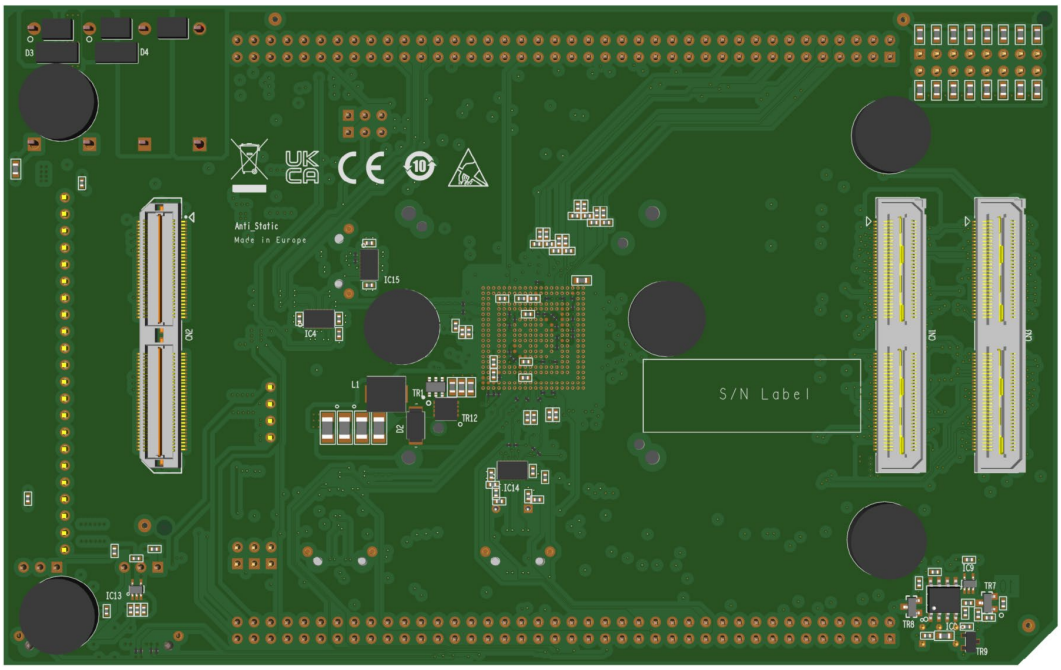


Figure 1.2 D018567_06_V01 Piggyback board bottom view

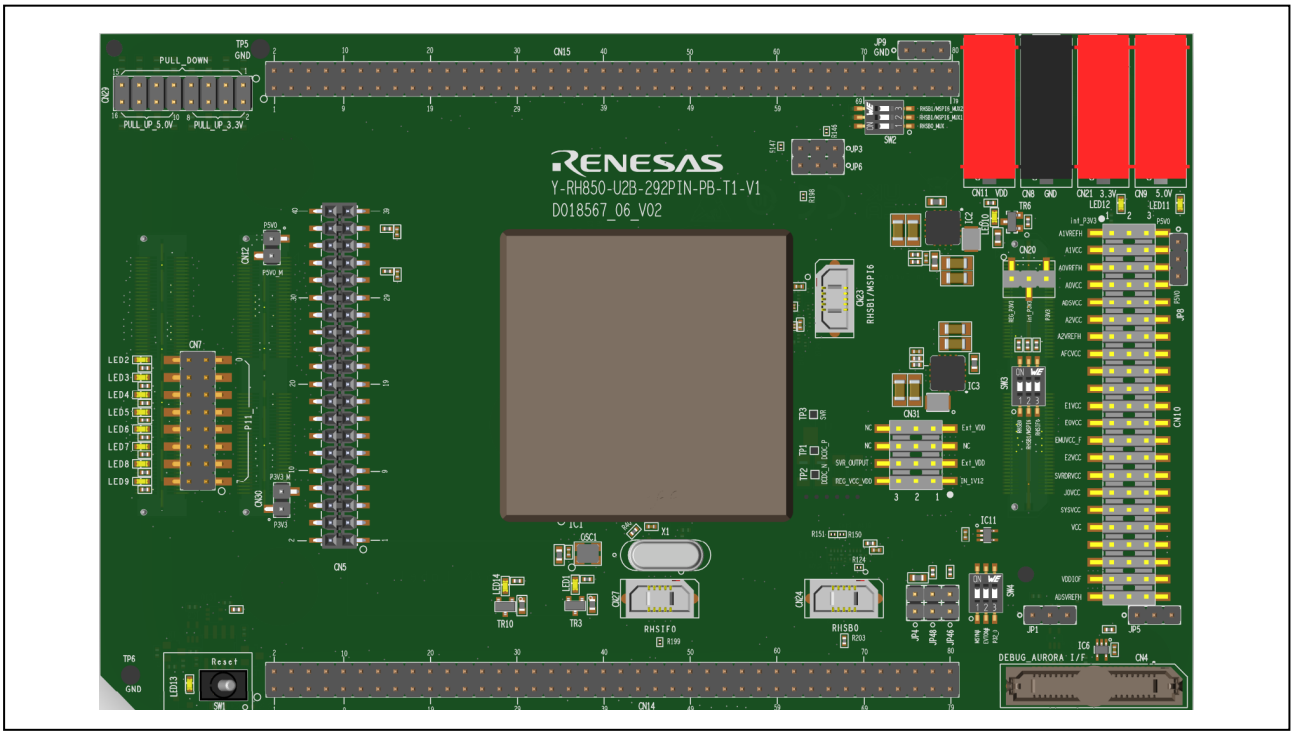


Figure 1.3 D018567_06_V02 Piggyback board top view

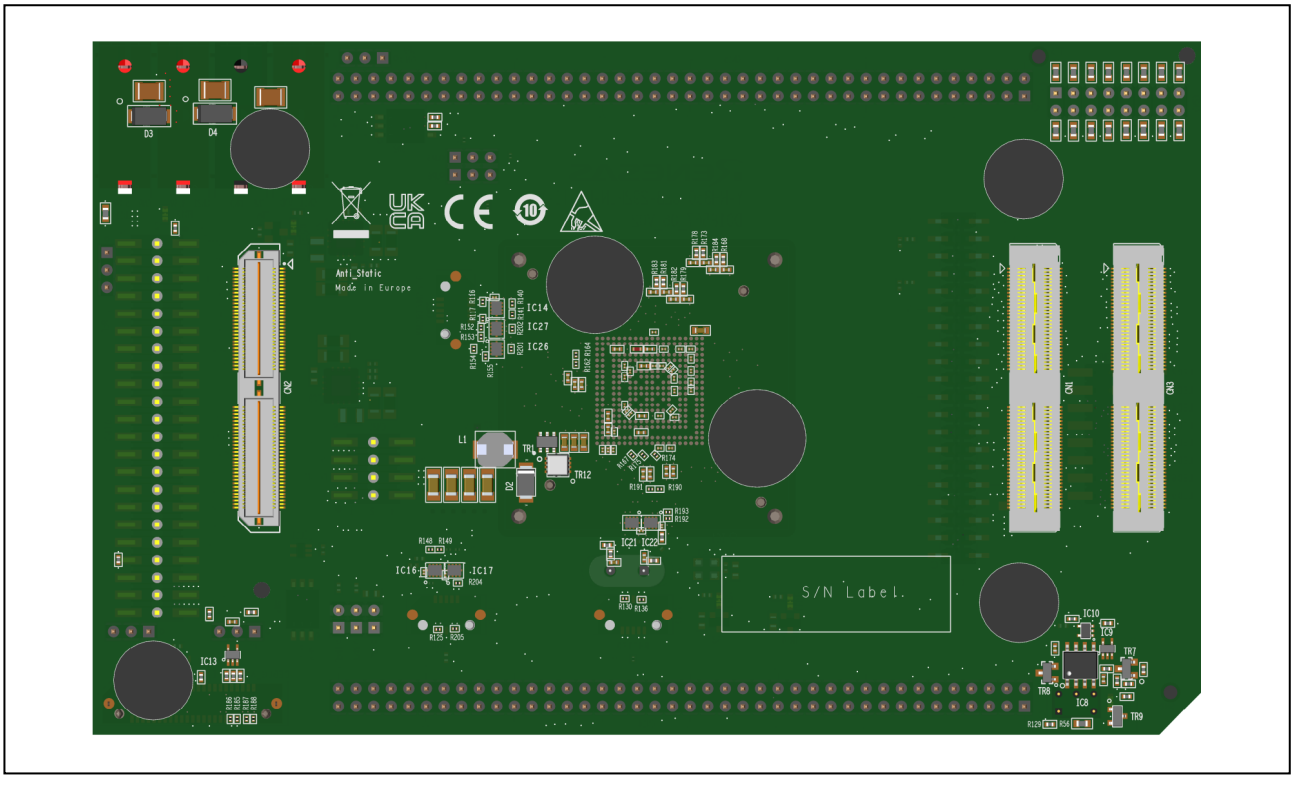


Figure 1.4 D018567_06_V02 Piggyback board bottom view

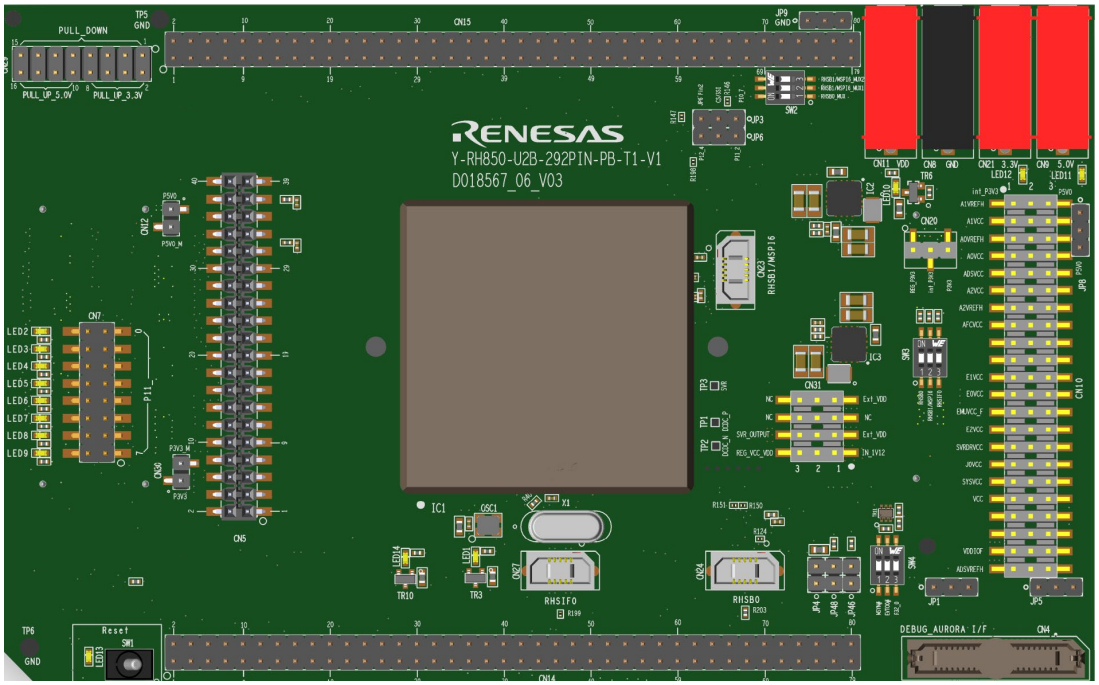


Figure 1.5 D018567_06_V03 Piggyback board top view

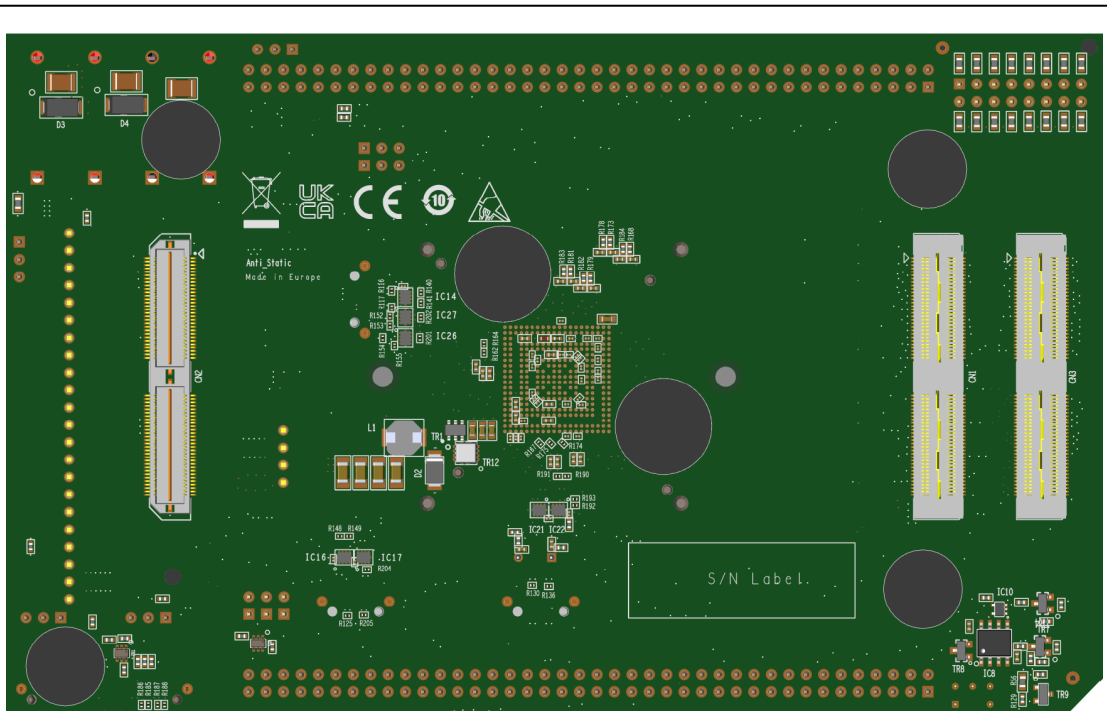


Figure 1.6 D018567_06_V03 Piggyback board bottom view

Following figures provide the drawing of top and bottom views of the piggyback board.

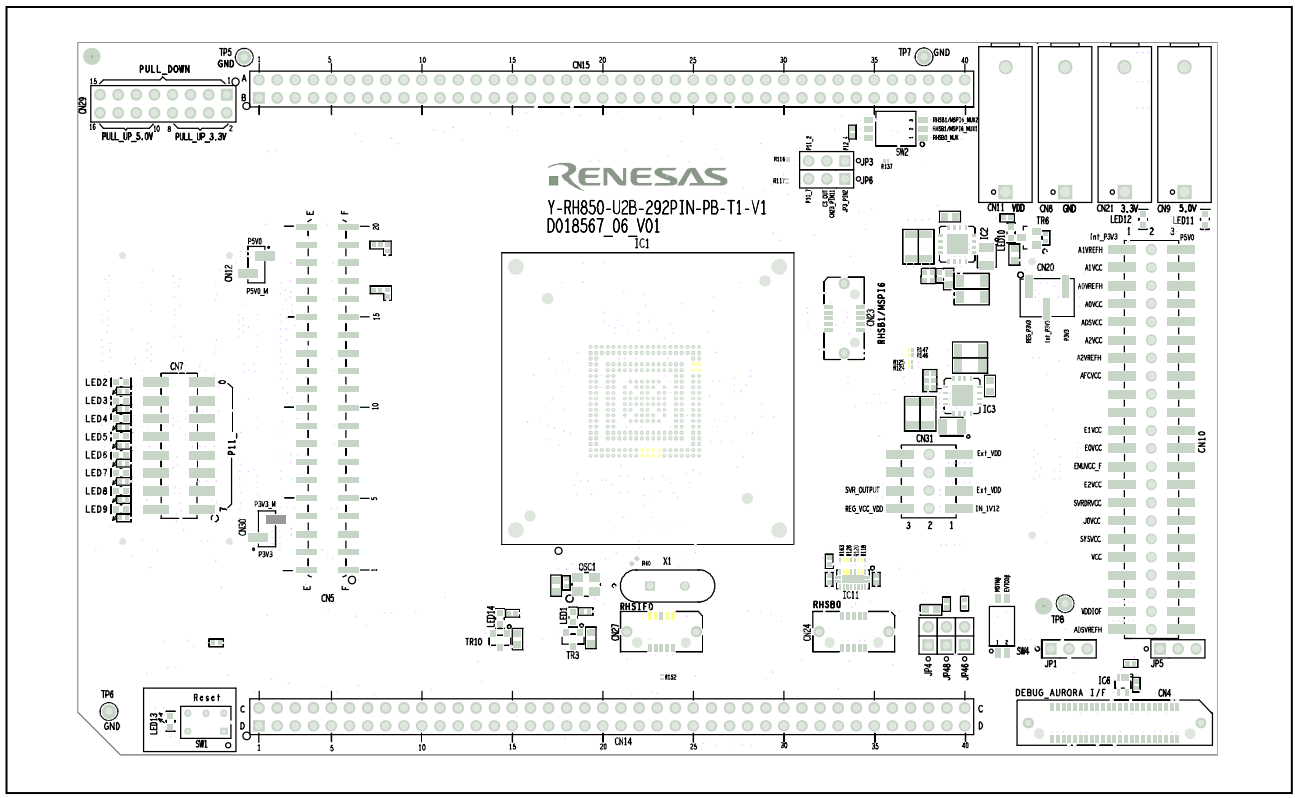


Figure 1.7 D018567_06_V01 Piggyback board top view

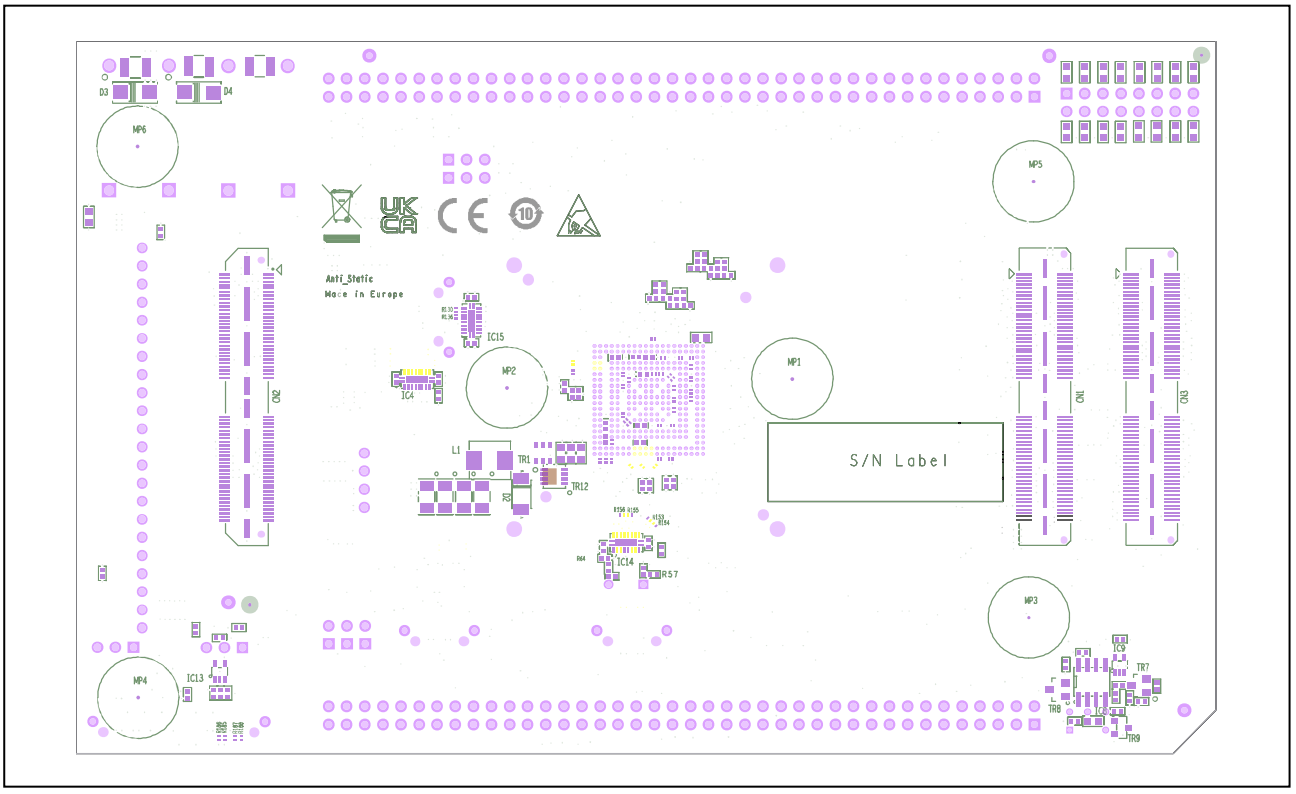


Figure 1.8 D018567_06_V01 Piggyback board bottom view

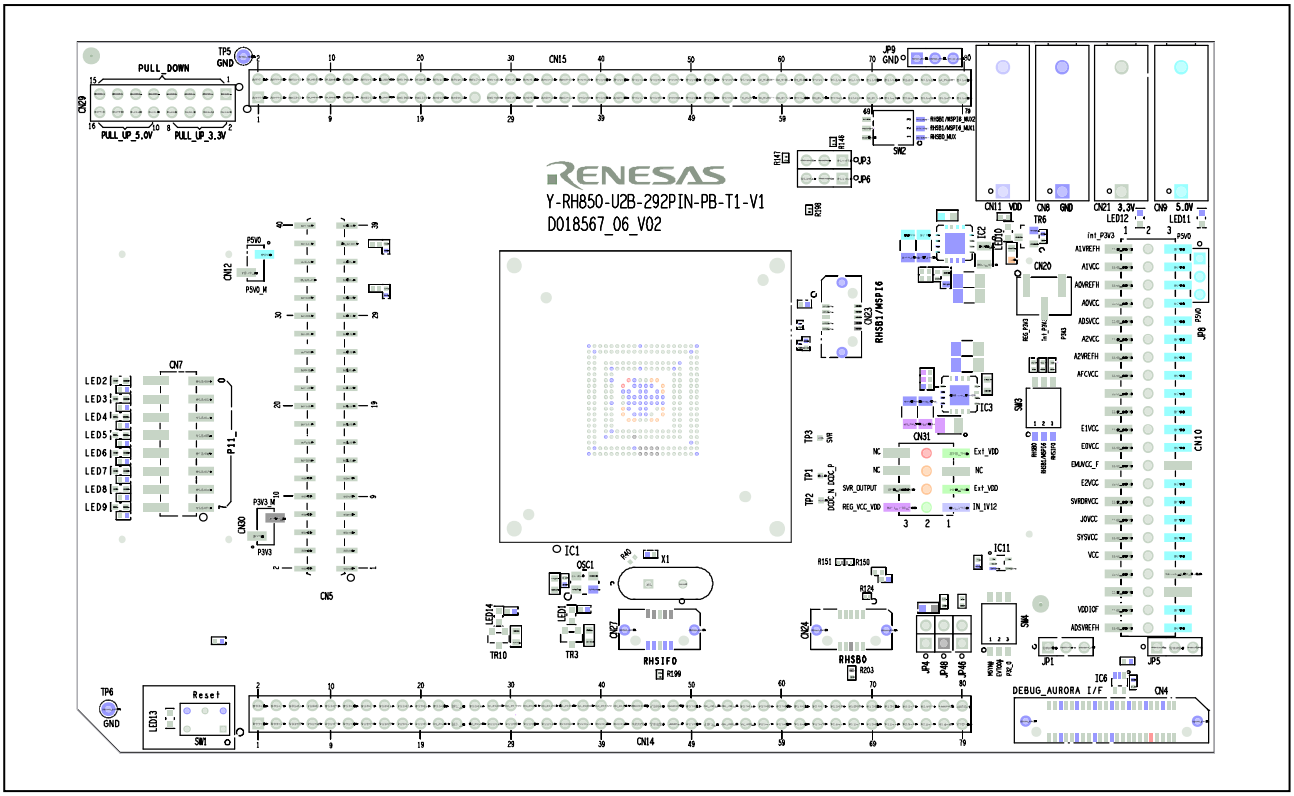


Figure 1.9 D018567_06_V02 Piggyback board top view

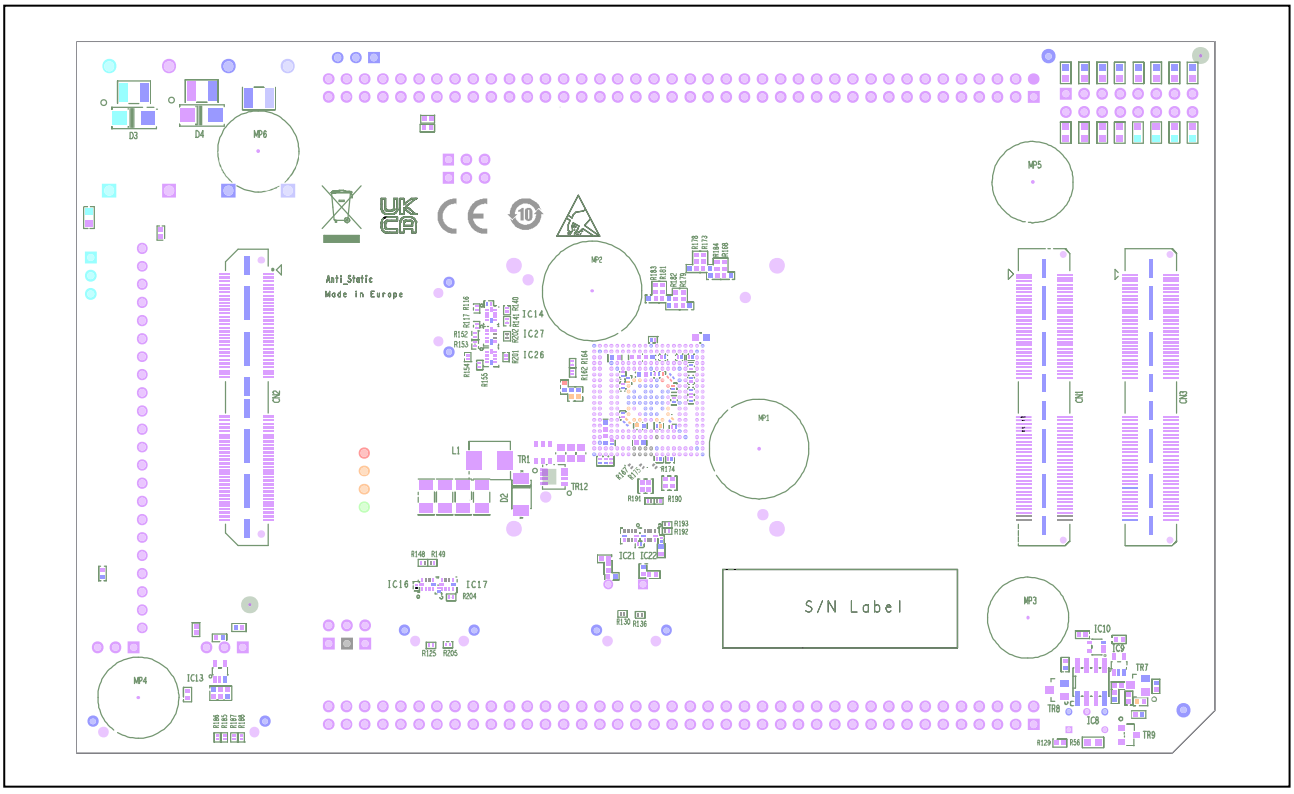


Figure 1.10 D018567_06_V02 Piggyback board bottom view

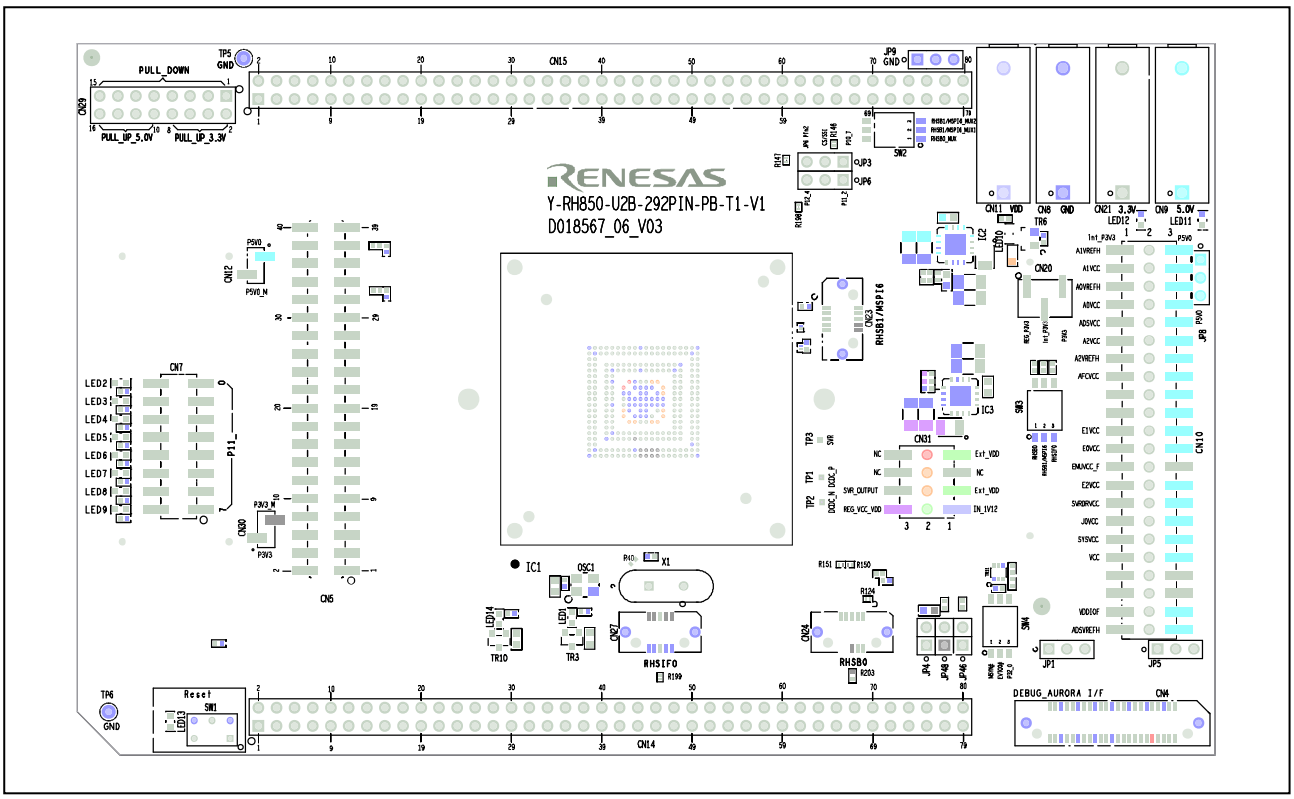


Figure 1.11 D018567_06_V03 Piggyback board top view

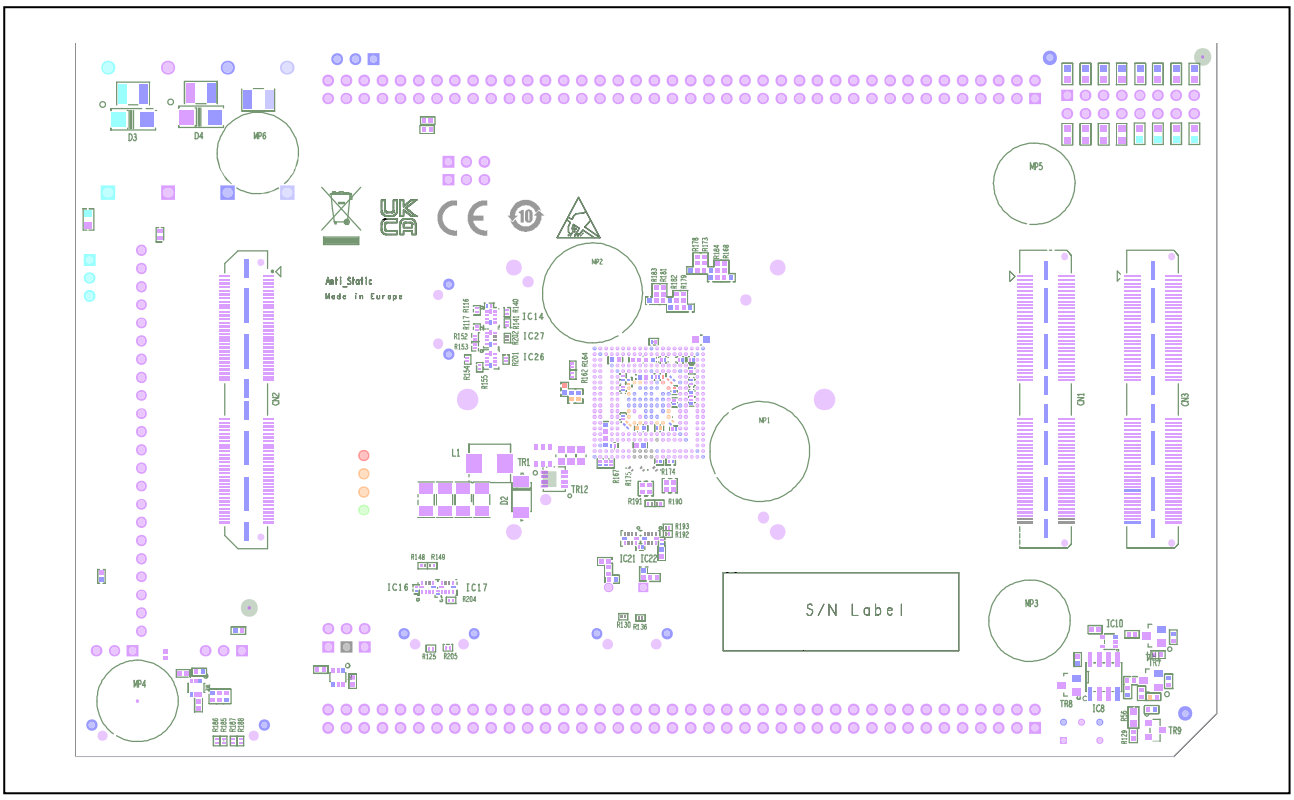


Figure 1.12 D018567_06_V03 Piggyback board top view

1.6 Mounting of the Device

The board is designed for use with the following devices.

Table 1.4 Type names for FCC and MP devices

	FCC device	MP device	Comments
RH850/U2B6	R7F702Z2*EDBB	R7F70255*FABB-C R7F70255*AFABB-C R7F70255*BFABB-C	FCC: Sixth through ninth characters of the part name indicate U2Bx-FCC(BGA292) PKG: The last 2 characters of the part name indicate BGA292.
RH850/U2B10	R7F702Z2*EDBB	R7F70254*FABB-C R7F70254*AFABB-C	

The device must be placed inside the socket IC1. To insert the device, align the device package A1 pin with the marking of the socket.
In below picture the A1 pin of the socket is marked with a circle. Please see also white point in *Figure 1.1 Piggyback board top view*.
On the device the index area is available on the corner near the A1 pin.

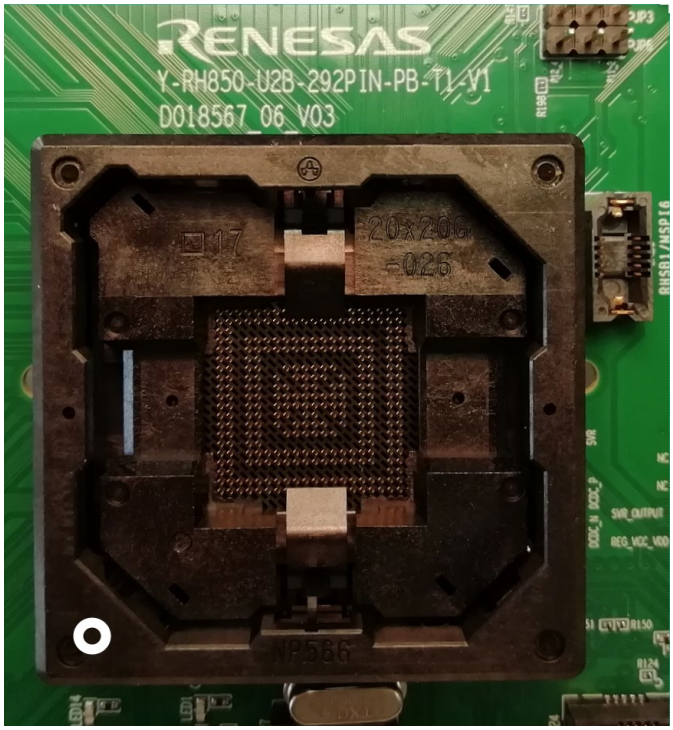


Figure 1.13 Yamaichi NP566-292-048-2 socket

CAUTION

Be careful with the device placement in the socket to avoid damage of the device.

2. Jumpers, Connectors, Switches and LEDs

This section provides complete lists of all jumpers, connectors and LEDs.

The placement of these components on the board is depicted in the figure below.

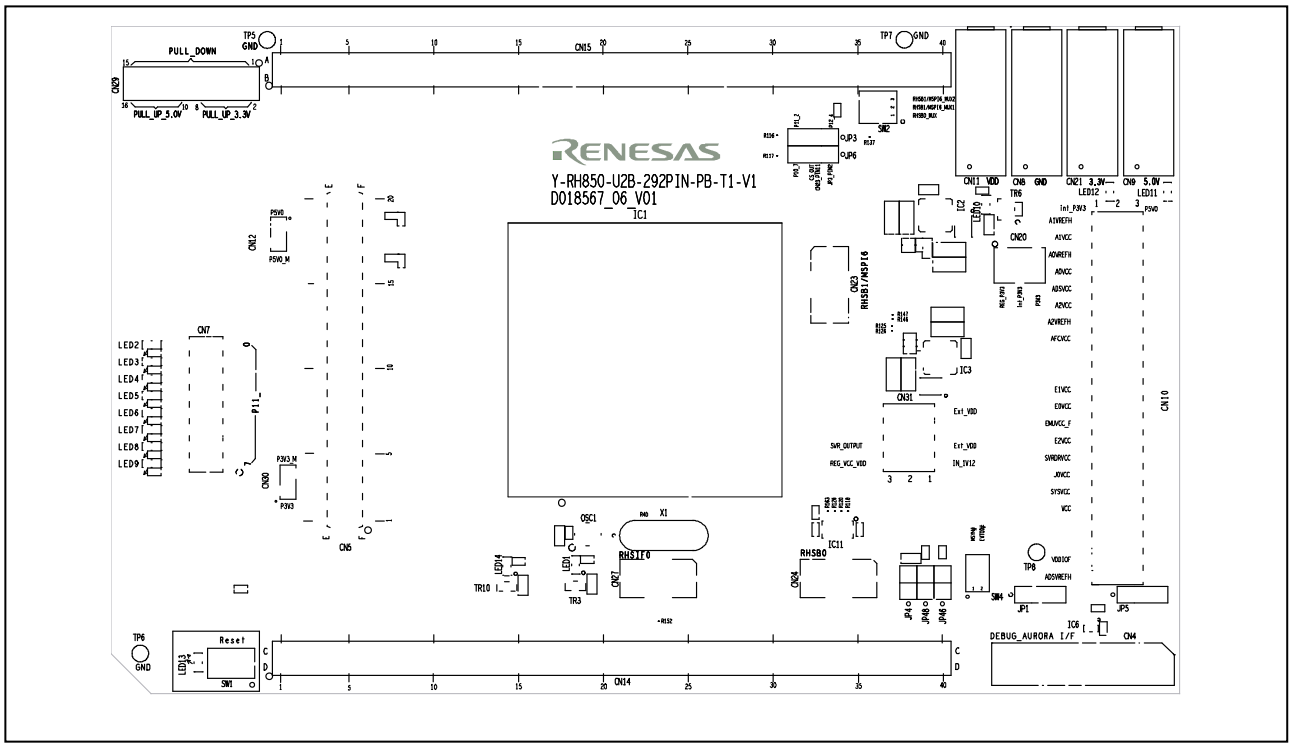


Figure 2.1 D018567_06_V01 Placement of jumpers, connectors and LEDs on top side

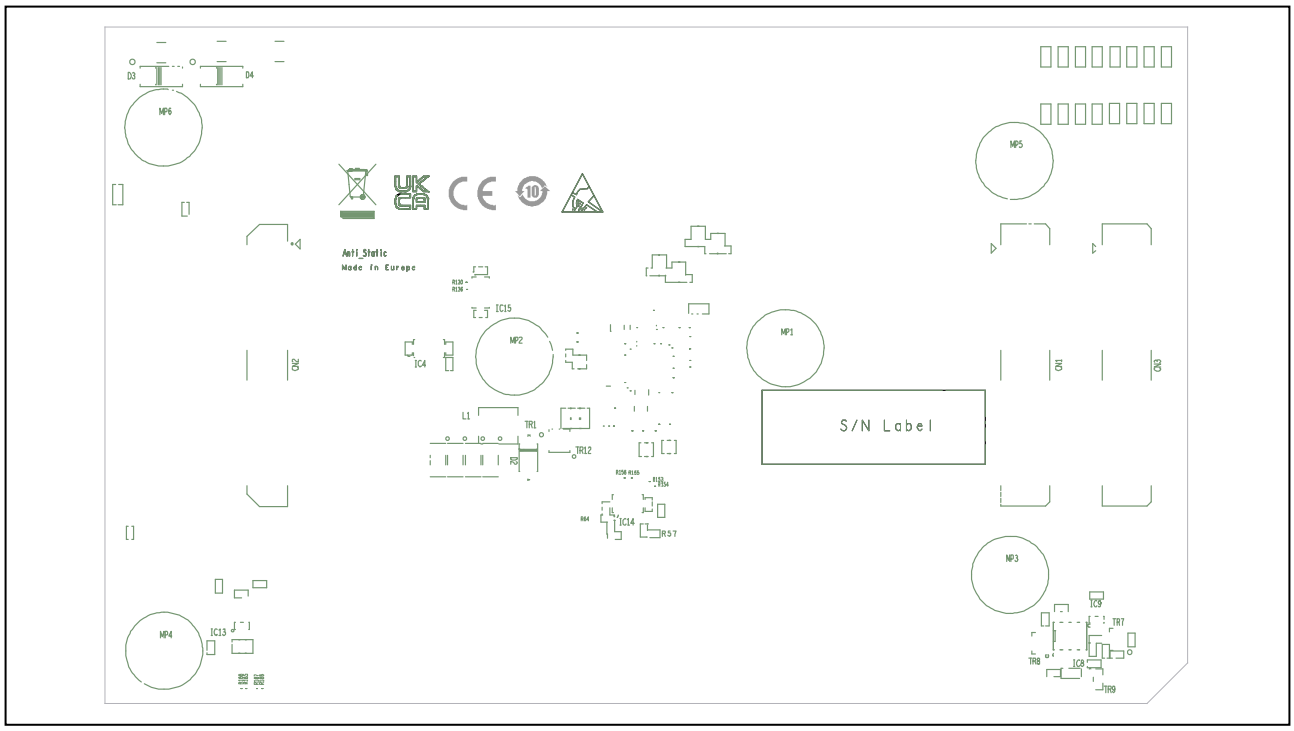


Figure 2.2 D018567_06_V01 Placement of connectors on bottom side

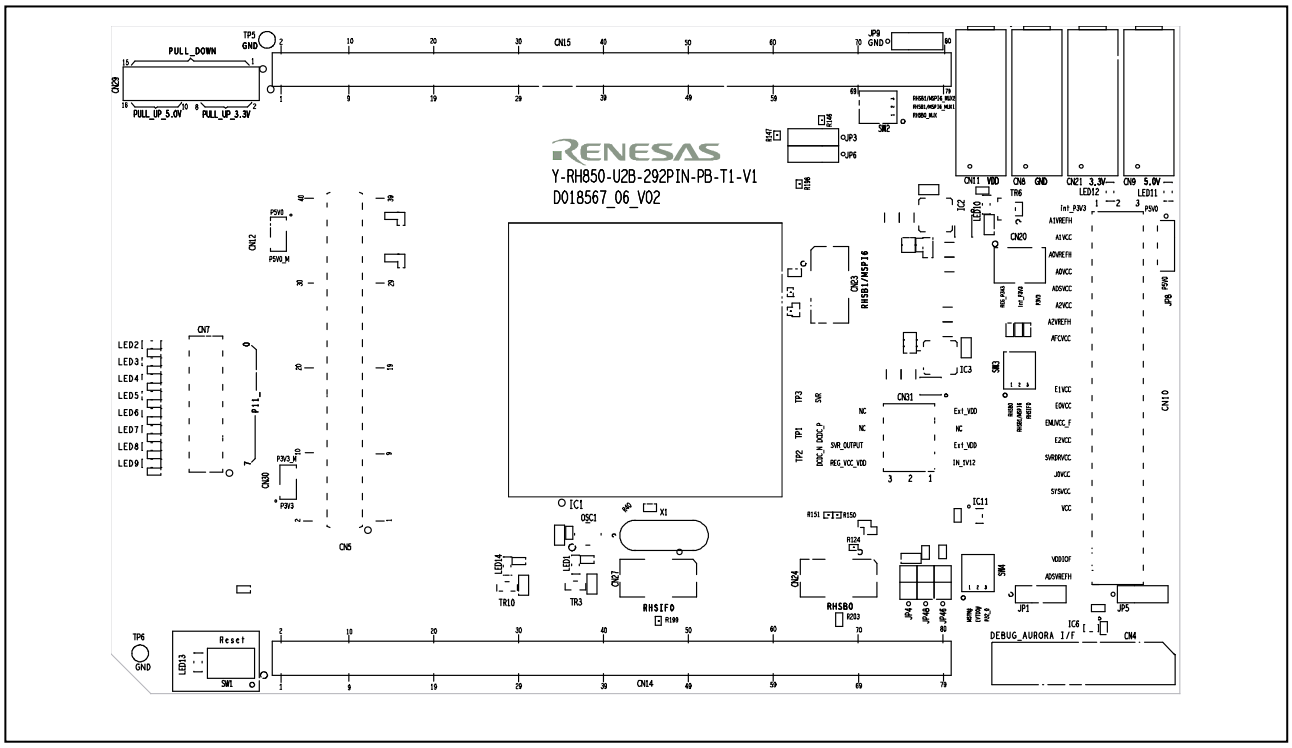


Figure 2.3 D018567_06_V02 Placement of jumpers, connectors and LEDs on top side

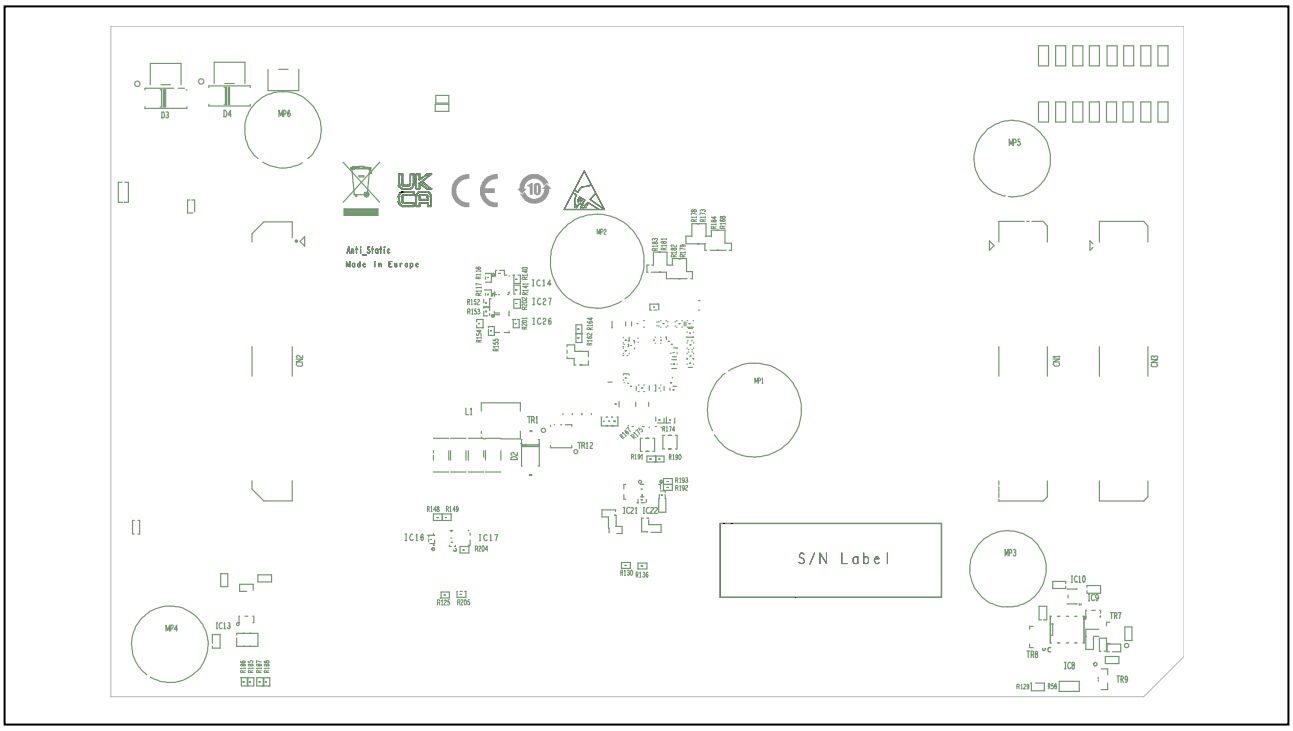


Figure 2.4 D018567_06_V02 Placement of connectors on bottom side

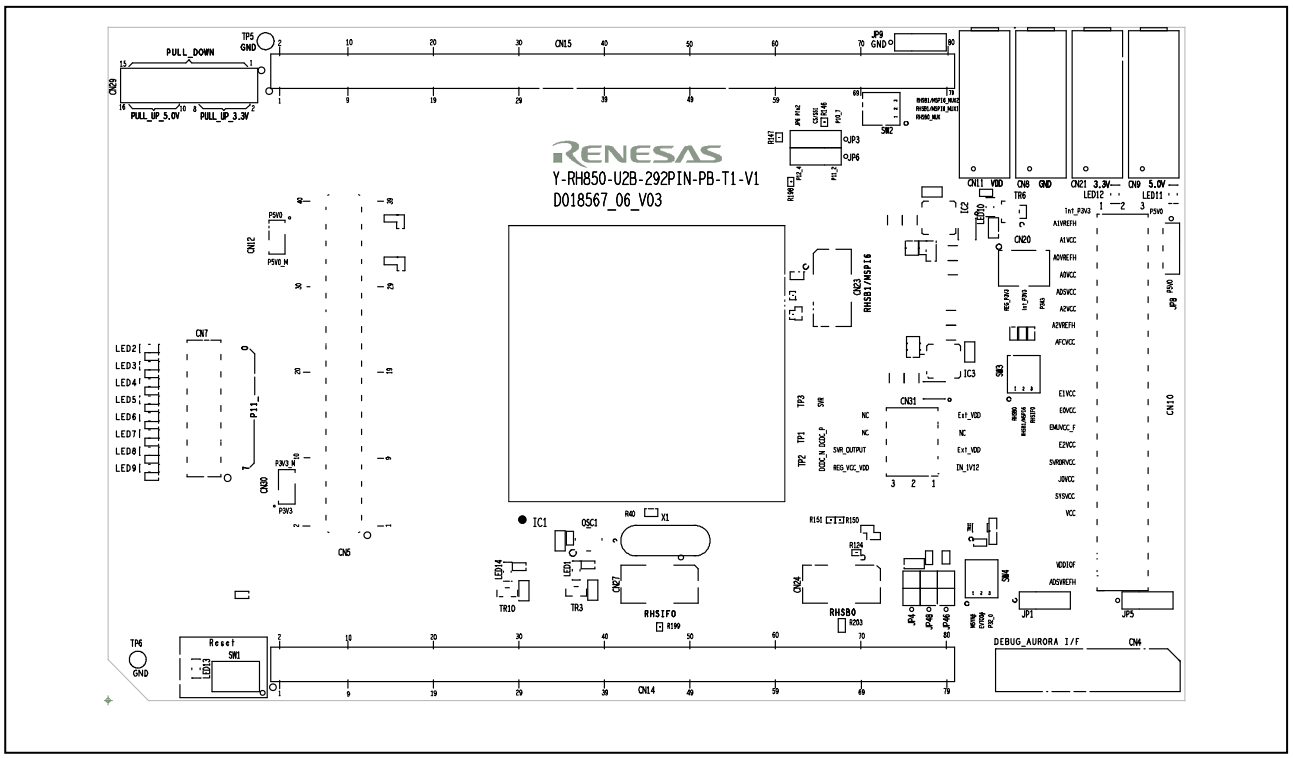


Figure 2.5 D018567_06_V03 Placement of connectors on top side

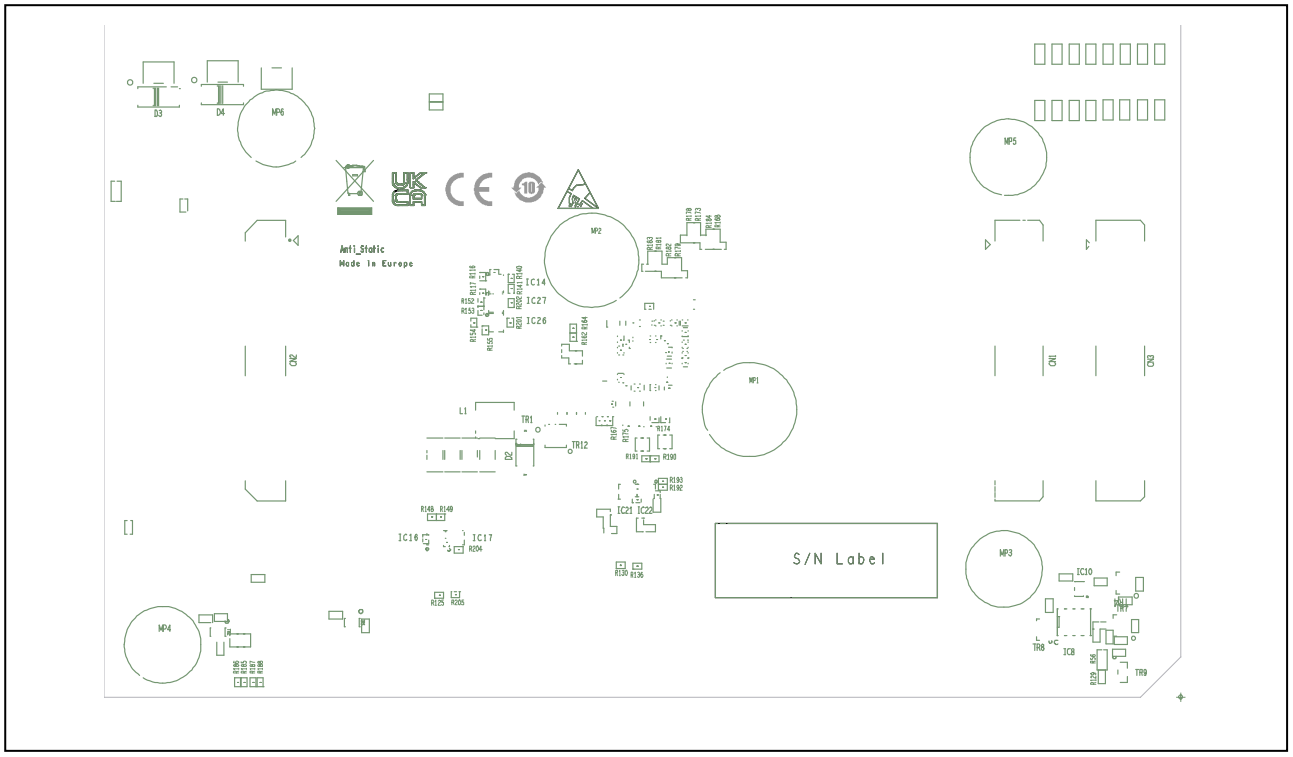


Figure 2.6 D018567_06_V03 Placement of connectors on bottom side

2.1 Jumper Overview

The following table provides an overview of all jumpers.

Table 2.1 Jumper overview

<table>
<tr><th>Jumper</th><th>Function</th><th>Remark</th></tr>
<tr><td>JP1</td><td>Select signal source for AURORES# input on RH850/U2B
• JP1[2-1]: TRST# signal from Aurora debug I/F connector CN4
• JP1[2-3]: AURORES# signal from Aurora debug I/F connector CN4</td><td>refer to 5 Debug and Flash Programming Interfaces and 8.2 Operation using FCC Device or Mass Production Device</td></tr>
<tr><td>JP3, JP6</td><td>JP3 and JP6 are cascaded to select MSPI6 signal connected to pin 6 on connector CN23.
On board D018567_06_V01
<table>
<tr><td>JP3</td><td>JP6</td><td>CN23.6pin</td></tr>
<tr><td>1-2</td><td>1-2</td><td>P12_4</td></tr>
<tr><td>2-3</td><td>1-2</td><td>P11_2</td></tr>
<tr><td>-</td><td>2-3</td><td>P10_7</td></tr>
</table>
On boards other than D018567_06_V01
<table>
<tr><td>JP3</td><td>JP6</td><td>CN23.6pin</td></tr>
<tr><td>1-2</td><td>-</td><td>P10_7</td></tr>
<tr><td>2-3</td><td>1-2</td><td>P11_2</td></tr>
<tr><td>2-3</td><td>2-3</td><td>P12_4</td></tr>
</table></td><td>refer to 6.6 Renesas High-Speed Bus RHSB1 and Multichannel Serial Peripheral Interface MSPI6 and 7.4 RHSB1/MSPI6 Connector CN23</td></tr>
<tr><td>JP4</td><td>Swap TX and RX signals of RHSIF0 interface available at CN27</td><td>refer to 6.7 Renesas High-Speed Serial I/F RHSIF0</td></tr>
<tr><td>JP5</td><td>Select signal source for TRST# signal
• JP5[1-2]: Fix TRST# signal to SYSVCC
• JP5[2-3]: TRST# signal is TRST input from Aurora debug interface connector (pin 12 on connector CN4)</td><td>refer to 5 Debug and Flash Programming Interfaces</td></tr>
<tr><td>JP8</td><td>5.0V pin header</td><td rowspan="2">available at board versions other than D018567_06_V01
refer to 3.2 Voltage Distribution</td></tr>
<tr><td>JP9</td><td>GND pin header</td></tr>
<tr><td>JP46</td><td>Change FLMD0 signal to “H”.</td><td rowspan="2">refer to 6.1 Operation Mode Selection</td></tr>
<tr><td>JP48</td><td>Change FLMD1 signal to “H”.</td></tr>
<tr><td>CN7</td><td>Enable LED outputs</td><td>refer to 6.3 Signaling LEDs</td></tr>
<tr><td>CN10</td><td>Select +3.3 V / +5.0 V power supply configuration</td><td>refer to 3.2 Voltage Distribution</td></tr>
<tr><td>CN12</td><td>Enable +5.0 V power supply from main board</td><td>refer to 3.1 Board Power Connection</td></tr>
<tr><td>CN20</td><td>Select +3.3 V power supply source
• CN20[1-2]: Get 3.3 V from onboard voltage regulator
• CN20[2-3]: Get 3.3V from external power supply CN21 or from main board</td><td>refer to 3.2 Voltage Distribution</td></tr>
<tr><td>CN30</td><td>Enable +3.3 V power supply from main board</td><td>refer to 3.1 Board Power Connection</td></tr>
<tr><td>CN31</td><td>Device core voltage configuration</td><td>refer to 3.3 Device Core Voltage (VDD) Selection</td></tr>
</table>

2.2 Connector Overview

The following table provides an overview of all connectors.

Table 2.2 Connector overview (cont'd)

Connector	Function	Remark
CN1	Main board connectors	refer to *7.1 Connectors to the Main Board CN1 to CN3*
CN2		
CN3		
CN4	Debug connector	refer to *5 Debug and Flash Programming Interfaces* and *7.2 Debug Connector* CN4
CN5	Device ports connector	refer to *7.3 Device Ports Connectors CN5, CN14 and CN15*
CN7	Signaling LEDs pin header	refer to *6.3 Signaling LEDs*
CN8	GND external power supply	refer to *3.1 Board Power Connection*
CN9	+5.0 V external power supply	
CN10	+3.3 V / +5.0 V power supply configuration	refer to *3.2 Voltage Distribution*
CN11	+1.12 V external power supply	refer to *3.1 Board Power Connection*
CN12	+5.0 V power supply from main board	
CN14	Device ports connector	refer to *7.3 Device Ports Connectors CN5, CN14 and CN15*
CN15		
CN20	+3.3 V power supply configuration	refer to *3.2 Voltage Distribution*
CN21	+3.3 V external power supply	refer to *3.1 Board Power Connection*
CN23	RHSB1 / MSPI6 interface connector	*refer to 6.6 Renesas High-Speed Bus RHSB1 and Multichannel Serial Peripheral Interface MSPI6*
CN24	RHSB0 interface connector	refer to *6.5 Renesas High-Speed Bus RHSB0*
CN27	RHSIF0 interface connector	refer to *6.7 Renesas* High-Speed Serial I/F RHSIF0
CN29	Pull up / pull down configuration	refer to *6.4 Pull-Up/Pull-Down Pin Header*
CN30	+3.3 V power supply from main board	refer to *3.1 Board Power Connection*
CN31	Device core voltage configuration	refer to *3.3 Device Core Voltage (VDD) Selection*

2.3 Switches Overview

The following table provides an overview of all switches.

Table 2.3 Switches overview

Connector	Function	Remark
SW1	RESET#	refer to *6.2 RESET Switch*
SW2	Port selection RHSB0 / RHSB1 / MSPI6	refer to *6.5 Renesas High-Speed Bus RHSB0* and *6.6 Renesas High-Speed Bus RHSB1 and Multichannel Serial Peripheral Interface MSPI6*
SW3 [1)]	Enable control for RHSB0 / RHSB1 / MSPI6 multiplexers.	
SW4	Debug port connection EVTO0 / MSYN#	refer to *5 Debug and Flash Programming Interfaces* and *8.2 Operation using FCC Device or Mass Production Device*

[1)] On board versions other than D018567_06_V01

2.4 LED Overview

The following table provides an overview of all LED.

Table 2.4 LED overview

LED	Function	Color	Remark
LED1	Device ERROROUT_M# signal	red	
LED2	Signaling LED	yellow	connection via CN7, refer to *6.3 Signaling LEDs*
LED3	Signaling LED		
LED4	Signaling LED		
LED5	Signaling LED		
LED6	Signaling LED		
LED7	Signaling LED		
LED8	Signaling LED		
LED9	Signaling LED		
LED10	1.12 V device core voltage VDD	green	refer to *3.4 Power Supply LEDs*
LED11	5.0 V power supply P5V0	green	
LED12	3.3 V power supply int_P3V3	green	
LED13	Reset switch SW1 on	red	refer to *6.2 RESET Switch*
LED14	Device VMONOUT# signal	red	

3. Power Supply

3.1 Board Power Connection

The device and the board require various power supply voltages:

- 3.3 V for most of the digital circuitry on the device and on the board
- 5.0 V in case some ports shall be operated with 5.0 V I/O voltage
- 1.12 V for the device's VDD core voltage supply
  Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

Note

Within this document all voltage values are considered as 'typical'.

Refer to the 'Electrical Characteristics' section of the Hardware User's Manual for allowed voltage ranges.

The following connectors are available to supply external voltages:

- Four 4 mm 'banana-type' connectors are used to connect external power supplies:
  - black connector CN8 for GND (VSS)
  - red connector CN9 for 5 V
  - red connector CN21 for 3.3 V
  - red connector CN11 for 1.12 V
    Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
    Connector CN11 is not assembled at delivery of the board, but separately supplied with the board package.

In case the piggyback board is mounted on a main board, all voltages except for 1.12 V (VDD) can be supplied by the main board. The jumpers CN12 (5.0 V) and CN30 (3.3 V) are used to enable power supply from main board.

CAUTION

Do not power on the piggyback board when no RH850 microcontroller is installed in socket IC1 because the switching regulator in the SVR power supply circuit doesn't have defined control signals when the microcontroller is not installed and may be damaged.

If you want to power on the piggyback board without microcontroller, make sure jumper CN10[43-44-45] (SVRDRVCC) is open.

If the piggyback board is being used with the microcontroller installed please make sure the ports SVRNGATE and SVRPGATE are set to "Fixed" (output) in bit SVRENDCDCHZ in option byte 25.

Do not supply the 5 V (CN9) and 3.3 V (CN21) voltage directly to the piggyback board in case if the power supply from the main board is enabled.

Connecting external 1.12 V via CN11 (and GND via CN8) is still an option also in this case.

For some general power supply scenarios, the jumper settings are described in *8 Jumper Configuration Examples*.

3.2 Voltage Distribution

The following table shows the required device power supply pins and their function:

Table 3.1 Device power supply pins

Device power supply pin	Voltage	Function
E0VCC, E1VCC, E2VCC	3.3 V, 5 V	Power supply for I/O ports
EMUVDD	1.09 V	Power supply for debug circuits, only available on FCC devices
EMUVCC_F	3.3 V	
J0VCC	3.3 V, 5 V	
SYSVCC	3.3 V, 5 V	Power supply for System Logic and internal voltage regulator power I/O ports
VCC	3.3 V, 5 V	Power supply for on-chip flash memory
SVRDRVCC	3.3 V, 5 V	Power supply for on-chip Switching Voltage Regulator (SVR)
SVRAVCC	3.3 V, 5 V	Connected to SYSVCC
LVDVCC	3.3V, 5V	RHSIF/RHSB supply voltage
OSCVCC	3.3 V, 5 V	Power supply for OSC
VDDIOF	3.3 V, 5 V	I/O voltage supply for the main board
A0VCC, A1VCC, A2VCC	3.3 V, 5 V	A/D Converter's power supplies and reference voltages
A0VREFH, A1VREFH, A2VREFH, ADSVREFH	3.3 V, 5 V	
ADSVCC, AFCVCC	3.3 V, 5 V	
VDD	1.12 V	Core supply voltage Refer to *3.3 Device Core Voltage (VDD) Selection*

Each of the above voltages can be selected from 5.0 V or 3.3 V (where applicable, see table above) by a set of jumpers.

The supply for 3.3 V can be selected from external power supply / main board power supply or from the onboard voltage regulator using jumper CN20:

- CN20 [1-2]: 3.3 V supply comes from the onboard voltage regulator.
- CN20 [2-3]: 3.3 V supply comes from the external power supply or from the main board power supply.

Table 3.2 Voltage Selection shows which jumpers to set to select the different device supply voltages, and *Figure 3.1 Voltage distribution* shows the schematic for it.

Table 3.2 Voltage Selection

Device power supply pin	Connection for 3.3 V	Connection for 5.0 V
A1VREFH	CN10 [1-2]	CN10 [2-3]
A1VCC	CN10 [4-5]	CN10 [5-6]
A0VREFH	CN10 [7-8]	CN10 [8-9]
A0VCC	CN10 [10-11]	CN10 [11-12]
ADSVCC	CN10 [13-14]	CN10 [14-15]
A2VCC	CN10 [16-17]	CN10 [17-18]
A2VREFH	CN10 [19-20]	CN10 [20-21]
AFCVCC	CN10 [22-23]	CN10 [23-24]
E1VCC	CN10 [31-32]	CN10 [32-33]
E0VCC	CN10 [34-35]	CN10 [35-36]
EMUVCC_F	CN10 [37-38]	---
E2VCC	CN10 [40-41]	CN10 [41-42]
SVRDRVCC	CN10 [43-44]	CN10 [44-45]
J0VCC	CN10 [46-47]	CN10 [47-48]
SYSVCC	CN10 [49-50]	CN10 [50-51]
VCC	CN10 [52-53]	CN10 [53-54]
VDDIOF	CN10 [61-62]	CN10 [62-63]
ADSVREFH	CN10 [64-65]	CN10 [65-66]

CN10

	int_P3V3		P5V0
A1VREFH	1	2	3
A1VCC	4	5	6
A0VREFH	7	8	9
A0VCC	10	11	12
ADSVCC	13	14	15
A2VCC	16	17	18
A2VREFH	19	20	21
AFCVCC	22	23	24
E1VCC	31	32	33
E0VCC	34	35	36
EMUVCC_F	37	38	39
E2VCC	40	41	42
SVRDRVCC	43	44	45
J0VCC	46	47	48
SYSVCC	49	50	51
VCC	52	53	54
VDDIOF	61	62	63
ADSVREFH	64	65	66

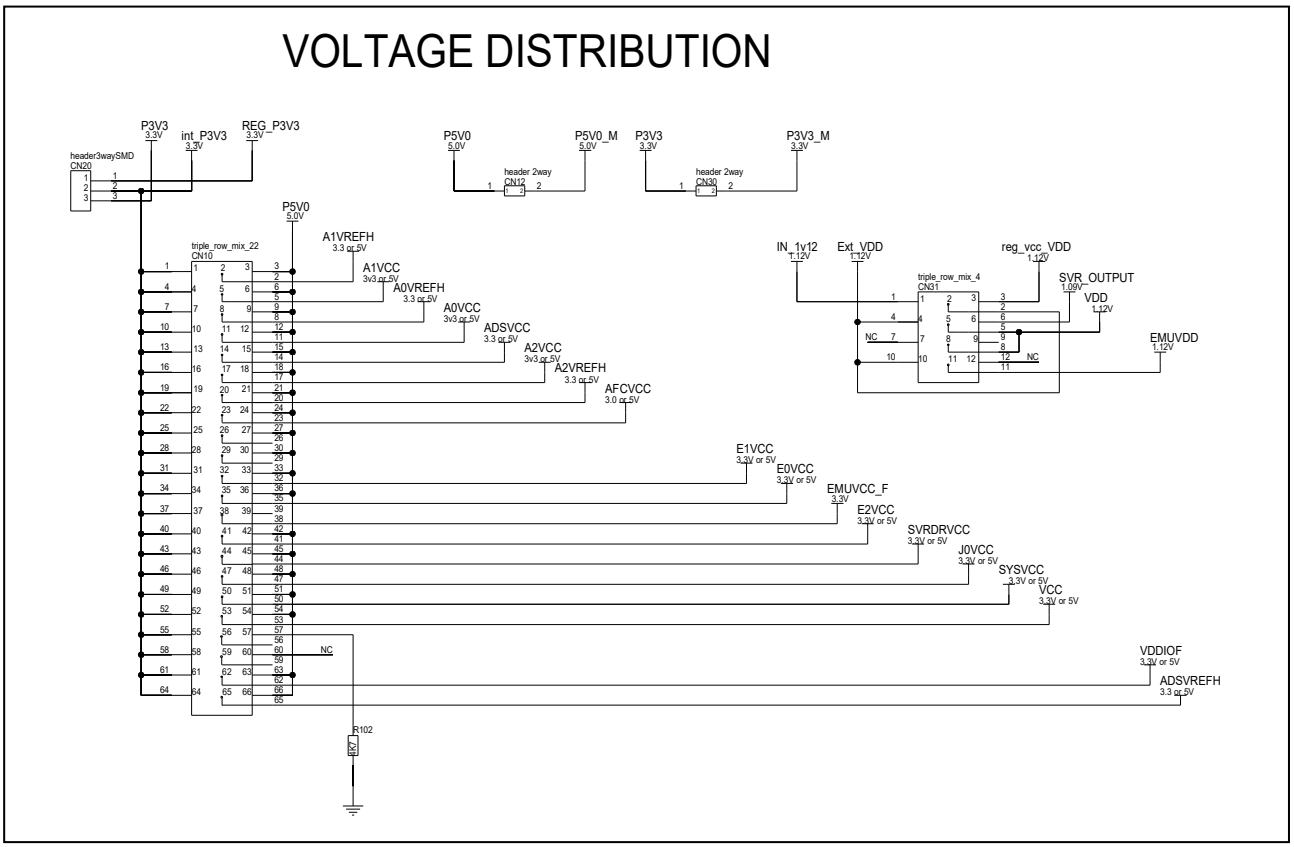


Figure 3.1 Voltage distribution on board version D018567_06_V01

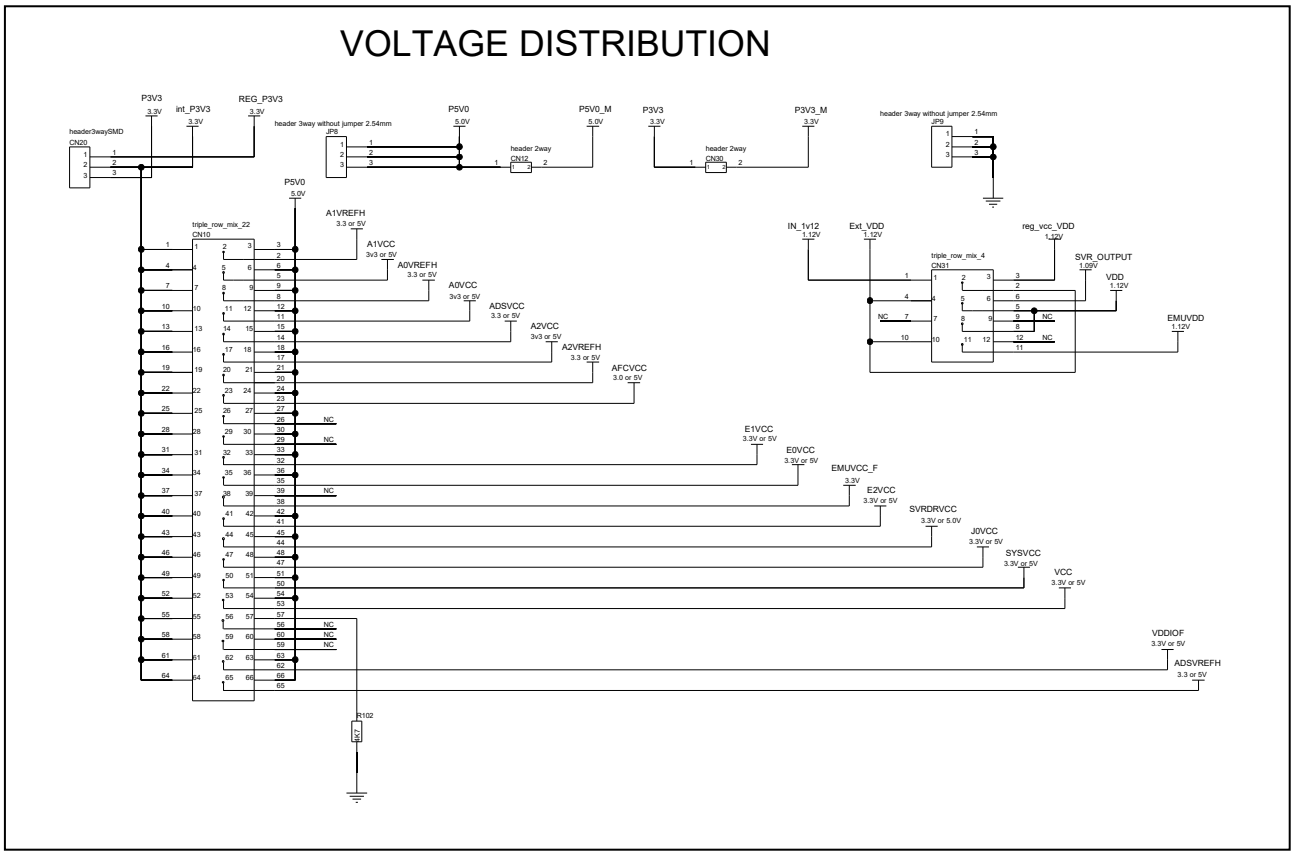


Figure 3.2 Voltage distribution on board versions other than D018567_06_V01

3.3 Device Core Voltage (VDD) Selection

The device core voltage VDD (typ.1.12 V) can be

- supplied from external via CN11 (voltage IN_1v12)
- generated from the P3V3 power rail by use of the on-board voltage regulator IC3 (voltage reg_vcc_VDD, only if 5.0V is supplied to the piggyback board)
- generated by the on-chip Switching Voltage Regulator (SVR) in combination with device external power transistors TR1, TR12 (voltage SVR_OUTPUT)

Note

The IN_1v12 and reg_vcc_VDD voltages have a level of typical 1.12 V, which is higher than the typical device core voltage VDD of 1.09 V. The 30 mV difference is supposed to compensate voltage drops over the power rails on the board, in particular over the jumpers.

Selection of the VDD source is achieved by use of the jumpers in CN31:

CN31[1-2]: Ext_VDD = IN_1v12

CN31[2-3]: Ext_VDD = reg_vcc_VDD

CN31[4-5]: VDD = Ext_VDD

CN31[5-6]: VDD = SVR_OUTPUT

CN31[10-11] enables the output of the supply voltage to the device debug circuit

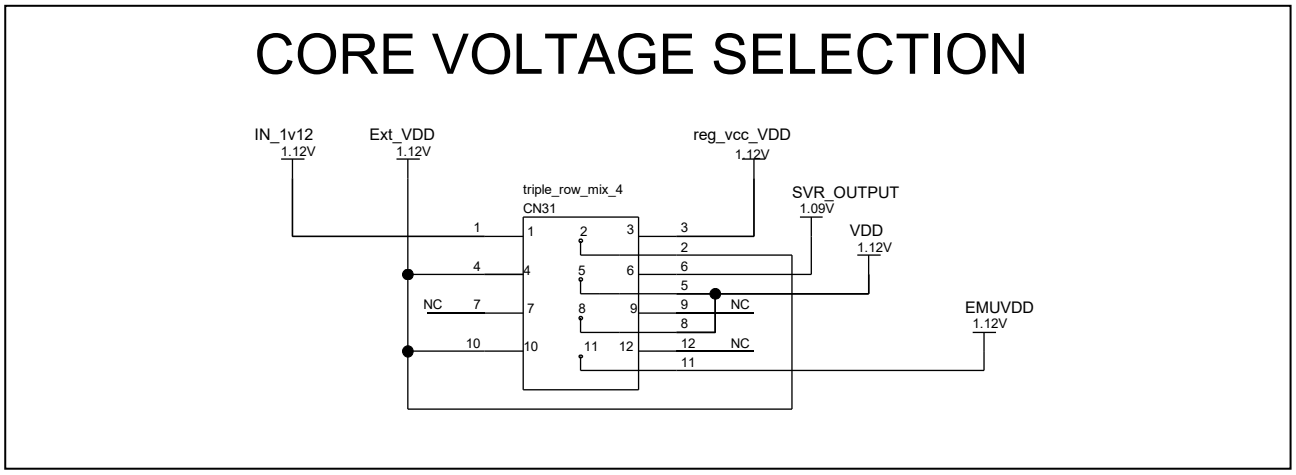


Figure 3.1 Device core voltage (VDD) selection

EMUVDD.

3.4 Power Supply LEDs

The following green LEDs indicate the presence of various voltages on the piggyback board:

- LED10 for 1.12 V device core voltage VDD
- LED11 for 5.0 V power rail P5V0
- LED12 for 3.3 V power rail P3V3

4. Clock Supply

The device's operation clock can be generated by

- the on-chip main oscillator circuit in combination with an off-chip resonator, connected to the X1, X2 terminals
- an off-chip oscillator, the clock is fed into the X1 terminal

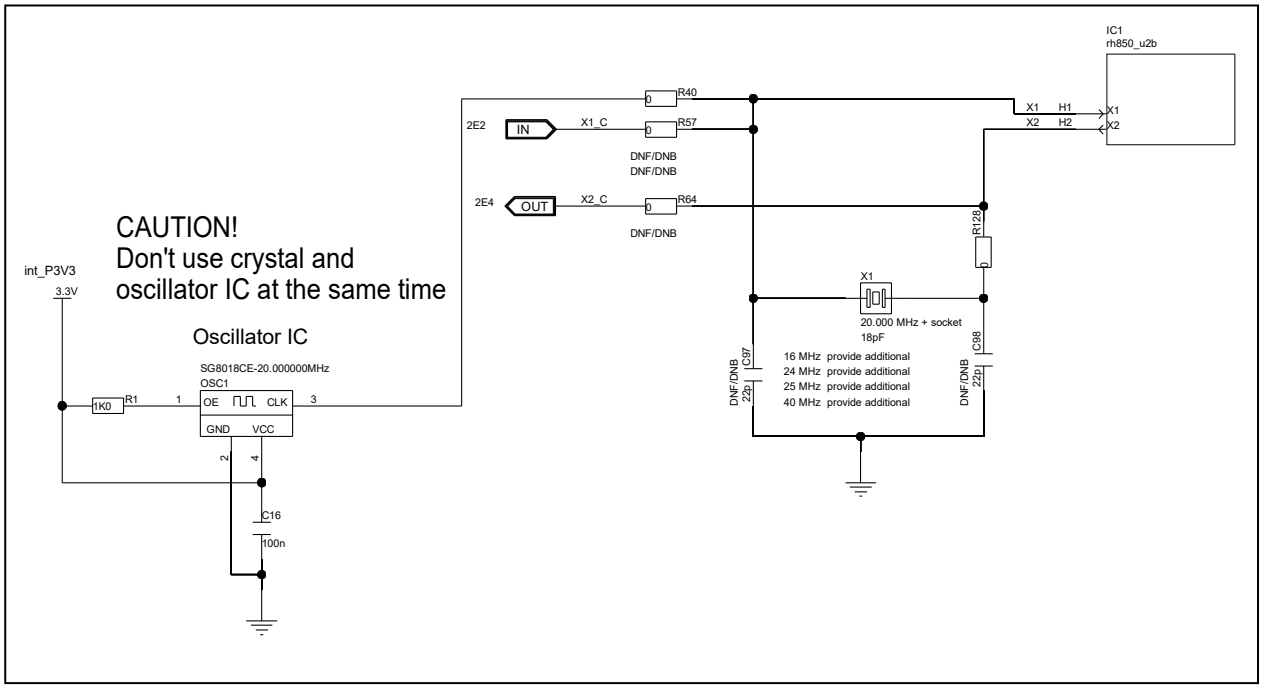


Figure 4.1 Clock supply

4.1 Main Oscillator

For operating the on-chip main oscillator the piggyback board provides a socket (X1) for a resonator.

Several resonators for various main oscillator frequencies (16 MHz, 20 MHz, 24 MHz, 25MHz, 40 MHz) are included in the board package.

The 20MHz resonator is by default mounted to X1.

For package content please refer to *1.1 Package Components*

CAUTION

Only one oscillator, either X1 or OSC1, can be used at any one time for the main oscillator.

4.2 Programmable Oscillator

Instead of using the on-chip main oscillator a programmable crystal oscillator (OSC1) circuit can be used on the board.

The available footprint and circuitry is designed for a SG-8018CE programmable crystal oscillator from Epson Toyocom. The output of this oscillator can be connected to X1 terminal via resistor R40.

For details about the available circuitry, refer to *Figure 4.1 Clock supply*.

CAUTION

A resonator mounted on socket X1 must not be used in parallel to another clock source.

4.3 Device Pins X1 and X2 on Connector CN14

To minimize disturbance on the resonator signal the device pins X1 and X2 are by default not connected to a pin header. If needed the pins can be connected to CN14 via 0 Ω resistors:

- Device pin X1: Connect to pin 23 of CN14 via R57 to supply an external clock to the device.
- Device pin X2: Connect to pin 24 of CN14 via R64 for measurement purposes of the clock.

5. Debug and Flash Programming Interfaces

For debugging and flash programming purposes debug and flash programming tools can be connected to the CN4 connector.

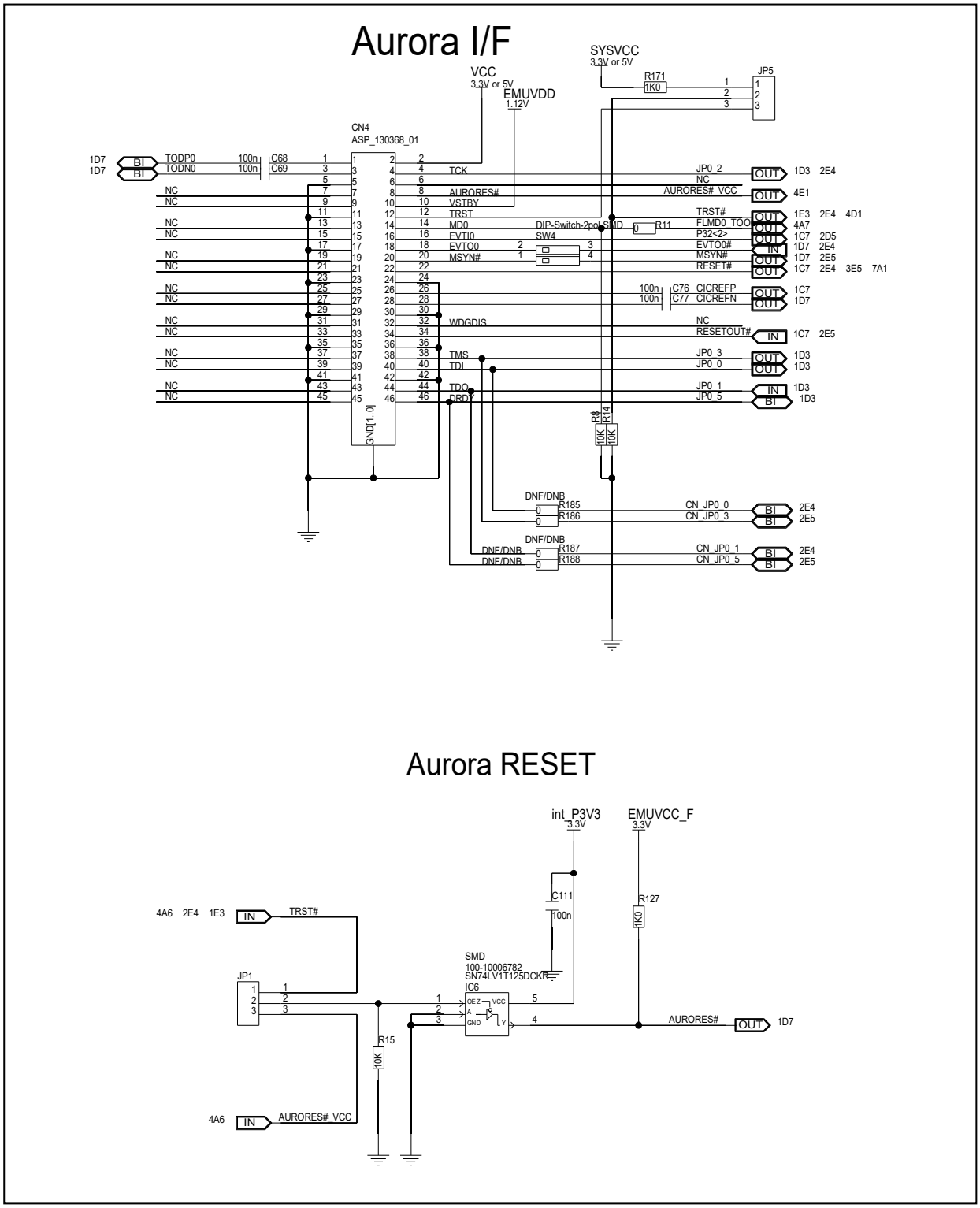


Figure 5.1 Debug connector CN4 and Aurora reset circuit on board version D018567_06_V01

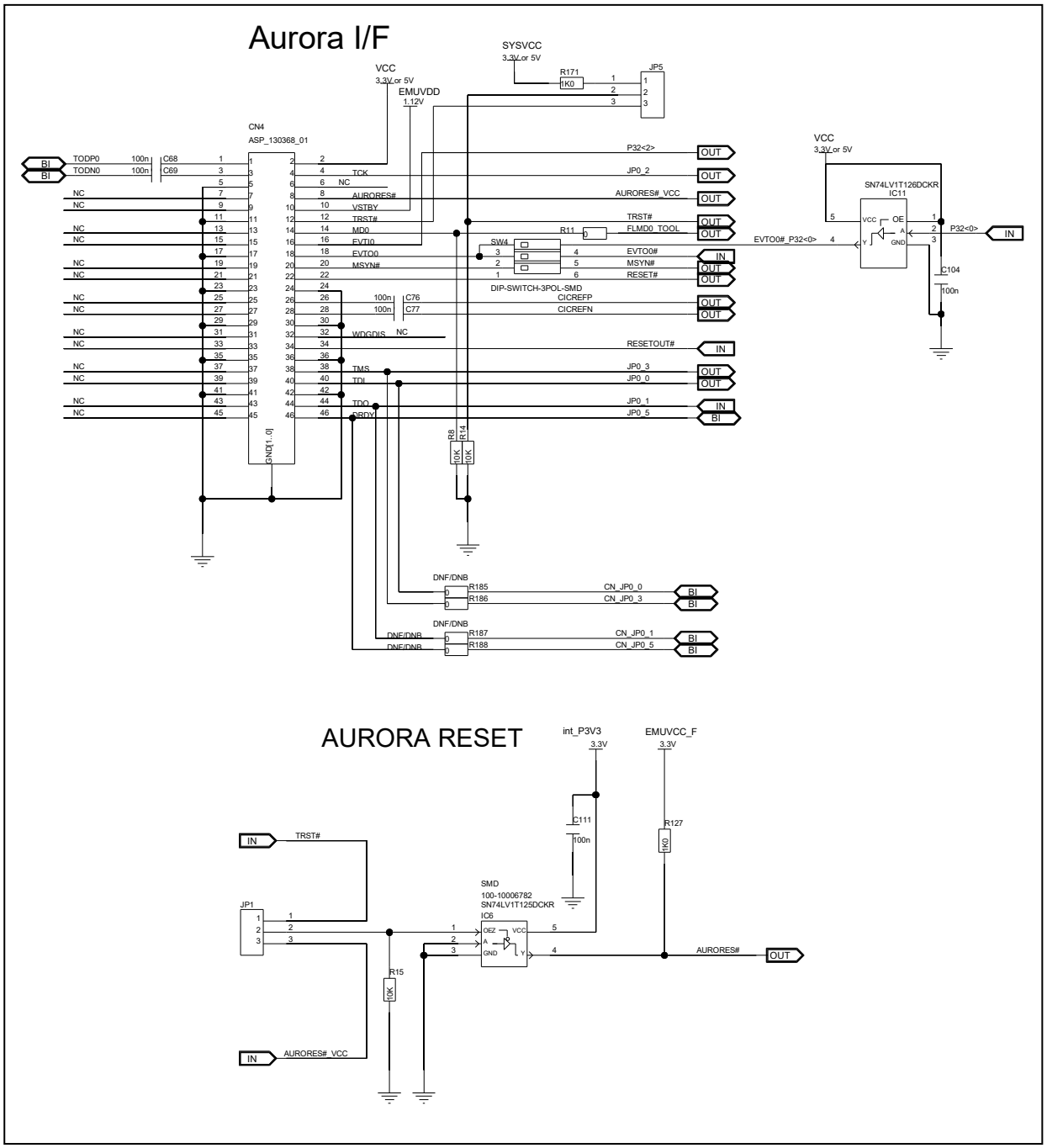


Figure 5.2 Debug connector CN4 and Aurora reset circuit on board version D018567_06_V02

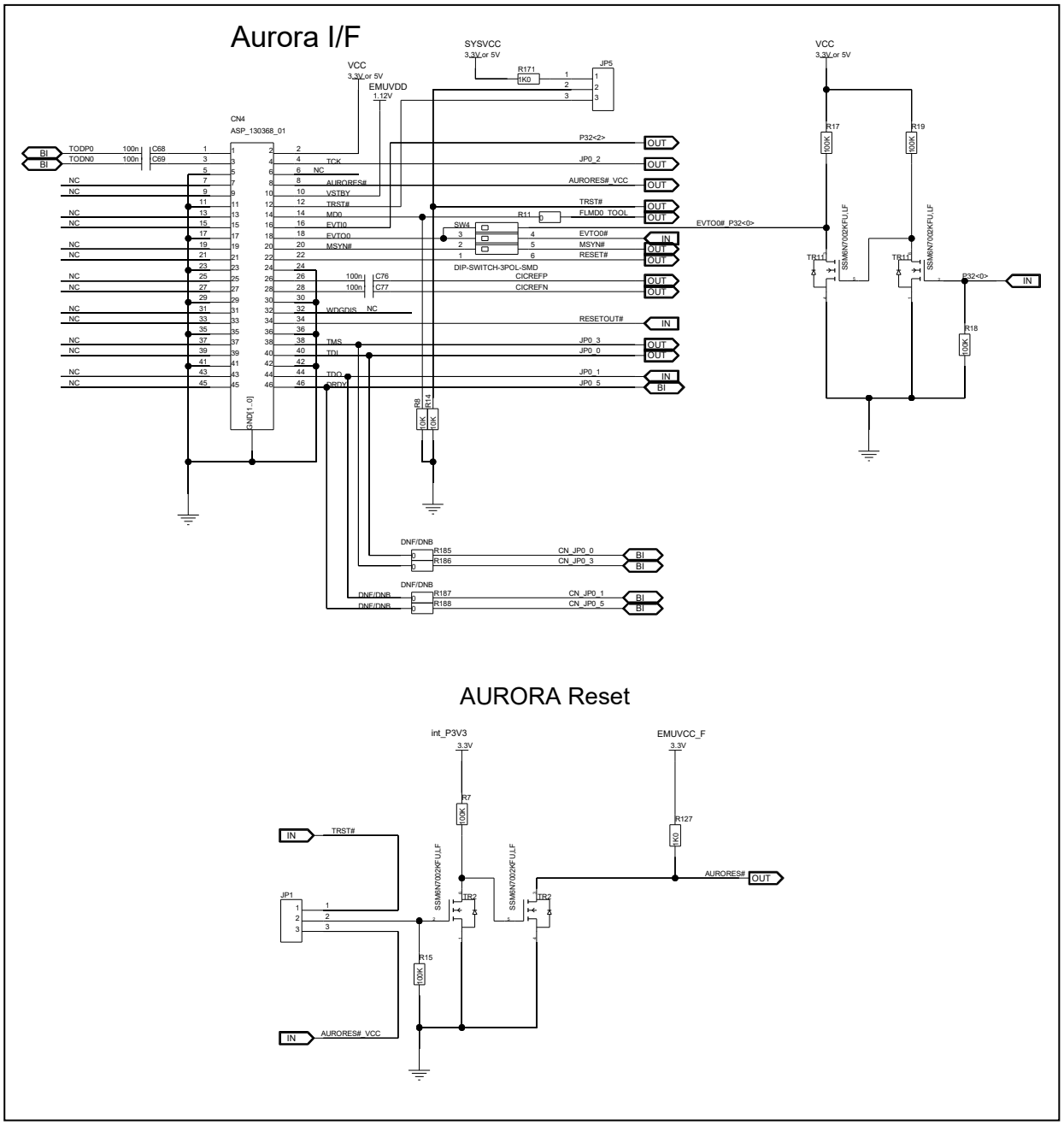


Figure 5.3 Debug connector CN4 and Aurora reset circuit on board version D018567_06_V03

Refer to *7.2 Debug Connector CN4* for details about the CN4 pin assignment.

Refer to *8.2 Operation using FCC Device or Mass Production Device* for details about the usage of SW4 and its related signals.

The Renesas standard emulator for RH850/U2B is the E2 emulator. This can be used as emulator for debugging or as flash programmer.

In order to connect the E2 emulator to Y-RH850-U2B-292PIN-PB-T1-V1 you have to use the adapter Y-RH850-DEBUG-ADAPTER-F14T46.

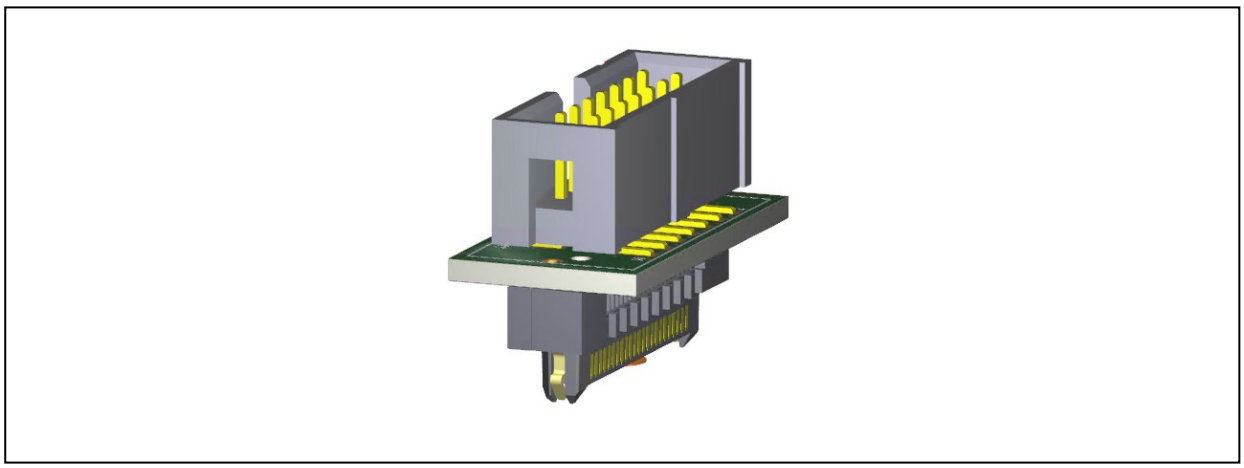


Figure 5.4 Outline view of debug adapter Y-RH850-DEBUG-ADAPTER-F14T46

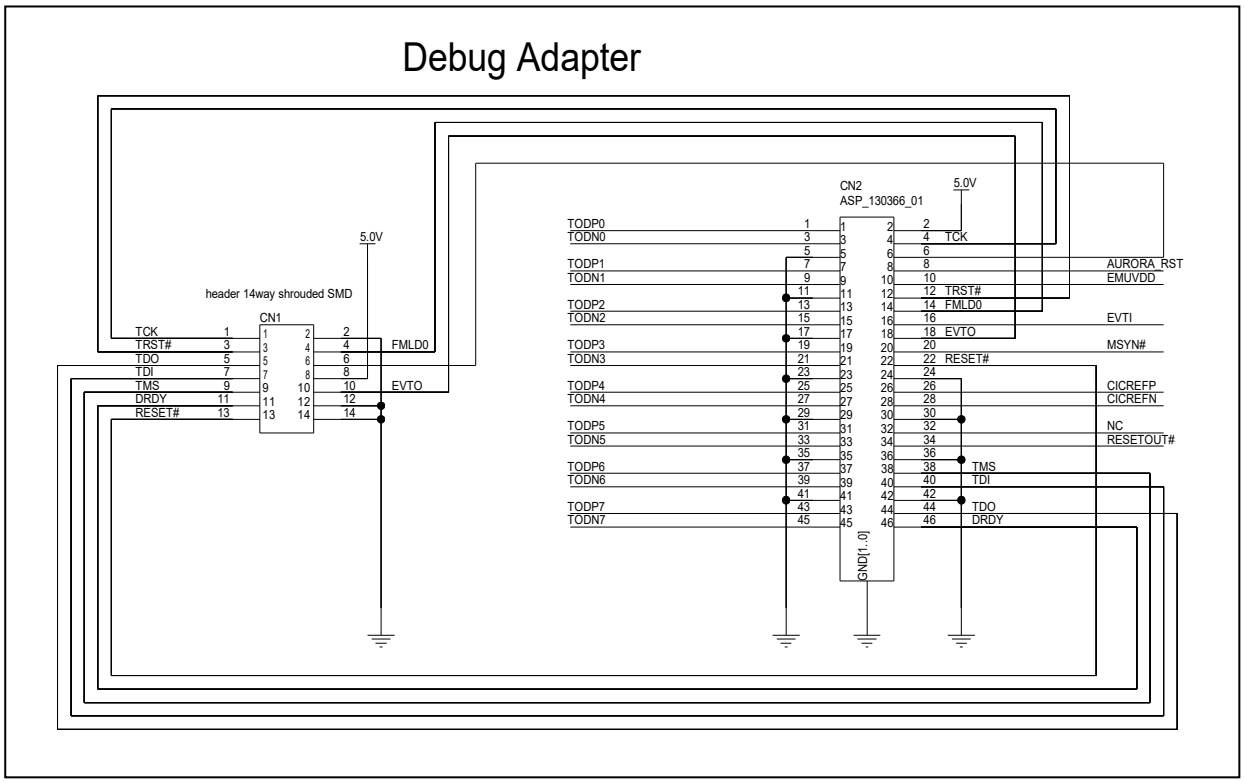


Figure 5.5 Circuit diagram of debug adapter Y-RH850-DEBUG-ADAPTER-F14T46

6. Other Circuitry

6.1 Operation Mode Selection

The piggyback board gives the possibility to configure the following jumpers for selection of the device operation mode.

Table 6.1 Device operation mode selection jumpers

Jumper	Function
JP46	FLMD0 pin level • JP46[SHORT]: FLMD0 = H level • JP46[OPEN]: FLMD0 – controlled by debugger or programming tool if a tool is connected via CN4 – GND, if no tool connected
JP48	FLMD1 pin level • JP48[SHORT]: FLMD1 = H level – Port function of port P6_13 can be used • JP48[OPEN]: FLMD1 = L level – JP48 must be open if Serial Programming Mode is used by a debugger or flash programming tool, that is connected to the board

CAUTION

Be careful in configuration of the operation mode related pins. The wrong configuration and operation of the device outside of its specification can cause irregular behavior of the device and long-term damage cannot be excluded. Be sure to check the corresponding Hardware User's Manual for details, which modes are specified for the used device.

Note

In most cases the 'normal operating mode' of the device will be used.
This mode is for execution of the user program. The on-chip debug functions also use this mode.

To select the 'normal operating mode' of the device, the FLMD0 pin must be pulled low. To do so, remove the jumper JP46.

All other jumpers related to the mode selection can be left open.

6.2 RESET Switch

The SW1 is used to issue a RESET to the device.

The SW1 toggle switch allows to activate the RESET in two different ways:

- SW1 in left '5-4(ON)' position: temporary reset
  Releasing the switch's lever returns the switch to its middle 'OFF' position and thus releases the reset.

- SW1 in right '5-6 ON' position: permanent reset
  For reset release the switch has to be moved back manually to its middle 'OFF' position.

The left and right switch position is defined from the side of the part number marking, which is highlighted with a red arrow in the figure below.

The lighted red LED13 indicates that SW1 is "on", i.e. in position '5-4 (ON)' or '5-6 ON'.

Note

LED13 does not light up when RESET is asserted by any other means than SW1.

Switch function	Viewed from part no. marking side		
			
NKK G19AP	ON	OFF	ON
Connecting terminals	5 – 4 momentary	None permanent	5 – 6 permanent

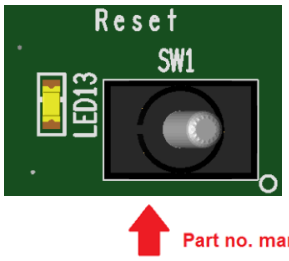


Figure 6.1 Operation of RESET switch

6.3 Signaling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins.

On the board version D018177_06_V01 the device pins P11_0 to P11_7 are connected to the odd pins of the pin header CN7.

On other board versions P11_0 to P11_3, P11_5 to P11_7 and P22_0 are connected to the odd pins of the pin header CN7.

The LEDs 2 to 9 are connected to the even CN7 pins.

Thus, the LEDs can be either connected to

- the device port pins P11_0 to P11_7 / P11_0 to P11_3, P11_5 to P11_7 and P22_0 by closing the connection on CN7 using a jumper, or
- any device pin by connecting the pin (from the connectors CN5, CN14 or CN15) directly with the even CN7 pins using a separate cable.

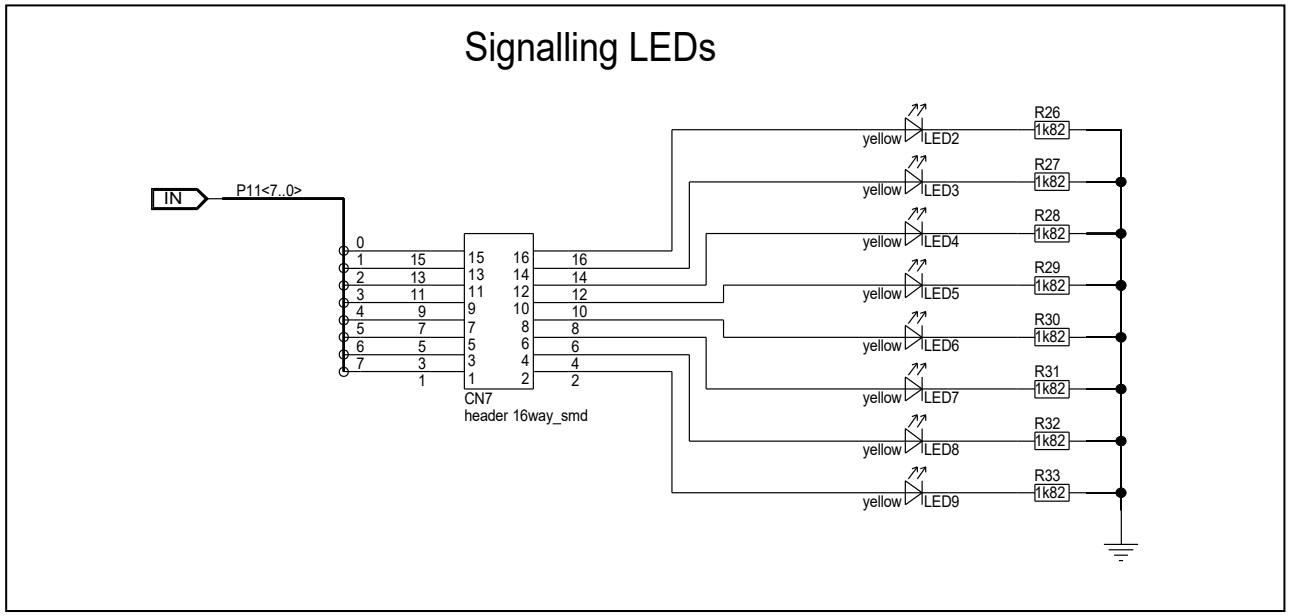


Figure 6.2 Circuit diagram for signalling LEDs on board version D018567_06_V01

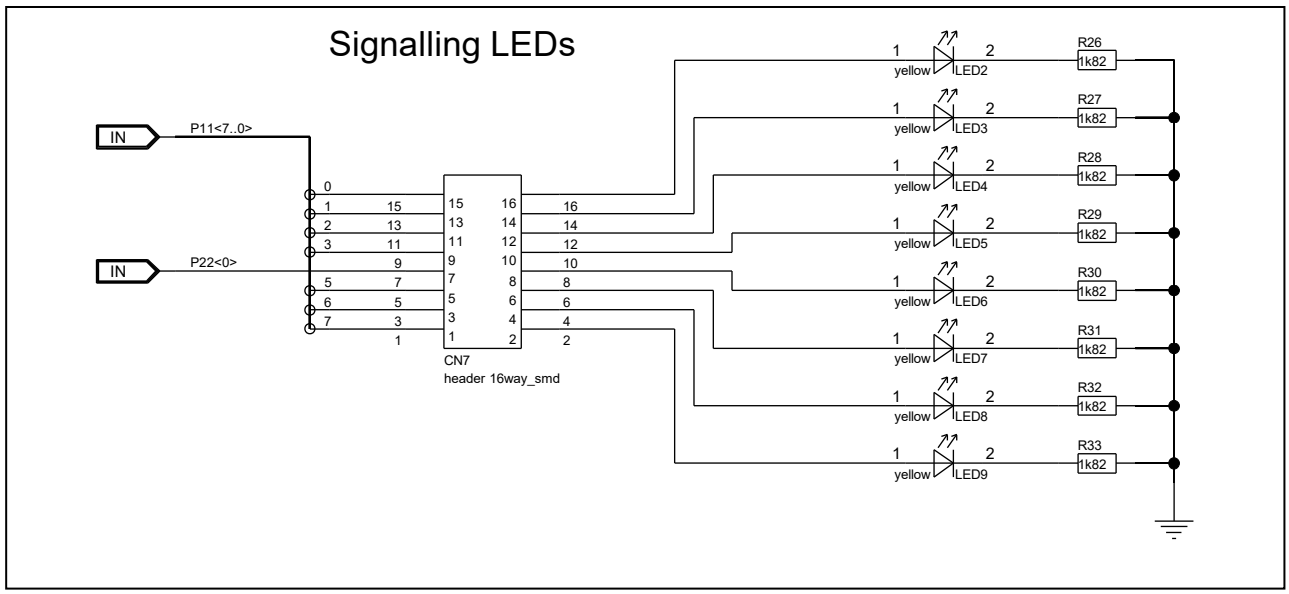


Figure 6.3 Circuit diagram for signalling LEDs on board versions other than D018567_06_V01

6.4 Pull-Up/Pull-Down Pin Header

The Pull-up/Pull-down pin header CN29 provides fixed voltage levels at its pins, that can be used to pull-up/pull-down a signal on the board or the device, respectively, by connecting a CN29 pin to the signal via a separate cable.

The CN29 pins have following pull-up or pull-down voltage levels:

- all odd numbered pins are connected to L level, i.e. to GND
- even numbered pins 2, 4, 6, 8 are connected to 3.3 V
- even numbered pins 10, 12, 14, 16 are connected to 5.0 V

Refer to *7.7 Pull-Up/*Pull-Down Pin Header CN29 for CN29 details.

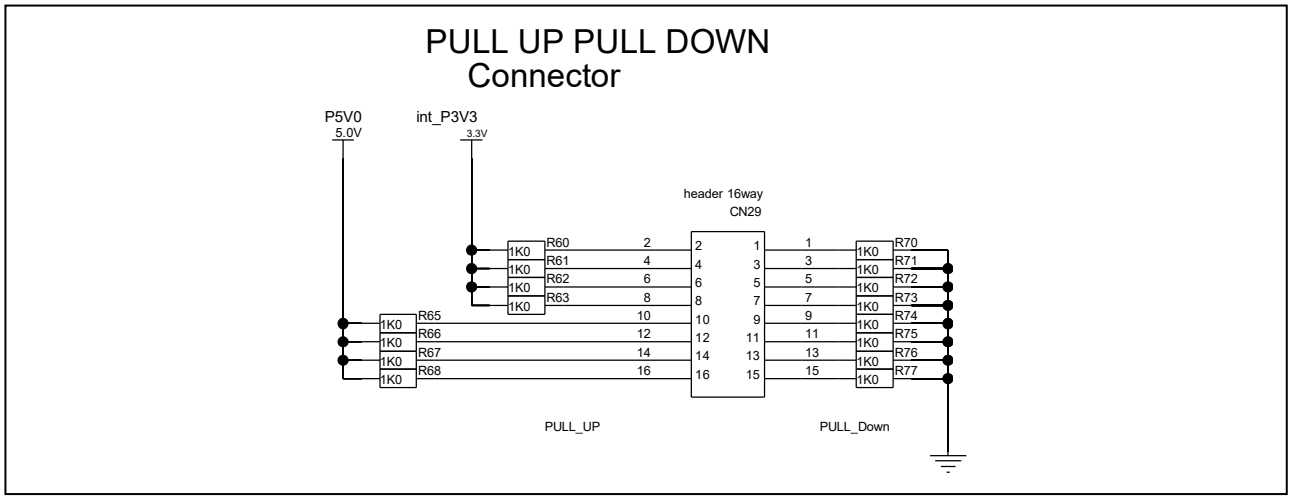


Figure 6.4 Circuit diagram for pull up / pull down signals

6.5 Renesas High-Speed Bus RHSB0

The piggyback board provides access to the high-speed bus interface RHSB0 on connector CN24.

On boards other than D018567_06_V01 connection of RHSB0 interface to CN24 has to be enabled using switch SW3-1.

The pin configuration on connector CN24 can be modified using the RHSB0_MUX signal from switch SW2-1.

Refer to *7.5 RHSB0 Connector CN24* for the possibility to configure the pin assignment on CN24.

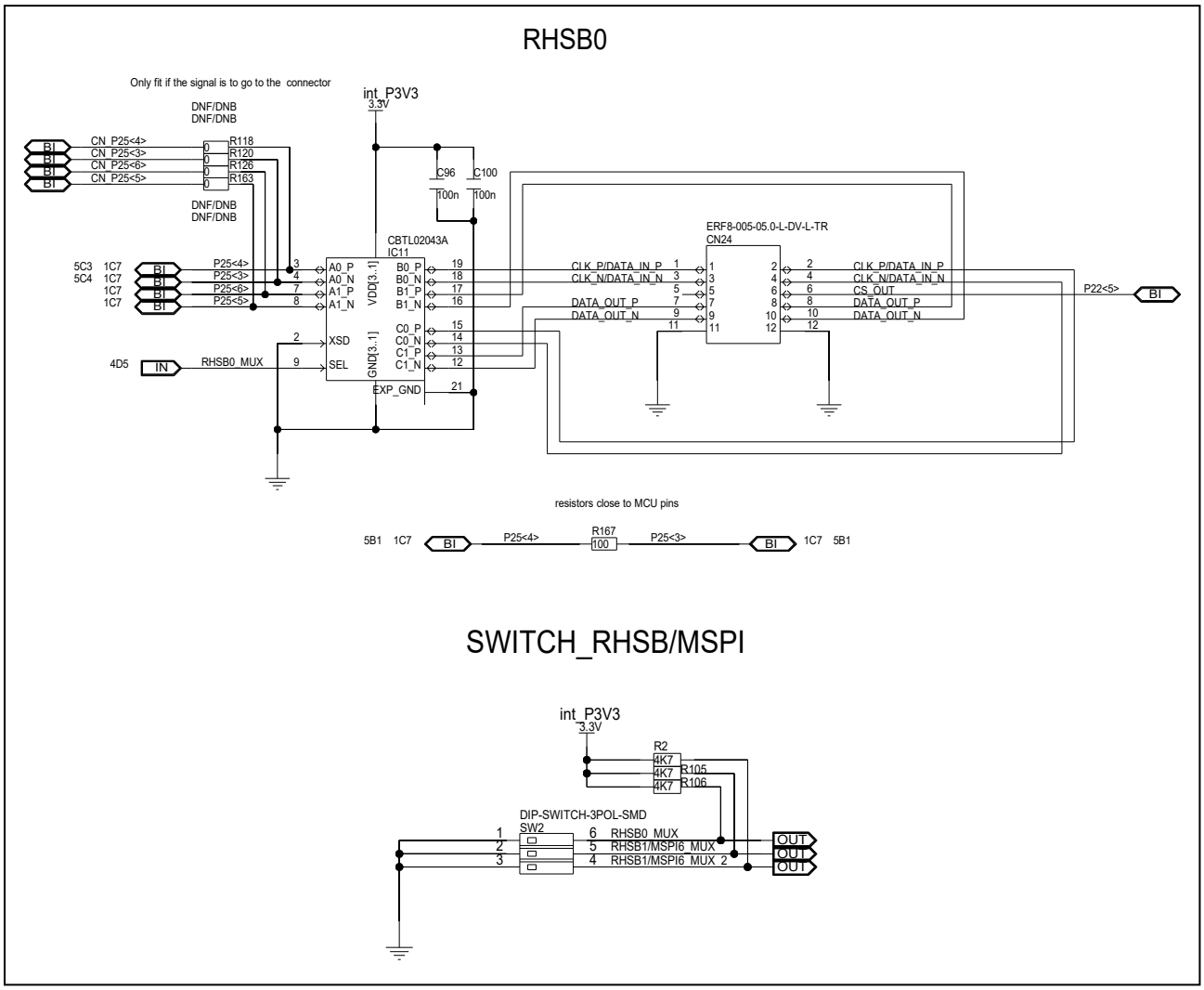


Figure 6.5 Circuit diagram for RHSB0 interface on board version D018567_06_V01

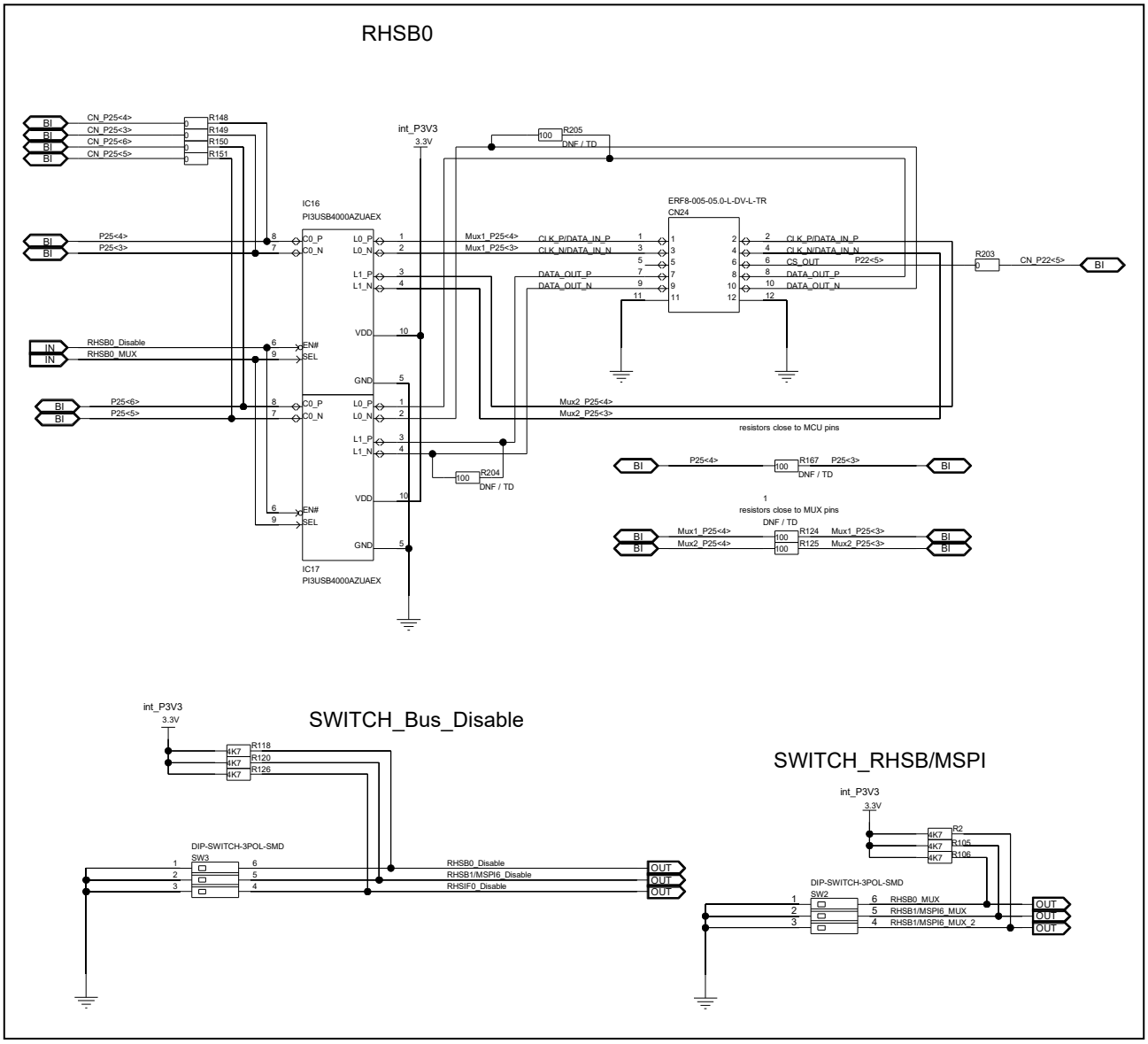


Figure 6.6 Circuit diagram for RHSB0 interface on board versions other than D018567_06_V01

CAUTION

The piggyback board has 100Ω termination resistors on P25_4 – P25_3.

The resistor on P25_4 – P25_3 and should be removed if the board is used as RHSB0 communicating to a MSPI6 slave.

Notes

1. The signals on the RHSB0 interface are connected to connectors CN3 and CN14. In order to minimize signal interference they can be disconnected by removing 0 Ω resistors R148-R151, R203.
2. Swapping the Rx/Tx signals allows board-to-board communication e.g. with another piggyback board via separate cables.

6.6 Renesas High-Speed Bus RHSB1 and Multichannel Serial Peripheral Interface MSPI6

The CN23 connector can be used to connect to the device's RHSB1 and MSPI6 interface.

On boards other than D018567_06_V01 the signal output of RHSB1 or MSPI6 to connector CN23 is enabled by switch SW3-2.

The pin configuration on connector CN23 can be modified using

- the RHSB1/MSPI6_MUX signal from switch SW2-2.
- the RHSB1/MSPI6_MUX_2 signal from switch SW2-3

Refer to *7.4 RHSB1/MSPI6 Connector CN23* for the CN23 pin assignment.

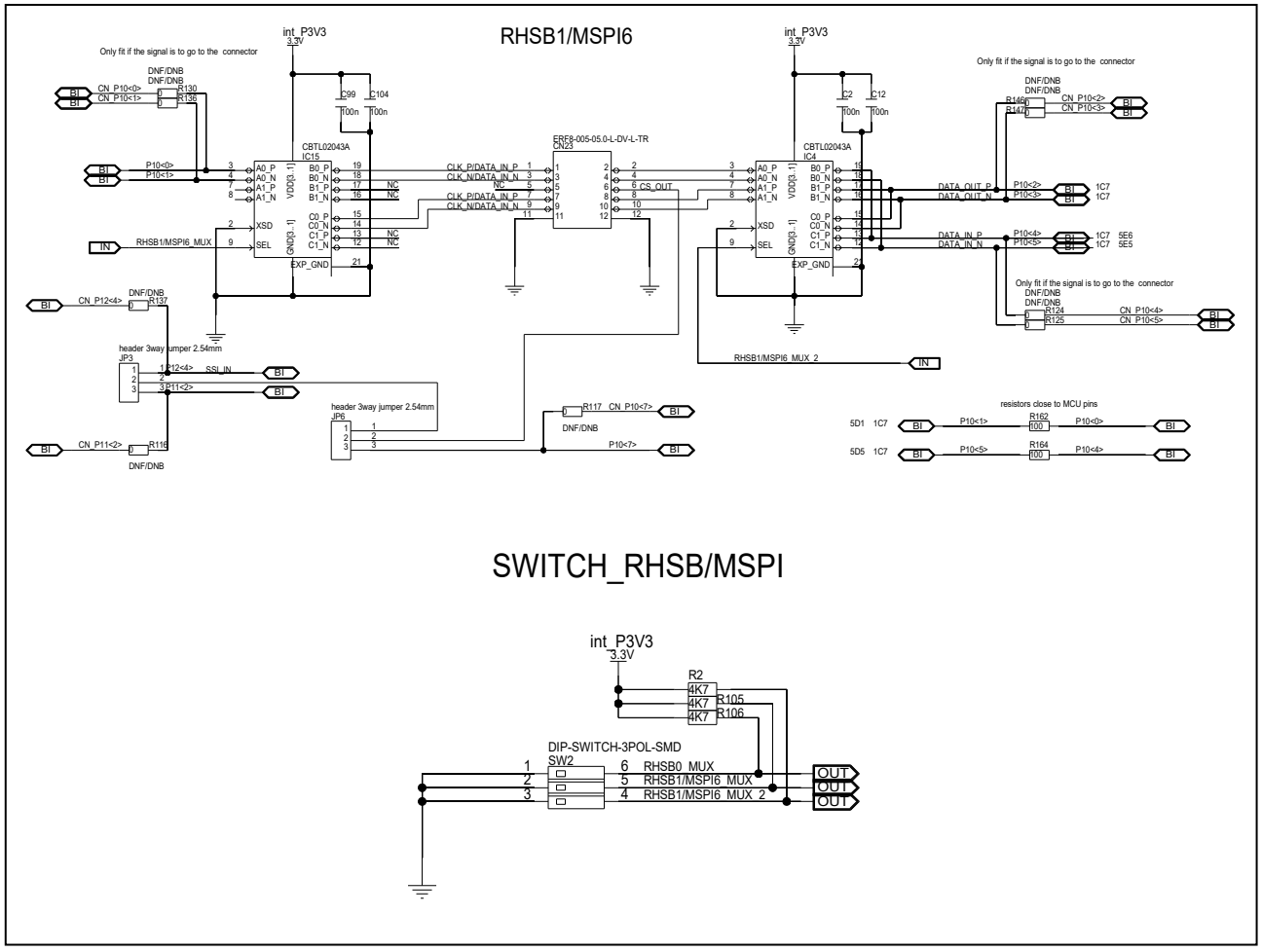


Figure 6.7 Circuit diagram for RHSB1/MSPI6 interface on board version D018567_06_V01

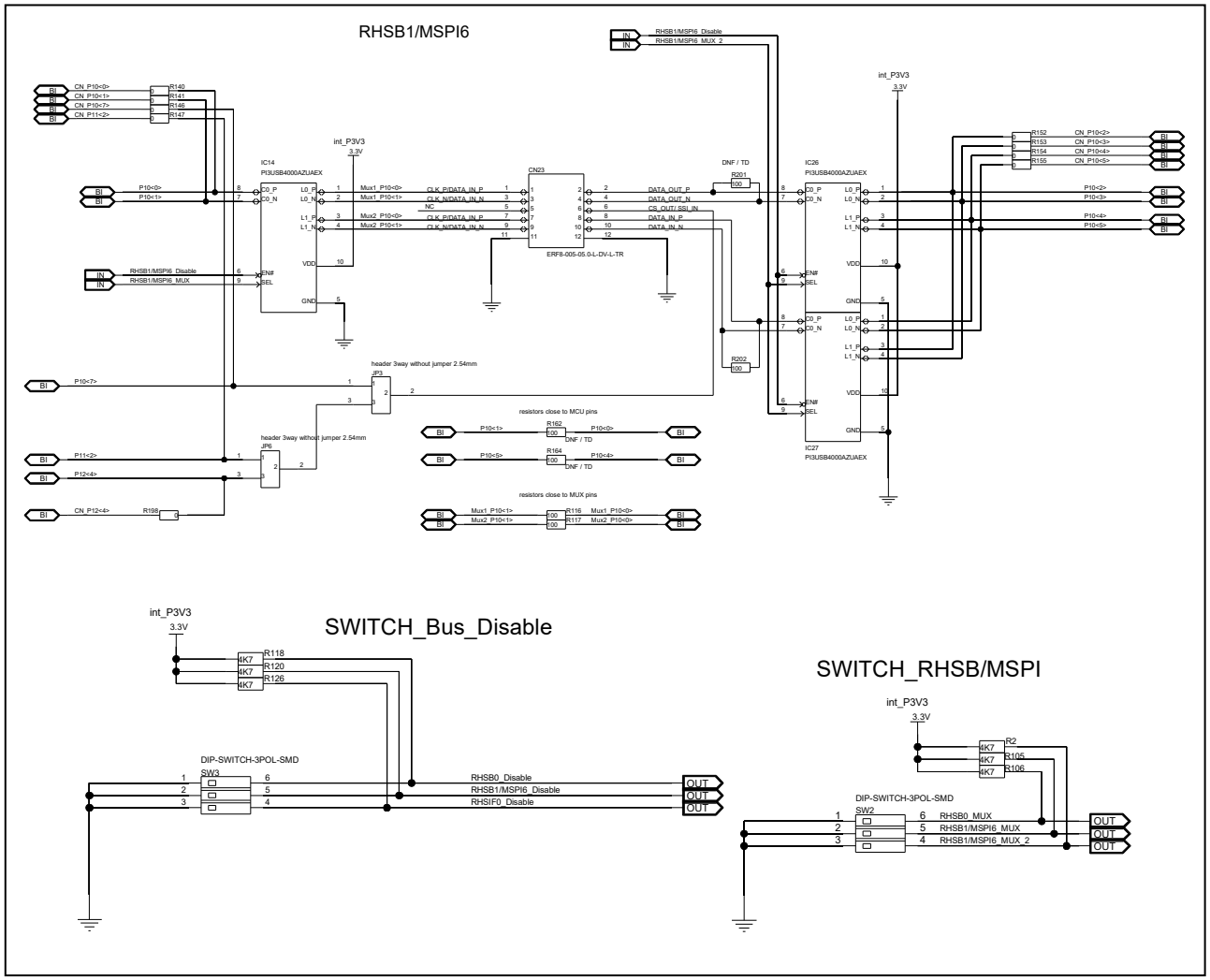


Figure 6.8 Circuit diagram for RHSB1/MSPI6 interface on board versions other than D018567_06_V01

CAUTION

The piggyback board has 100Ω termination resistors on P10_0 – P10_1 and P10_4 – P10_5.

The resistor on P10_0 – P10_1 should be removed if the board is used as MSPI6 master or as RHSB1 interface communicating to a MSPI6 slave.

Notes

1. The signals on the RHSB1/MSPI6 interface are connected to connectors CN1–CN3, CN14 and CN15. In order to minimize signal interference they can be disconnected by removing 0 Ω resistors R140, R141, R146, R147, R152-R155, R198.
2. Swapping the Rx/Tx signals allows board-to-board communication e.g. with another piggyback board via separate cables.

6.7 Renesas High-Speed Serial I/F RHSIF0

Connector CN27 provides access to the RHSIF0 interface.

CAUTION

RHSIF0 is only included in RH850/U2B10 devices. RH850/U2B6 does not have RHSIF0.

The signal output of RHSIF0 to connector CN27 is enabled by switch SW3-3 for board D018567_06_V02.

Rx and Tx signals available at CN27 can be swapped by setting the jumper JP4:

- JP4[1-2] = ON:
  - RXDP/RXDN at CN27 pins 1 and 3
  - TXDP/TXDN at CN27 pins 7 and 9
- JP4[1-2] = OFF:
  - RXDP/RXDN at CN27 pins 7 and 9
  - TXDP/TXDN at CN27 pins 1 and 3

Refer to *7.6 RHSIF0 Connector CN27* for the CN27 pin assignment.

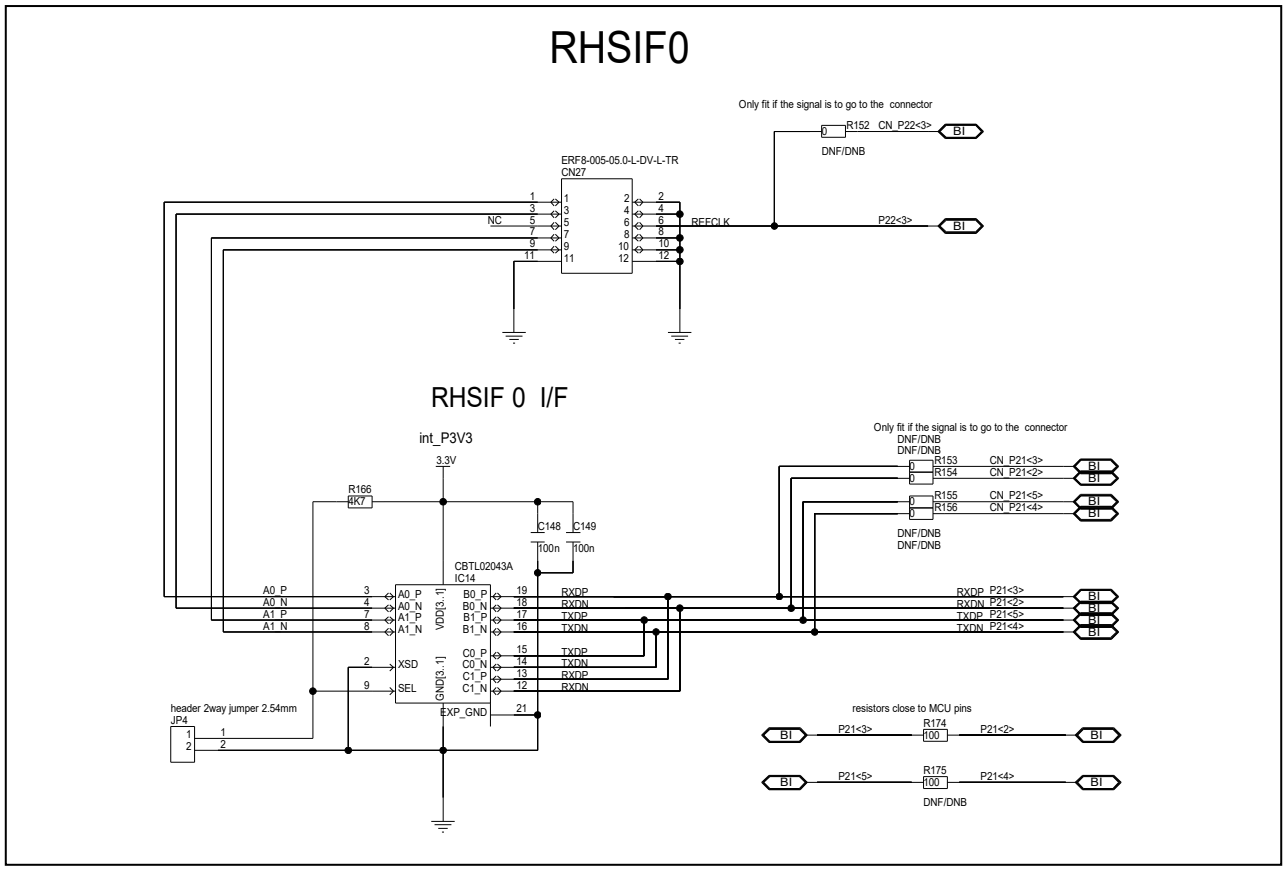


Figure 6.9 Circuit diagram for RHSIF0 interface on board version D018567_06_V01

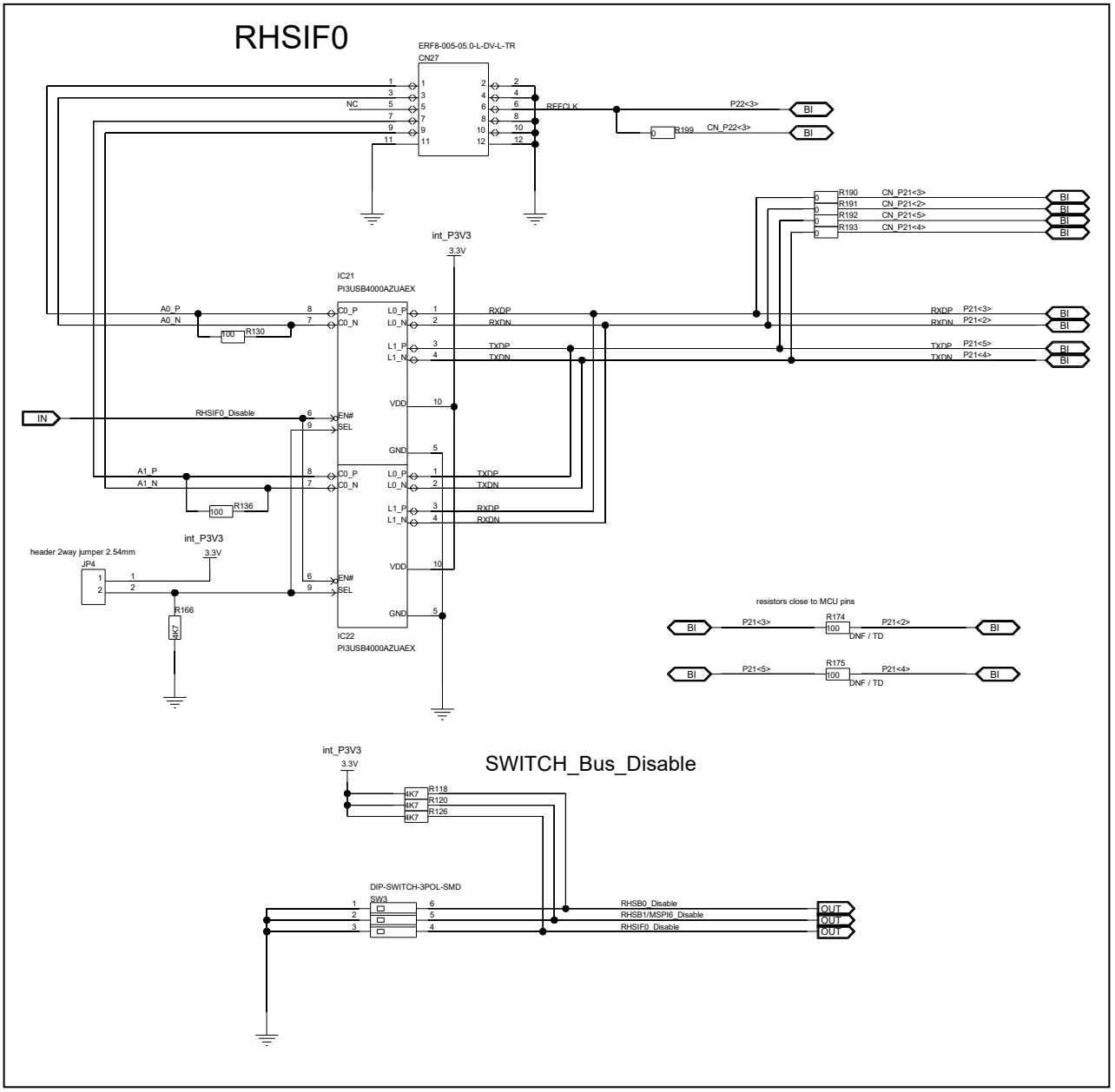


Figure 6.10 Circuit diagram for RHSIF0 interface on board versions other than D018567_06_V01

Notes

1. The signals on the RHSIF0 interface are connected to connectors CN3 and CN14. In order to minimize signal interference they can be disconnected by removing 0 Ω resistors R190-R193, R199.
2. Swapping the Rx/Tx signals allows board-to-board communication e.g. with another piggyback board via separate cables.

6.8 Low Pass Filter

The piggyback board includes a set of low pass filters in order to filter input signals to analog input ports.

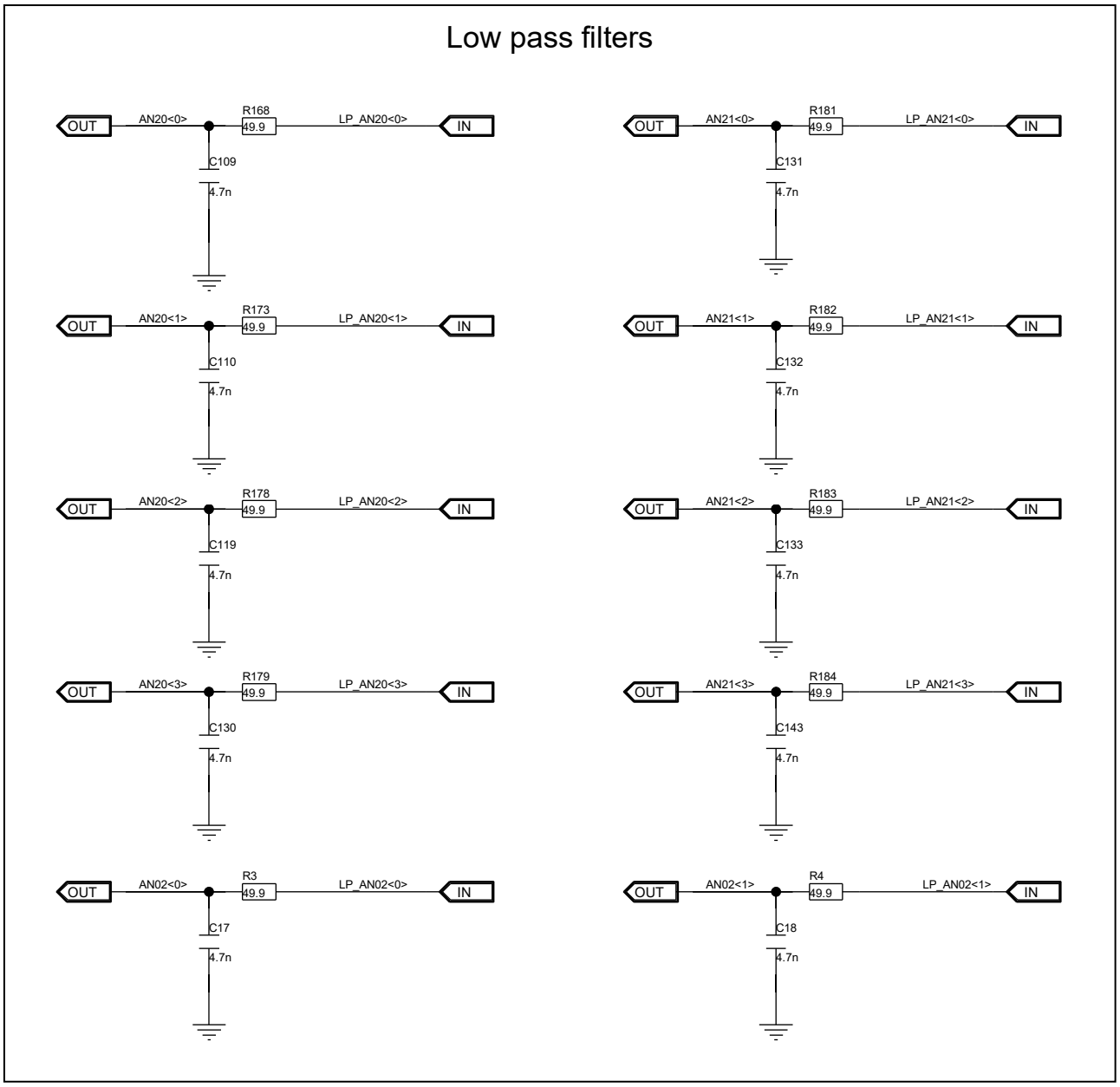


Figure 6.11 Circuit diagram for low pass filters

The analog input ports on RH850/U2B can be accessed through the device port connectors CN5 and CN15. Inputs including the low pass filter can be identify by the leading “LP_” in the pin name.

Please refer to *7.3.1 Device Ports Connector CN5* and *7.3.3 Device Ports Connector CN15* for details on the pin assignments.

7. Connectors

7.1 Connectors to the Main Board CN1 to CN3

Three connectors (CN1 to CN3) are available to connect the piggyback board to a main board.

The signals of each connector are summarized in the following tables.

Note

Regarding the function on the main board, please refer to the User's Manual of any supported main board.
Refer to *1.2 Supported Main Boards* for a list of supported main boards.

7.1.1 Main Board Connector CN1

Table 7.1 Main board connector CN1

Pin	Function	Device port	Pin	Function	Device port
1	VDDA	–	2	VDDA	–
3	VDDA	–	4	VDDA	–
5	RESET	RESET#	6	NMI	P25_2
7	WAKE	–	8	–	–
9	INT0	P23_2	10	INT1	P23_3
11	INT2	P23_4	12	INT3	P23_5
13	–	–	14	–	–
15	UART0TX	P12_6	16	UART1TX	P33_1
17	UART0RX	P12_5	18	UART1RX	P33_0
19	LIN0TX	P34_0	20	LIN1TX	P20_7
21	LIN0RX	P34_2	22	LIN1RX	P20_6
23	IIC0SCL	CN_P10_7 *	24	IIC1SCL	P00_6
25	IIC0SDA	P10_8	26	IIC1SDA	P00_7
27	CAN0TX	CN_P21_4 *	28	CAN1TX	P02_7
29	CAN0RX	CN_P21_5 *	30	CAN1RX	P02_10
31	SENT0RX	P00_0	32	SENT1RX	P00_4
33	SENT0SPCO	P00_1	34	SENT1SPCO	P00_5
35	PSI5SRX0	P02_10	36	PSI5RX0	P02_0
37	PSI5STX0	P02_8	38	PSI5TX0	P02_1
39	PSI5SCLK0	P02_6	40	–	–
41	FLX0TX	P12_1	42	FLX0EN	P12_0
43	FLX0RX	P12_7	44	FLXSTPWT	CN_P12_4 *
45	FLX1TX	P22_11	46	FLX1EN	P12_9

Table 7.1 Main board connector CN1 (cont'd)

Pin	Function	Device port
47	FLX1RX	P12_8
49	–	–
51	ETH0MDIO	CN_P10_4 *
53	ETH0RXD0	P11_3
55	ETH0RXD1	CN_P11_2 *
57	ETH0RXD2	CN_P10_3 *
59	ETH0RXD3	CN_P10_0 *
61	ETH0RXCLK	CN_P10_1 *
63	ETH0RXER	P11_6
65	ETH0CRSDV	–
67	ETH0RXDV	P11_7
69	ETH0RESET	P12_3 [1)] P10_8 [2)]
71	–	–
73	–	–
75	–	–
77	–	–
79	–	–
81	–	–
83	–	–
85	DIGIO_0	P11_0
87	DIGIO_2	CN_P11_2 *
89	DIGIO_4	P11_4 [1)] P22_0 [2)]
91	DIGIO_6	P11_6
93	DIGIO_8	P11_8
95	DIGIO_10	CN_P10_0 *
97	DIGIO_12	CN_P10_2 *
99	DIGIO_14	CN_P10_4 *
101	–	–
103	MUX0	P34_0
105	MUX2	P34_1
107	ADC0	LP_AN02_0
109	ADC2	AN02_2
111	ADC4	AN03_0
113	ADC6	AN03_2

Pin	Function	Device port
48	–	–
50	–	–
52	ETH0MDC	CN_P10_2 *
54	ETH0TXD0	P11_8
56	ETH0TXD1	P11_9
58	ETH0TXD2	P11_5
60	ETH0TXD3	P11_1
62	ETH0TXCLK	P11_4
64	ETH0TXER	P11_10
66	ETH0TXEN	P11_0
68	ETH0COL	–
70	ETH0LINK	CN_P10_7 *
72	–	–
74	–	–
76	–	–
78	–	–
80	–	–
82	–	–
84	–	–
86	DIGIO_1	P11_1
88	DIGIO_3	P11_3
90	DIGIO_5	P11_5
92	DIGIO_7	P11_7
94	DIGIO_9	P11_9
96	DIGIO_11	CN_P10_1 *
98	DIGIO_13	CN_P10_3 *
100	DIGIO_15	CN_P10_5 *
102	–	–
104	MUX1	P34_2
106	–	–
108	ADC1	LP_AN02_1
110	ADC3	AN02_3
112	ADC5	AN03_1
114	ADC7	AN03_3

Table 7.1 Main board connector CN1 (cont'd)

Pin	Function	Device port
115	VDDIOF	–
117	VDDB	–
119	VDDB	–
121	GND	–
123	GND	–
125	GND	–
127	GND	–

Pin	Function	Device port
116	VDDIOF	–
118	VDDB	–
120	VDDB	–
122	GND	–
124	GND	–
126	GND	–
128	GND	–

Note * By default, these CN_Pxx_x signals are connected to CN1. In order to minimize signal interference, they can be disconnected by removing each 0Ω resistor.

1) For board version D018567_06_V01

2) For board versions other than D018567_06_V01

7.1.2 Main Board Connector CN2

Table 7.2 Main board connector CN2

Pin	Function	Device port
1	CAN2TX	P02_1
3	CAN2RX	P02_4
5	CAN4TX	CN_P10_5 *
7	CAN4RX	P10_6
9	LIN2TX	P22_2
11	LIN2RX	CN_P22_3 *
13	LIN4TX	P12_6
15	LIN4RX	P12_5
17	–	–
19	–	–
21	–	–
23	–	–
25	–	–
27	–	–
29	–	–
31	–	–
33	–	–
35	–	–
37	–	–
39	–	–
41	–	–

Pin	Function	Device port
2	CAN3TX	P02_2
4	CAN3RX	P02_3
6	CAN5TX	P14_2
8	CAN5RX	P14_0
10	LIN3TX	P32_6
12	LIN3RX	P32_4
14	LIN5TX	P33_1
16	LIN5RX	P33_0
18	–	–
20	–	–
22	–	–
24	–	–
26	–	–
28	–	–
30	–	–
32	–	–
34	–	–
36	–	–
38	–	–
40	–	–
42	–	–

Table 7.2 Main board connector CN2 (cont'd)

Pin	Function	Device port
43	–	–
45	–	–
47	CAN6TX	P02_6
49	CAN6RX	P02_5
51	–	–
53	–	–
55	–	–
57	–	–
59	–	–
61	–	–
63	–	–
65	–	–
67	–	–
69	–	–
71	–	–
73	–	–
75	–	–
77	–	–
79	SFMA0CLK	P20_4
81	SFMA0IO0	P20_0
83	SFMA0IO2	P20_2
85	–	–
87	MMCA0CLK	P13_0
89	MMCA0DAT0	P13_1
91	MMCA0DAT2	P13_3
93	MMCA0DAT4	P14_0
95	MMCA0DAT6	P14_3
97	–	–
99	–	–
101	–	–
103	–	–
105	–	–
107	–	–
109	–	–
111	–	–

Pin	Function	Device port
44	–	–
46	–	–
48	CAN7TX	P20_5
50	CAN7RX	P20_4
52	–	–
54	–	–
56	–	–
58	–	–
60	–	–
62	–	–
64	–	–
66	–	–
68	–	–
70	–	–
72	–	–
74	LIN23TX	P32_1
76	LIN23RX	P32_0
78	–	–
80	SFMA0SSL	P20_5
82	SFMA0IO1	P20_1
84	SFMA0IO3	P20_3
86	–	–
88	MMCA0CMD	P14_5
90	MMCA0DAT1	P13_2
92	MMCA0DAT3	P14_1
94	MMCA0DAT5	P14_2
96	MMCA0DAT7	P14_4
98	–	–
100	–	–
102	–	–
104	–	–
106	–	–
108	–	–
110	–	–
112	–	–

Table 7.2 Main board connector CN2 (cont'd)

Pin	Function	Device port	Pin	Function	Device port
113	–	–	114	–	–
115	–	–	116	–	–
117	–	–	118	–	–
119	–	–	120	–	–
121	GND	–	122	GND	–
123	GND	–	124	GND	–
125	GND	–	126	GND	–
127	GND	–	128	GND	–

Note * By default, these CN_Pxx_x signals are connected to CN2. In order to minimize signal interference, they can be disconnected by removing each 0Ω resistor.

7.1.3 Main Board Connector CN3

Table 7.3 Main board connector CN3

Pin	Function	Device port	Pin	Function	Device port
1	CSI0CS0	P23_2	2	CSI0CLK	P23_7
3	CSI0CS1	P23_4	4	CSI0SI	P23_6
5	CSI0CS2	P23_3	6	CSI0SO	P23_5
7	CSI0CS3	P23_0	8	–	–
9	–	–	10	CSI1CS1	P33_4
11	–	–	12	–	–
13	PSI5SRX1	P33_2	14	PSI5RX1	P02_9
15	PSI5STX1	P33_0	16	PSI5TX1	P02_7
17	PSI5SCLK1	P33_1	18	–	–
19	–	–	20	–	–
21	CSI1CS2	P33_7	22	CSI1CS3	P33_8
23	–	–	24	CSI1CS0	P22_5 [1)] CN_P22_5 [2)] *
25	–	–	26	DIGIO_24	P22_6
27	–	–	28	CSI1SO	CN_P22_3 *
29	CSI1SCLK	P33_6	30	CSI1SI	P33_3
31	–	–	32	–	–
33	MOT0ADU (RFU)	AN00_0	34	AD0 (RFU)	AN10_0
35	MOT0ADV (RFU)	AN00_1	36	AD1 (RFU)	AN10_1
37	MOT0ADW (RFU)	AN00_2	38	AD2 (RFU)	AN10_2
39	MOT0RDCS1 (RFU)	AN24_3	40	RDCS1 (RFU)	AN27_2
41	MOT0RDCS3 (RFU)	AN24_2	42	RDCS3 (RFU)	AN27_1

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function	Device port
43	MOT0RDCS2 (RFU)	AN24_0
45	MOT0RDCS4 (RFU)	AN24_1
47	MOT0RDCCOM (RFU)	AN25_1
49	MOT0RDCRSO (RFU)	AN25_0
51	–	–
53	–	–
55	AD1_0	AN12_0
57	AD1_2	AN12_2
59	AD1_4	AN04_3
61	AD1_6	AN04_1
63	PWM0	P33_0
65	PWM2	P33_2
67	PWM4	P33_4
69	PWM6	P33_6
71	DIGIO16	P20_0
73	DIGIO18	P20_2
75	DIGIO20	P20_4
77	DIGIO22	P20_6
79	ENC0	CN_P10_5 *
81	–	–
83	MOT0U_P (RFU)	CN_P21_2 *
85	MOT0U_N (RFU)	CN_P21_3 *
87	MOT0V_P (RFU)	CN_P21_4 *
89	MOT0V_N (RFU)	CN_P21_5 *
91	MOT0W_P (RFU)	CN_P25_4 *
93	MOT0W_N (RFU)	CN_P25_3 *
95	–	–
97	–	–
99	–	–
101	GND	–
103	–	AN04_1
105	–	AN04_3
107	–	AN01_3
109	–	AN01_2
111	–	AN23_3

Pin	Function	Device port
44	RDCS2 (RFU)	AN26_0
46	RDCS4 (RFU)	AN26_2
48	RDCCOM (RFU)	AN27_3
50	RDCRSO (RFU)	AN26_3
52	–	–
54	–	–
56	AD1_1	AN12_1
58	AD1_3	AN12_3
60	AD1_5	AN04_2
62	AD1_7	AN04_0
64	PWM1	P33_1
66	PWM3	P33_3
68	PWM5	P33_5
70	PWM7	P33_7
72	DIGIO17	P20_1
74	DIGIO19	P20_3
76	DIGIO21	P20_5
78	DIGIO23	P20_7
80	ENC1	P10_6
82	–	–
84	O1 (RFU)	P13_0
86	O2 (RFU)	P13_1
88	O3 (RFU)	P13_2
90	O4 (RFU)	P13_3
92	O5 (RFU)	P14_5
94	O6 (RFU)	P14_4
96	–	–
98	–	–
100	–	–
102	–	–
104	–	–
106	–	–
108	–	–
110	–	–
112	–	–

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function	Device port
113	–	AN22_2
115	–	AN23_2
117	–	AN22_3
119	GND	–
121	GND	–
123	GND	–
125	GND	–
127	GND	–

Pin	Function	Device port
114	–	–
116	–	–
118	–	–
120	–	–
122	GND	–
124	GND	–
126	GND	–
128	GND	–

Note * By default, these CN_Pxx_x signals are connected to CN3. In order to minimize signal interference, they can be disconnected by removing each 0Ω resistor.

3) For board version D018567_06_V01

4) For board versions other than D018567_06_V01

(RFU) Ready for use with future main boards, actually main boards do not support this function.

7.2 Debug Connector CN4

Table 7.4 On-chip debug connector CN4

Pin	Function	Device port
1		TODP0
3		TODN0
5	GND	
7	–	–
9	–	–
11	GND	
13	–	–
15	–	–
17	GND	
19	–	–
21	–	–
23	GND	
25	–	–
27	–	–

Pin	Function	Device port
2	VCC	
4	TCK	JP0_2
6	–	–
8	AURORES#	AURORES#_VCC
10	VSTBY	EMUVDD
12	TRST#	Controlled by JP5 JP5 [1-2]: SYSVCC JP5 [2-3]: TRST#
14	MD0	FLMD0_TOOL
16	EVTI0	P32_2
18	EVTO0	Controlled by SW4 SW4-2 [ON]: EVTO0# SW4-3 [ON]: EVTO0#_P32_0
20	MSYN#	MSYN#
22		RESET#
24	GND	
26		CICREFP
28		CICREFN

Table 7.4 On-chip debug connector CN4

Pin	Function	Device port
29	GND	
31	–	–
33	–	–
35	GND	
37	–	–
39	–	–
41	GND	
43	–	–
45	–	–

Pin	Function	Device port
30	GND	
32	WDGDIS	–
34		RESETOUT#
36	GND	
38	TMS	JP0_3
40	TDI / LPDIO / FPDR	JP0_0
42	GND	
44	TDO / LPDO / FPDT	JP0_1
46	DRDY	JP0_5

7.3 Device Ports Connectors CN5, CN14 and CN15

The device port connectors enable easy connection to almost all ports of the device.

Note

The print on the pcb changed from D018567_06_V01 to the later versions.

The column “PCB Silk (only D018567_06_v01)” shows the numbering for board revision D018567_06_V01.

The column “Pin” shows the numbering for board revision OTHER than D018567_06_V01.

CAUTION

The pin headers are directly connected to the pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

7.3.1 Device Ports Connector CN5

Table 7.5 Device ports connector CN5

Pin	PCB Silk (only D018567_06_v01)	Device port	Pin	PCB Silk (only D018567_06_v01)	Device port
1	F1	P33_6	2	E1	P32_1
3	F2	P32_0	4	E2	P34_4
5	F3	P33_4	6	E3	P33_1
7	F4	P34_3	8	E4	P34_2
9	F5	P33_3	10	E5	P33_0
11	F6	P34_1	12	E6	P34_0
13	F7	AN11_2	14	E7	AN12_0
15	F8	AN12_3	16	E8	AN12_2
17	F9	AN12_1	18	E9	AN11_0
19	F10	AN11_3	20	E10	AN11_1
21	F11	AN10_3	22	E11	AN10_1
23	F12	AN10_2	24	E12	AN04_1
25	F13	AN04_3	26	E13	AN10_0
27	F14	AN04_2	28	E14	AN03_0
29	F15	AN04_0	30	E15	AN03_1
31	F16	AN02_3	32	E16	AN03_3
33	F17	AN02_2	34	E17	LP_AN02_1
35	F18	AN03_2	36	E18	AN01_3
37	F19	LP_AN02_0	38	E19	AN01_0
39	F20	AN01_2	40	E20	AN00_2

7.3.2 Device Ports Connector CN14

Table 7.6 Device ports connector CN14

Pin	PCB Silk (only D018567_06_v01)	Device port	Pin	PCB Silk (only D018567_06_v01)	Device port
1	D1	P33_2	2	C1	P33_8
3	D2	P33_5	4	C2	P32_3
5	D3	P33_7	6	C3	P32_2
7	D4	P32_4	8	C4	P23_1
9	D5	P32_5	10	C5	P23_5
11	D6	P32_6	12	C6	P23_6
13	D7	P23_3	14	C7	P23_0
15	D8	P23_7	16	C8	P23_4
17	D9	P23_2	18	C9	P22_1
19	D10	P22_0	20	C10	P25_2
21	D11	CN_P22_3 *1	22	C11	P22_2
23	D12	X1_C	24	C12	X2_C
25	D13	CN_P22_5 *1	26	C13	P22_4
27	D14	P22_6	28	C14	CN_P21_2 *1
29	D15	P22_7	30	C15	CN_P21_3 *1
31	D16	P22_8	32	C16	CN_P21_4 *1
33	D17	P22_9	34	C17	CN_P21_5 *1
35	D18	P22_10	36	C18	CN_P25_4 *1
37	D19	P22_11	38	C19	CN_P25_3 *1
39	D20	P22_12	40	C20	CN_P25_5 *1
41	D21	P22_13	42	C21	CN_P25_6 *1
43	D22	RESET#	44	C22	RESETOUT#
45	D23	TRST#	46	C23	FLMD0
47	D24	ERROROUT_M#	48	C24	VMONOUT#
49	D25	P20_0	50	C25	P20_1
51	D26	JP0_2	52	C26	CN_JP0_3 *2
53	D27	CN_JP0_0 *2	54	C27	CN_JP0_5 *2
55	D28	CN_JP0_1 *2	56	C28	P20_4
57	D29	P20_2	58	C29	P20_5
59	D30	P20_3	60	C30	P20_6
61	D31	P14_0	62	C31	P14_1
63	D32	P20_7	64	C32	P14_3
65	D33	P14_2	66	C33	P12_0
67	D34	P12_1	68	C34	P13_0

Table 7.6 Device ports connector CN14 (cont'd)

Pin	PCB Silk (only D018567_06_v01)	Device port	Pin	PCB Silk (only D018567_06_v01)	Device port
69	D35	P13_1	70	C35	P12_2
71	D36	P12_6	72	C36	P13_2
73	D37	P13_3	74	C37	P12_5
75	D38	P12_3	76	C38	P14_5
77	D39	P14_4	78	C39	RAMSVCL
79	D40	EVTO0#	80	C40	MSYN#

Note *1 By default, these CN_Pxx_x signals are connected to CN14. In order to minimize signal interference, they can be disconnected by removing each 0Ω resistor.

*2 By default these CN_Pxx_x signals are not connected to CN14 in order to minimize signal interference. If required they can be connected by adding each 0 Ω resistor.

7.3.3 Device Ports Connector CN15

Table 7.7 Device ports connector CN15

Pin	PCB Silk (only D018567_06_v01)	Device port	Pin	PCB Silk (only D018567_06_v01)	Device port
1	B1	AN00_3	2	A1	AN01_1
3	B2	AN00_1	4	A2	AN00_0
5	B3	AN23_1	6	A3	AN22_1
7	B4	LP_ AN20_0	8	A4	LP_ AN21_3
9	B5	LP_ AN20_1	10	A5	LP_ AN20_2
11	B6	LP_ AN20_3	12	A6	AN23_0
13	B7	AN22_2	14	A7	AN22_3
15	B8	LP_AN21_0	16	A8	LP_AN21_1
17	B9	AN23_3	18	A9	AN23_2
19	B10	AN22_0	20	A10	LP_AN21_2
21	B11	AN24_0	22	A11	AN24_2
23	B12	AN24_1	24	A12	AN24_3
25	B13	–	26	A13	AN25_2
27	B14	AN26_0	28	A14	AN26_1
29	B15	AN25_0	30	A15	AN25_1
31	B16	AN26_2	32	A16	AN26_3
33	B17	AN27_0	34	A17	AN25_3
35	B18	AN27_1	36	A18	AN27_3
37	B19	P02_9	38	A19	P02_10
39	B20	P02_7	40	A20	P02_8
41	B21	AN27_2	42	A21	P00_5

Table 7.7 Device ports connector CN15 (cont'd)

Pin	PCB Silk (only D018567_06_v01)	Device port
43	B22	P02_5
45	B23	P02_3
47	B24	P00_4
49	B25	P02_1
51	B26	P00_6
53	B27	P10_8
55	B28	CN_P10_7 *
57	B29	CN_P10_5 *
59	B30	CN_P10_3 *
61	B31	P00_0
63	B32	CN_P10_0 *
65	B33	P00_2
67	B34	P11_10
69	B35	CN_P11_2 *
71	B36	P11_9
73	B37	P12_9
75	B38	P11_8
77	B39	P12_7
79	B40	P11_0

Pin	PCB Silk (only D018567_06_v01)	Device port
44	A22	P02_6
46	A23	P02_4
48	A24	P00_3
50	A25	P02_2
52	A26	P02_0
54	A27	P00_7
56	A28	P10_6
58	A29	CN_P10_4 *
60	A30	CN_P10_2 *
62	A31	CN_P10_1 *
64	A32	P00_1
66	A33	P11_6
68	A34	P11_7
70	A35	P11_3
72	A36	P11_4
74	A37	P12_8
76	A38	P11_5
78	A39	CN_P12_4 *
80	A40	P11_1

Note * By default, these CN_Pxx_x signals are connected to CN15. In order to minimize signal interference, they can be disconnected by removing each 0Ω resistor.

7.4 RHSB1/MSPI6 Connector CN23

Table 7.8 RHSB1/MSPI6 connector CN23

Pin	SW2-2 = ON (RHSB1/MSPI6_MUX)		SW2-2 = OFF (RHSB1/MSPI6_MUX)	
	Device port	Function	Device port	Function
1	P10_0	CLK_P, DATA_IN_P (RHSB1MCSIP / RHSB1FCLP / MSPI6_SCKP)	–	–
3	P10_1	CLK_N, DATA_IN_N (RHSB1MCSIN / RHSB1FCLN / MSPI6_SCKN)	–	–
7	–	–	P10_0	CLK_P, DATA_IN_P (RHSB1MCSIP / RHSB1FCLP / MSPI6_SCKP)
9	–	–	P10_1	CLK_N, DATA_IN_N (RHSB1MCSIN / RHSB1FCLN / MSPI6_SCKN)

Pin	Device port	Function
5	-	-
6	On board D018567_06_V01 JP3 / JP6 / CN23.6pin 1-2 / 1-2 / P12_4 2-3 / 1-2 / P11_2 - / 2-3 / P10_7 On boards other than D018567_06_V01 JP3 / JP6 / CN23.6pin 1-2 / - / P10_7 2-3 / 1-2 / P11_2 2-3 / 2-3 / P12_4	RHSB1CSD0 MSPI6CSS0 MSPI6SSI
11	–	GND
12	–	GND

Pin	SW2-3 = ON (RHSB1/MSPI6_MUX_2)		SW2-3 = OFF (RHSB1/MSPI6_MUX_2)	
	Device port	Function	Device port	Function
2	P10_4	DATA_IN_P (MSPI6_SIP)	P10_2	DATA_OUT_P (RHSB1MCSOP / RHSB1SOP / MSPI6_SOP)
4	P10_5	DATA_IN_N (MSPI6_SIN)	P10_3	DATA_OUT_N (RHSB1MCSON / RHSB1SON / MSPI6_SON)

Table 7.8 RHSB1/MSPI6 connector CN23

8	P10_2	DATA_OUT_P (RHSB1MCSOP / RHSB1SOP / MSPI6_SOP)	P10_4	DATA_IN_P (MSPI6_SIP)
10	P10_3	DATA_OUT_N (RHSB1MCSON / RHSB1SON / MSPI6_SON)	P10_5	DATA_IN_N (MSPI6_SIN)

Note

The signals on the RHSB1/MSPI6 interface are connected to connectors CN1–CN3, CN14 and CN15. In order to minimize signal interference they can be disconnected by removing 0 Ω resistors R140, R141, R146, R147, R152-R155, R198.

7.5 RHSB0 Connector CN24

Table 7.9 RHSB0 connector CN24 cont'd

Pin	SW2_1 = ON (RHSB0_MUX)		SW2_1 = OFF (RHSB0_MUX)	
	Device port	Function	Device port	Function
1	P25_4	CLK_P/DATA_IN_P	–	–
2	–	–	P25_4	CLK_P/DATA_IN_P
3	P25_3	CLK_P/DATA_IN_N	–	–
4	–	–	P25_3	CLK_P/DATA_IN_N
5	–	–		–
6	P22_5	CS_OUT	P22_5	CS_OUT
7	–	–	P25_6	DATA_OUT_P
8	P25_6	DATA_OUT_P	–	–
9	–	–	P25_5	DATA_OUT_N
10	P25_5	DATA_OUT_N	–	–
11	–	GND		GND
12	–	GND		GND

Note

The signals on the RHSB0 interface are connected to connectors CN3 and CN14. In order to minimize signal interference they can be disconnected by removing 0 Ω resistors R148-R151, R203.

7.6 RHSIF0 Connector CN27

Table 7.10 RHSIF0 connector CN27

Pin	JP4 connected		JP4 open	
	Device port	Function	Device port	Function
1	P21_3	RXDP	P21_5	TXDP
2	–	GND	–	GND
3	P21_2	RXDN	P21_4	TXDN
4	–	GND	–	GND
5	–	–	–	–
6	P22_3	REFCLK	P22_3	REFCLK
7	P21_5	TXDP	P21_3	RXDP
8	–	GND	–	GND
9	P21_4	TXDN	P21_2	RXDN
10	–	GND	–	GND
11	–	GND	–	GND
12	–	GND	–	GND

Note

The signals on the RHSIF0 interface are connected to connectors CN3 and CN14. In order to minimize signal interference they can be disconnected by removing 0 Ω resistors R190-R193, R199.

7.7 Pull-Up/Pull-Down Pin Header CN29

Table 7.11 Pull-up and pull-down signal connector CN29

Pin	Function		Pin	Function
1	fixed L level		2	fixed H level, 3.3V
3			4	
5			6	
7			8	
9			10	fixed H level, 5.0V
11			12	
13			14	
15			16	

8. Jumper Configuration Examples

Several functions of the board can be configured via jumpers.
The board is shipped without any jumpers set.

For a complete list of jumpers refer to *2.1 Jumper Overview*.

For jumper settings related to the device operation mode, refer to *6.1 Operation Mode Selection*.

The following sections show some jumper settings, that allow to operate the piggyback board in different power supply configurations.

8.1 Stand-Alone Operation with Power Supply by Debugger

Basically the piggyback board can solely be powered by a connected debugger. Please make sure the debug tool is able to provide sufficient current on the power supply rails in order to operate the board in a useful manner.

Due to the limited current capability of Renesas' E2 Emulator, powering the board only via this debugger is not feasible.

In case of using another debug tool check its specification whether powering the piggyback board with the tool is possible.

8.2 Operation using FCC Device or Mass Production Device

It is possible to use a device with additional debug functions called FCC device or a mass production device with the piggyback board. There are some differences between FCC device or mass production (MP) device.

Jumper JP1

- When using a MP device do open jumper JP1.
- When using the FCC device the AURORES# signal has to be provided to the device. On the CN4 debug connector there are 2 signals that can be used for this signal.
  - If the AURORES# signal on CN4 is to be used for the FCC device put a jumper to JP1[2-3].
  - If the TRST# signal on CN4 is to be used for the FCC device put a jumper to JP1[1-2].

Switch SW4

- When using a MP device or an FCC device with a debug tool that does not support Aurora interface the signals EVTO0 and MSYN# are not needed on the processor. The switches SW4-1, SW4-2 and SW4-3 must be set OFF.
- When using an FCC device with a debug tool supporting Aurora interface the signals EVTO0 and MSYN# on connector CN4 must be connected to the device. The switches SW4-1 must be set to ON to select the MSYN# signal.
  For EVTO0 control set
  - SW4-2 to ON to select the device EVTO# signal or
  - SW4-3 to ON to select P32_0.

Power supply for debug interface

Some power supply jumpers only have to connected when the device is a FCC device. They are not needed when a MP device is used.

- CN10[37-38]: This jumper has to be set to provide 3.3V to EMUVCC_F
- CN10[46-47-48]: This jumper has to be set to provide supply voltage to J0VCC. The voltage level must be the same as for VCC.
  - CN10[46-47]: use 3.3V as J0VCC
  - CN10[47-48]: use 5.0V as J0VCC
- CN31 has a jumper to enable EMUVDD supply for an FCC device. This is not needed when a MP device is used.
  - CN31[10-11]: use onboard VDD as EMUVDD

Table 8.1 Power supply jumper settings for FCC devices and MP devices

Purpose	Jumper	RH850/U2B6 RH850/U2B10	RH850/U2B6-FCC RH850/U2B10-FCC
AURORES# Config	JP1	---	O
Port Select for CS_OUT on CN23	JP3, JP6	O	O
TX and RX Signal swap on RHSIF0 Interface	JP4	O	O
TRST# Signal Source Select	JP5	O	O
FLMD0 Config	JP46	---	---
FLMD1 Config	JP48	---	---
LED Output Config	CN7	O	O
A1VREFH Config	CN10[1-2-3]	O	O
A1VCC Config	CN10[4-5-6]	O	O
A0VREFH Config	CN10[7-8-9]	O	O

Table 8.1 Power supply jumper settings for FCC devices and MP devices (cont'd)

Purpose	Jumper	RH850/U2B6 RH850/U2B10	RH850/U2B6-FCC RH850/U2B10-FCC
A0VCC Config	CN10[10-11-12]	O	O
ADSVCC Config	CN10[13-14-15]	O	O
A2VCC Config	CN10[16-17-18]	O	O
A2VREFH Config	CN10[19-20-21]	O	O
AFCVCC Config	CN10[22-23-24]	O	O
E1VCC Config	CN10[31-32-33]	O	O
E0VCC Config	CN10[34-35-36]	O	O
EMUVCC_F Config	CN10[37-38-39]	---	CN10[37-38]
E2VCC Config	CN10[40-41-42]	O	O
SVRDRVCC Config	CN10[43-44-45]	O	O
J0VCC Config	CN10[46-47-48]	O, same as VCC Config	O
SYSVCC Config	CN10[49-50-51]	O	O
VCC Config	CN10[52-53-54]	O	O
VDDIOF Config	CN10[61-62-63]	O	O
ADVSREFH Config	CN10[64-65-66]	O	O
+5.0V power supply from main board	CN12	O	O
int_P3V3 Config	CN20	O	O
+3.3V power supply from main board	CN30	O	O
Ext_VDD Config	CN31[1-2-3]	O	O
VDD Config	CN31[4-5-6]	O	O
VDD Config	CN31[7-8-9]	O	O
EMUVDD Config	CN31[10-11-12]	---	CN31[10-11]
Debug port connection EVTO0 / MSYN#	SW4	OFF	O

--- : Jumper open

O : possible setting

The lines marked in yellow are for use with FCC devices only.

8.3 Configuration Examples

8.3.1 General Settings

All of the following board configurations are based on these conditions:

- Normal device operation mode (JP46[OPEN]: FLMD0 = L).
  - When using Serial Programming Mode by a debugger or programming tool, that is connected to the board, make sure to open jumper JP48 (JP48[OPEN]: FLMD1 = GND).
- All voltages for all functions are activated.
- Clock supply: assuming one of the resonators, coming with the board, are plugged into X1 socket.
- For connection to external power supplies the 'banana-type' connectors CN8 (GND), CN9 (+5.0 V) and CN21 (*3.3 V) are assembled on the board.
- If also the core supply voltage of 1.12 V will be supplied from an external power supply the connector CN11 (included in the package) has to be assembled on the pcb.

8.3.2 Jumper Indicators

The green jumper JP46 for FLMD0 must always be open for a ‘normal’ (user mode and debug) operation of the device.

The red jumpers are related to the power supply configuration.
Following jumper symbols are used:

- : Jumper must not be set.
- 1 2 3: Jumper must be set in the indicated position
- 1 2 3: Jumper can be set to position [1-2] or position [2-3]
- 1 2 3: Jumper with optional setting. The red setting [2-3] is the default setting. The blue setting [1-2] is the optional setting.

Note

The pin 1 of a jumper can be identified by

- a small circle near the jumper
- a square soldering pad.

8.3.3 Stand-Alone Operation with Single External Power Supply 3.3V: Minimum Configuration 1

This example enables to operate the board with only the 3.3 V external power supply. VDD is generated using the SVR of the U2B device. All I/O ports can only use 3.3 V.

Table 8.2 Power supply connectors for single power supply 3.3V

Connector	Name	Ext. Power Supply	Remarks
CN8	GND	Connected, GND	
CN9	5.0 V	Not connected	Jumpers in CN10 (VCC and VREF selection) are set to 3.3 V position CN10
CN11	1.12 V	Not connected	VDD from SVR_OUTPUT (CN31[6-5]) from on-chip Switching Voltage Regulator. Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage. SVR must be switched on and configured in the option bytes by a flash programming tool (e.g. RFP) beforehand .
CN21	3.3 V	Connected, +3.3 V	

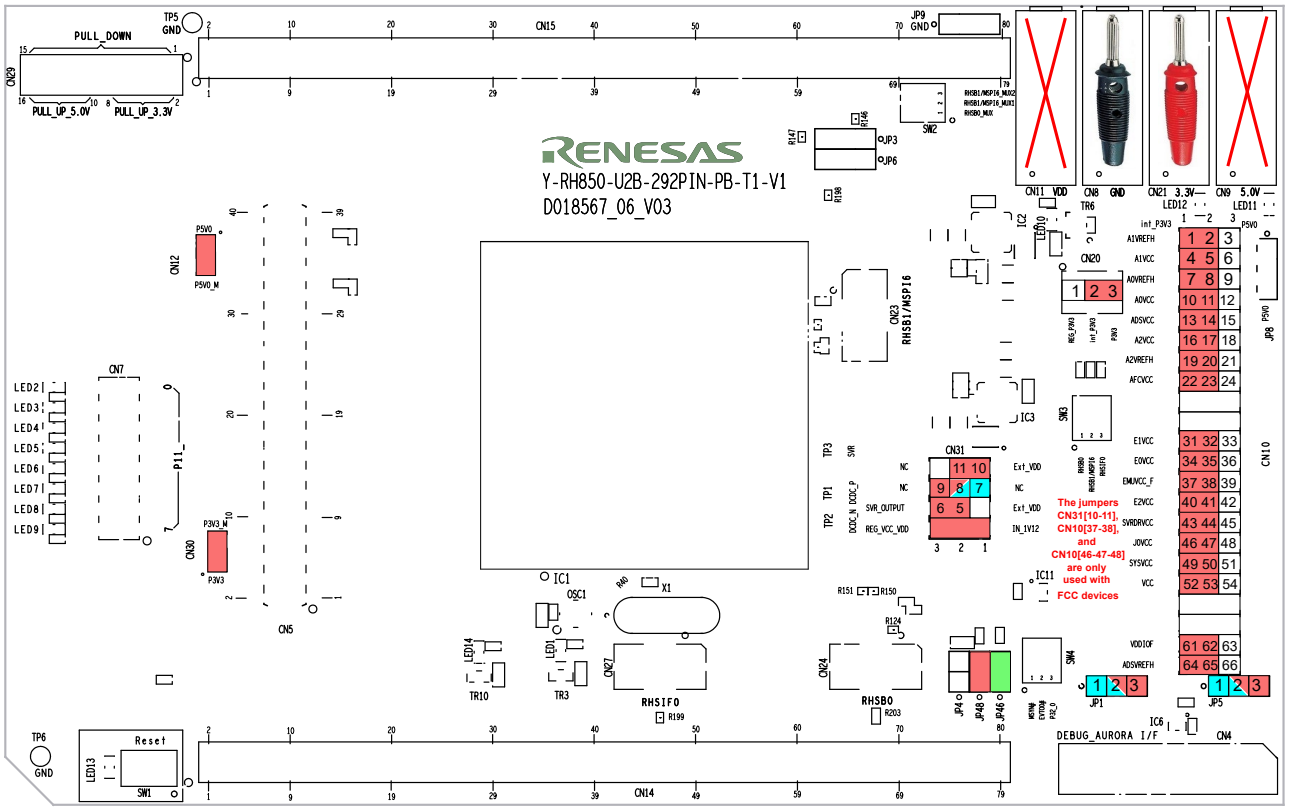


Figure 8.1 Stand-alone operation with 3.3V external power supply

8.3.4 Stand-Alone Operation with Single External Power Supply 5.0V: Minimum Configuration 2

This example enables to operate the board with only the 5.0 V external power supply. VDD is generated using the voltage generator on the piggyback board. All I/O ports can only use 5.0 V.

Table 8.3 Power supply connectors for single power supply 5.0V

Connector	Name	Ext. Power Supply	Remarks
CN8	GND	Connected, GND	
CN9	5.0 V	Connected, 5.0 V	
CN11	1.12 V	Not connected	VDD from onboard voltage regulator (CN31[5-4] and CN31[2-3]) Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
CN21	3.3 V	Not connected	Jumpers in CN10 (VCC and VREF selection) are set to 5.0 V position. 3.3V from onboard voltage regulator (CN20[1-2]) EMUVCC_F can only be connected to 3.3V (CN10[37-38]).

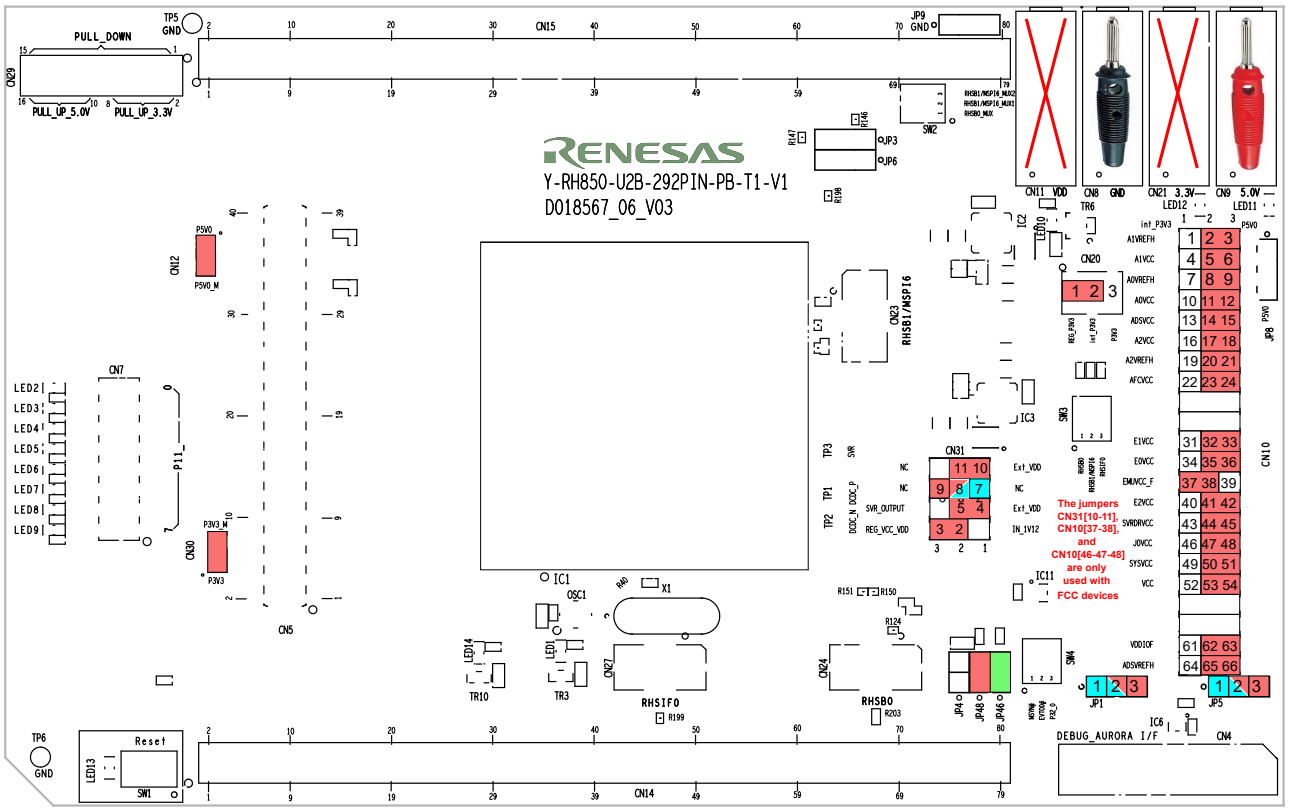


Figure 8.2 Stand-alone operation with 5.0V external power supply

8.3.5 Stand-Alone Operation with All External Power Supplies: Maximum Configuration

This example assumes all external power supplies are connected and used.

Table 8.4 Power supply connectors to use all external power supplies

Connector	Name	Ext. Power Supply	Remarks
CN8	GND	Connected, GND	
CN9	5.0 V	Connected, 5.0 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in CN10 Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in CN10.
CN11	1.12 V	Connected, 1.12 V	CN31[1-2] and CN31[4-5]: use IN_1v12 for VDD voltage Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
CN21	3.3 V	Connected, 3.3 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in CN10 CN20[2-3]: use p3V3 supply for 3.3 V. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in CN10.

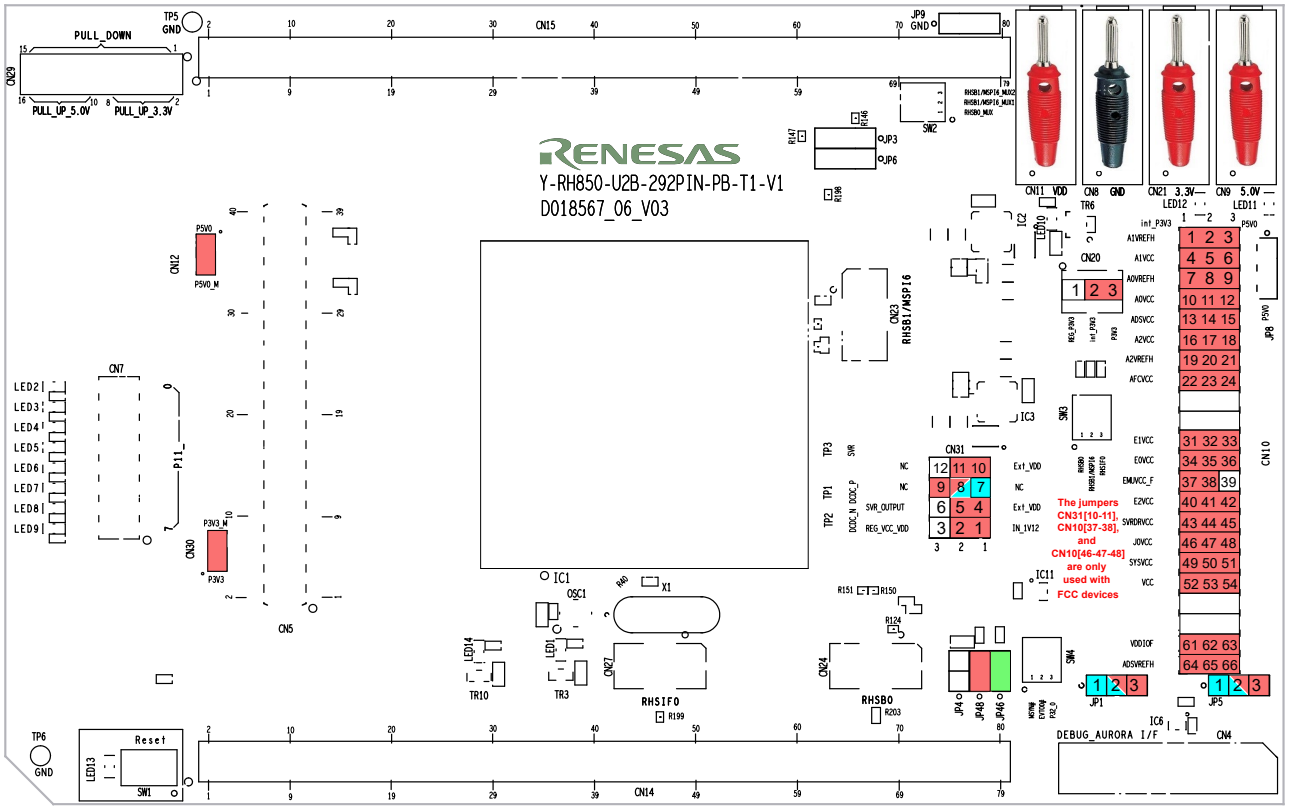


Figure 8.3 Stand-alone operation with all external power supplies

8.3.6 Operation on the Main Board: No External Supply

This example assumes the piggyback board is plugged onto a Main Board, which provides 3.3 V and 5.0 V.

The jumpers CN12 (P5V0) and CN30 (P3V3) must be set to connect the main board supply voltages P5V0_M and P3V3_M to the piggyback board power supply rails P5V0 and P3V3.

Do not supply the 5V (CN9) and 3.3V (CN21) voltage directly to the piggyback board

Table 8.5 Power supply connectors to use power supply from main board

Connector	Name	Ext. Power Supply	Remarks
CN8	GND	Not connected	
CN9	5.0 V	Not connected	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in CN10 Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in CN10.
CN11	1.12 V	Not connected	VDD supply: – CN31[2-3] and CN31[4-5]: use reg_vcc_VDD from on-board voltage regulator for supply of VDD voltage – CN31[6-5]: use SVR_OUTPUT from on-chip Switching Voltage Regulator Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage and possible settings of jumpers in CN31.
CN12	P5V0_M		Use jumper CN12[1-2] to connect the 5.0 V supply from the main board to the piggyback board
CN21	3.3 V	Not connected	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in CN10 3.3V from main board (CN20[2-3]) or from onboard voltage regulator (CN20[1-2]) Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in CN10.
CN30	P3V3_M		Use jumper CN30[1-2] to connect the 3.3 V supply from the main board to the piggyback board

Note

This configuration still allows to utilize an external IN_1v12 voltage (connected to CN8, CN11) as the source for VDD voltage. In this case set CN31[1-2] and CN31[4-5].

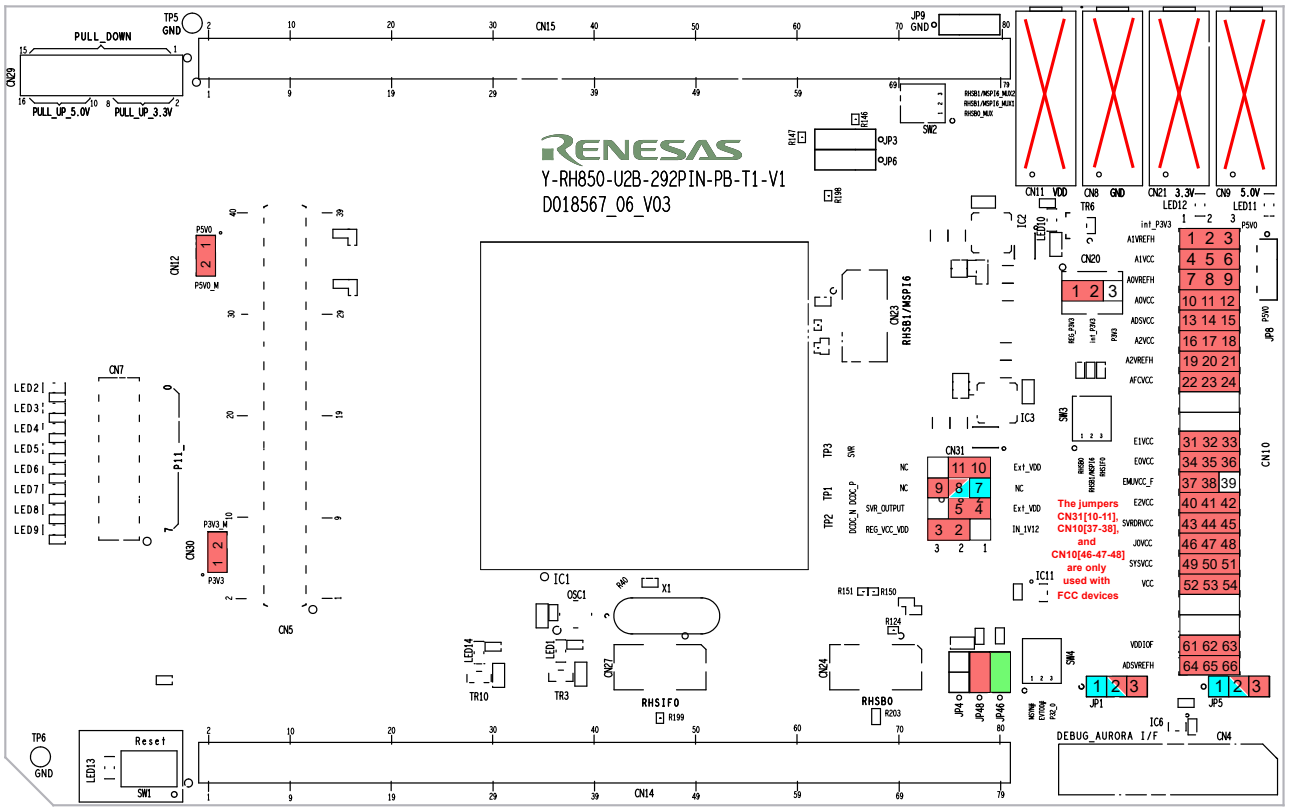


Figure 8.4 Main board operation without external power supply

9. Precautions

9.1 Power-Off Sequence

A dedicated sequence needs to be applied when the power supply to the board is turned off.

Please follow the below sequence:

1. At first turn the RESET switch SW1 into '5-6 ON' position, so that RESET is permanently asserted.
   Alternatively keep SW1 manually in' 5-4 (ON)' position.
2. Turn off the board power supply.
3. After the power supply has shut down, release RESET by returning SW1 into the 'OFF' position.

For details how to apply a RESET, please refer to *6.2 RESET Switch.*

9.2 Factory Rework on Board Marked D018567_06_V02

The PCB layout of Y-RH850-U2B-292PIN-PB-T1-V1 (board marked D018567_06_V02) have one fault:

- The ETH0TXCLK signal that is output by the U2B device on P11_4 is connected to CN1.62, as well as to CN1.89 (DIGIO4) and CN7.7 (LED6).
  As a result the signal quality is degraded and a reliable communication to the Ethernet circuitry on the main board is not possible.

To solve this fault, P11_4 is exchanged to the port P22_0 at CN1.89 (DIGIO_4) and CN7.7 (LED6).

The required changes to the D018177_06_V02 board version are applied during production and can be seen in the pictures below.

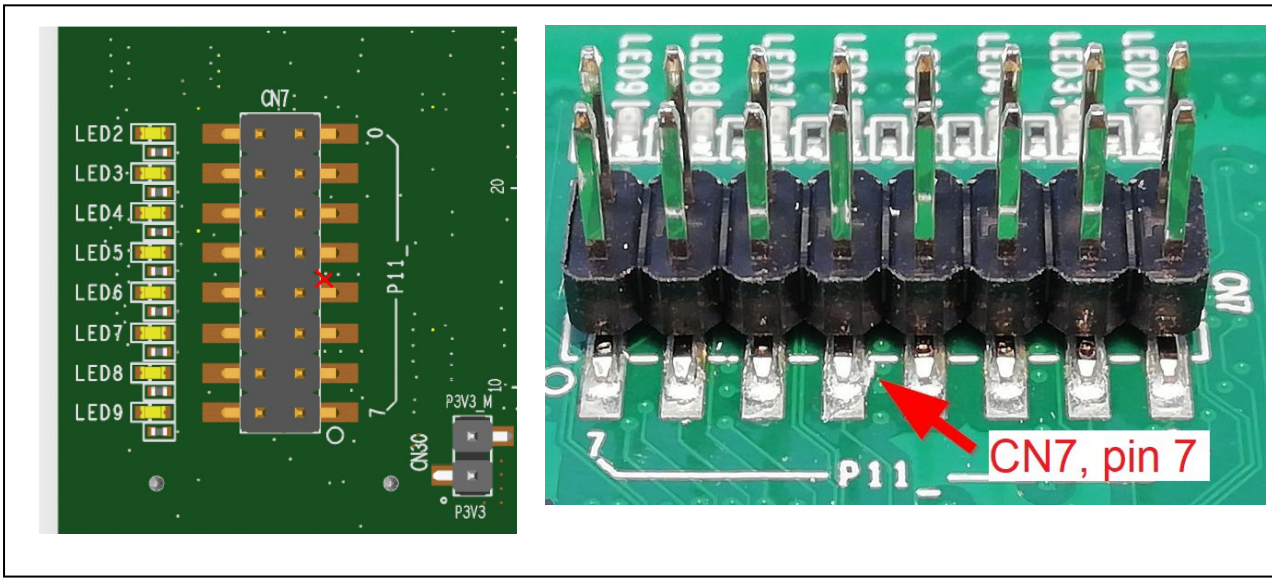


Figure 9.1 Top side rework: Cut conductive path close to CN7 pin 7

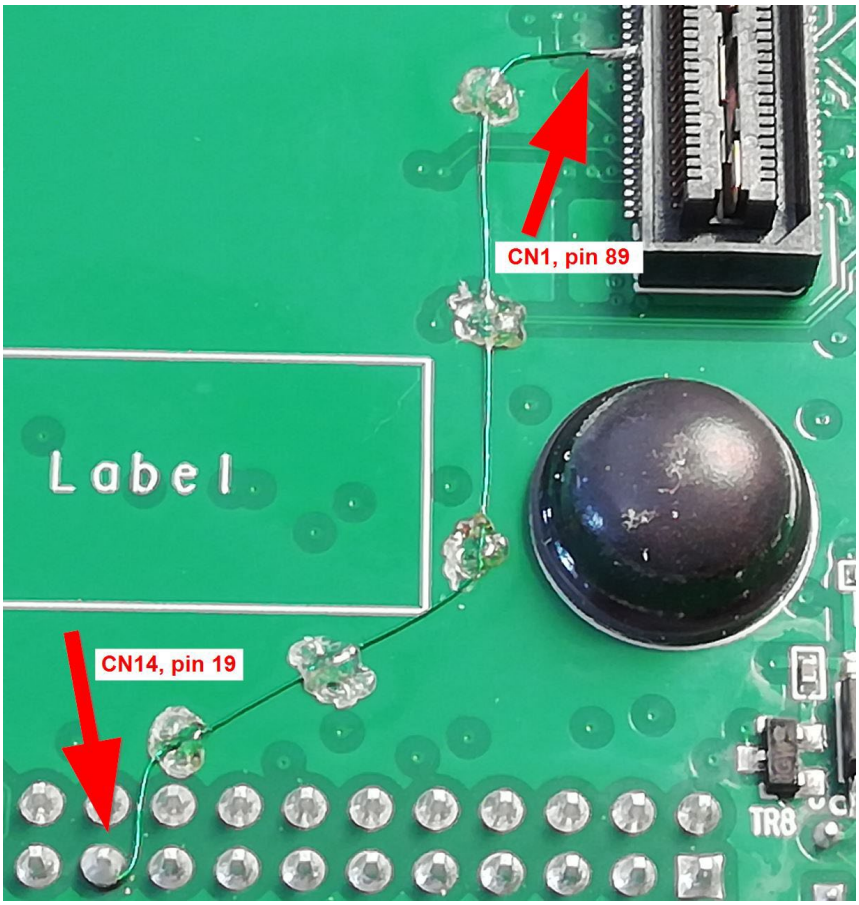


Figure 9.2 Bottom side rework: Add solder wire from connector CN14 pin 19 to connector CN1 pin 89

9.3 Power On Piggyback Board Without RH850 Microcontroller installed

The piggyback board Y-RH850-U2B-292PIN-PB-T1-V1 is not designed to be powered on when the RH850 microcontroller is not installed in socket IC1.

If the microcontroller is not installed the SVR power supply circuit does not have the control signals SVRNGATE and SVRPGATE and may be damaged.

If for some reason the board has to be powered on without a microcontroller mounted in socket IC1 please make sure the jumper CN10[43-44-45] (SVRDRVCC) is open. In this case no power is supplied to the SVR control circuit, and it will not be damaged.

If the piggyback board is being used with the microcontroller installed please make sure the ports SVRNGATE and SVRPGATE are set to “Fixed” (output) in bit SVRENDCDCHZ in option byte 25.

10. Mechanical Dimensions

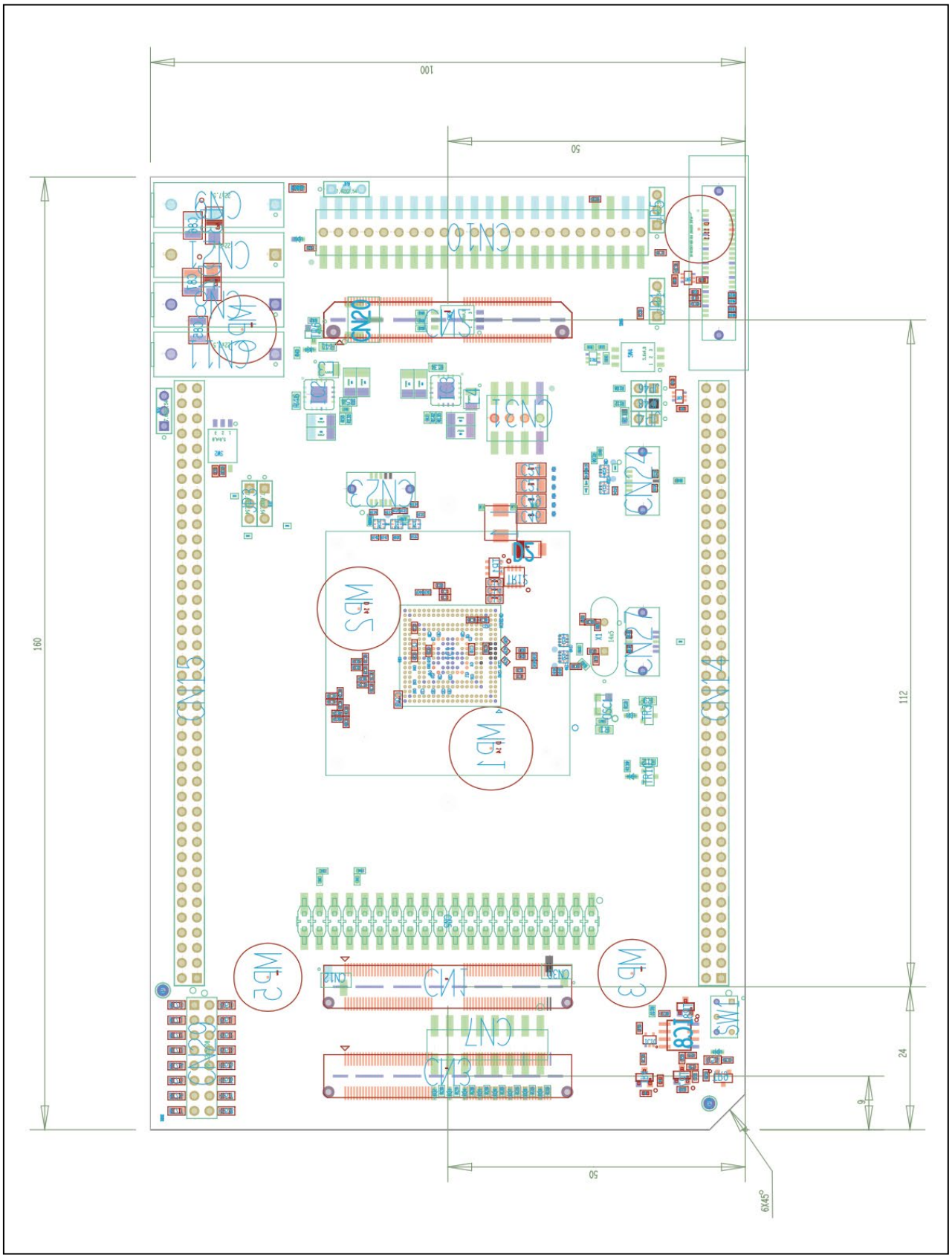


Figure 10.1 Mechanical dimensions

11. Schematics

CAUTION

The schematics shown in this document are not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.

The following components described in the schematics are not provided with the board upon delivery:

- Capacitors: C97, C98
- Resistors: R40, R57, R64, R107, R116 – R118, R120, R124 – R126, R130, R136 – R137, R146 – R147, R152 – R156, R163, R175, R185 – R188
  (Board version D018567_06_V01).
- Resistors: R40, R57, R64, R107, R185 – R188
  (Board versions other than D018567_06_V01)

The above components are indicated with "DNF/DNB" in the schematics.

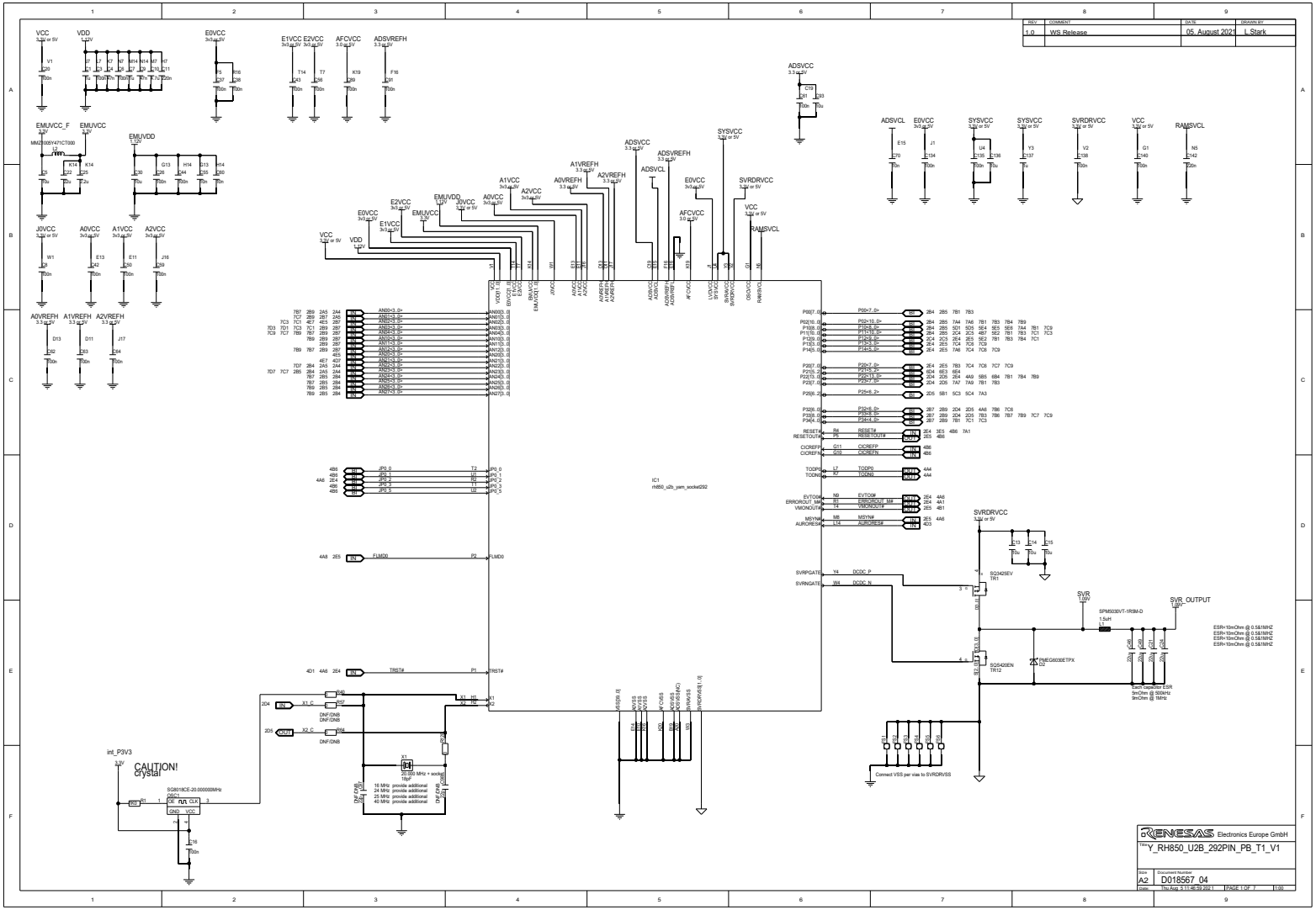
The following components described in the schematics are provided with but not mounted on the board upon delivery:

- 1 Hirschmann 4 mm power lab sockets, red for CN11
- Four resonators HC49 (16/24/25/40 MHz)
- 38 jumpers, 2.54 mm, black (Board version D018567_06_V01)
  39 jumpers, 2.54 mm, black (Board versions other than D018567_06_V01)
- 100 Ohm resistors for
  - R124, R162, R164, R167, R174, R175, R201, R204, R205
    (Board versions other than D018567_06_V01)

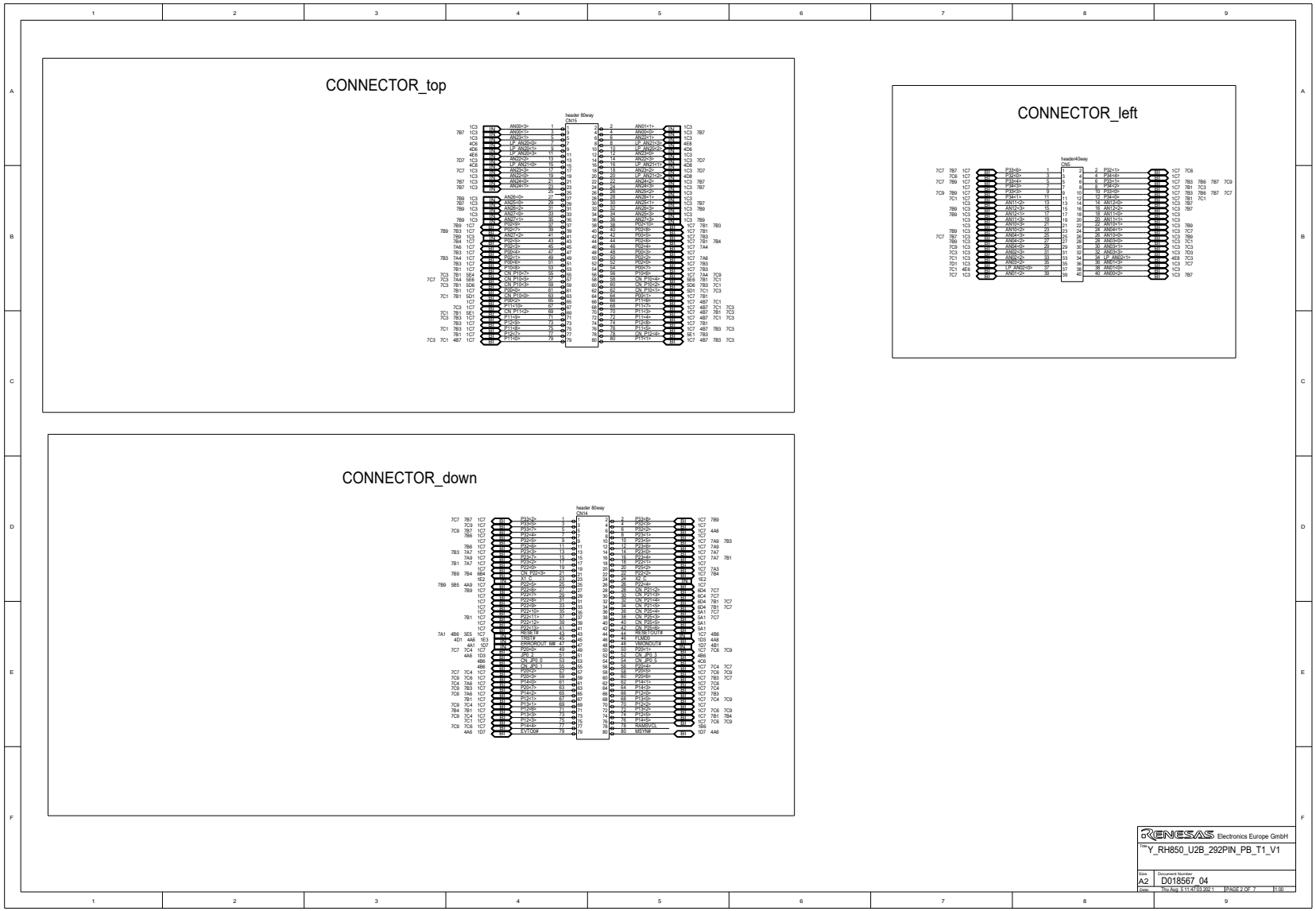
  The above components are indicated with "DNF / TD" in the schematics.

11.1 Board Version D018567_06_V01

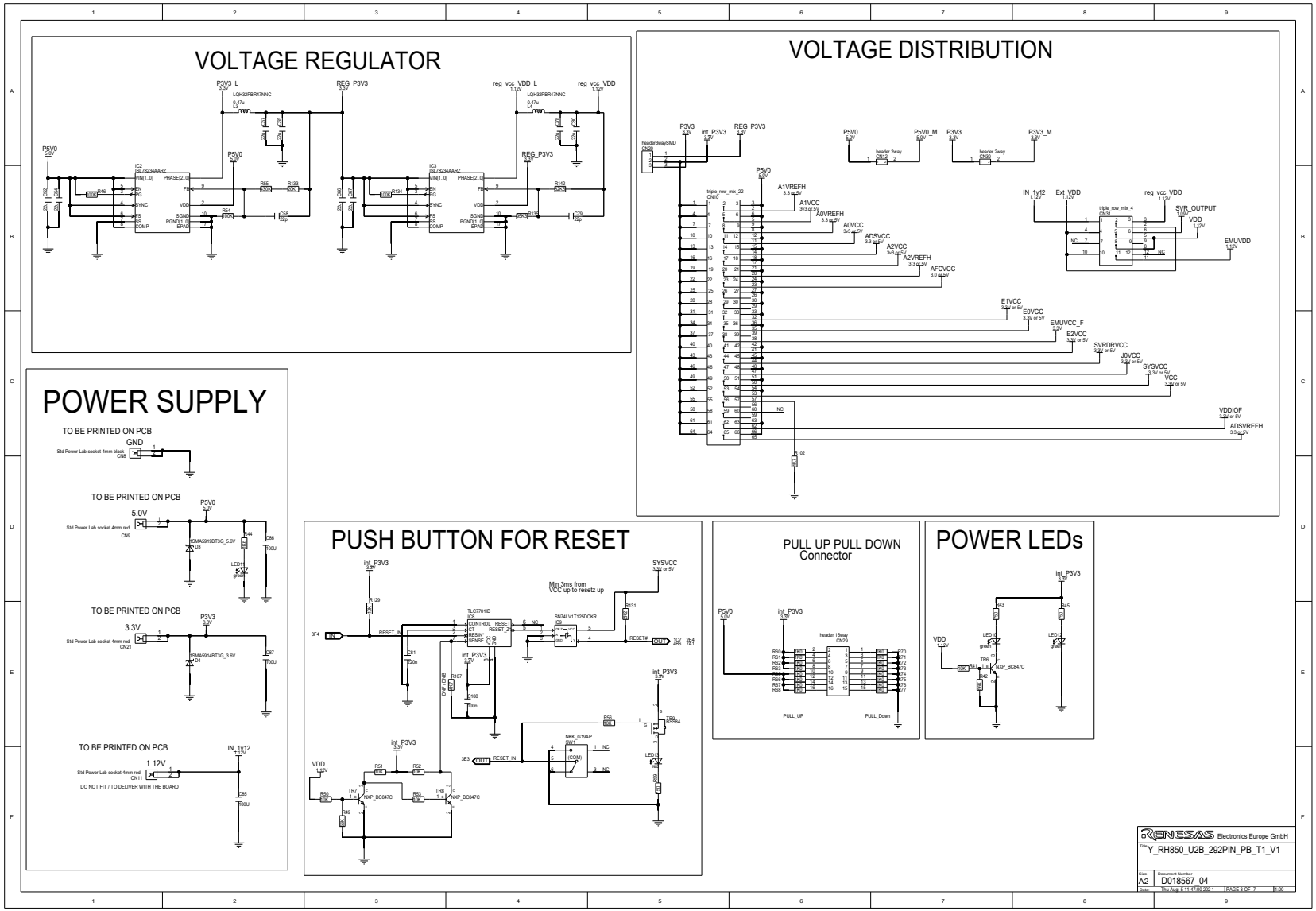
11.1.1 Page 1



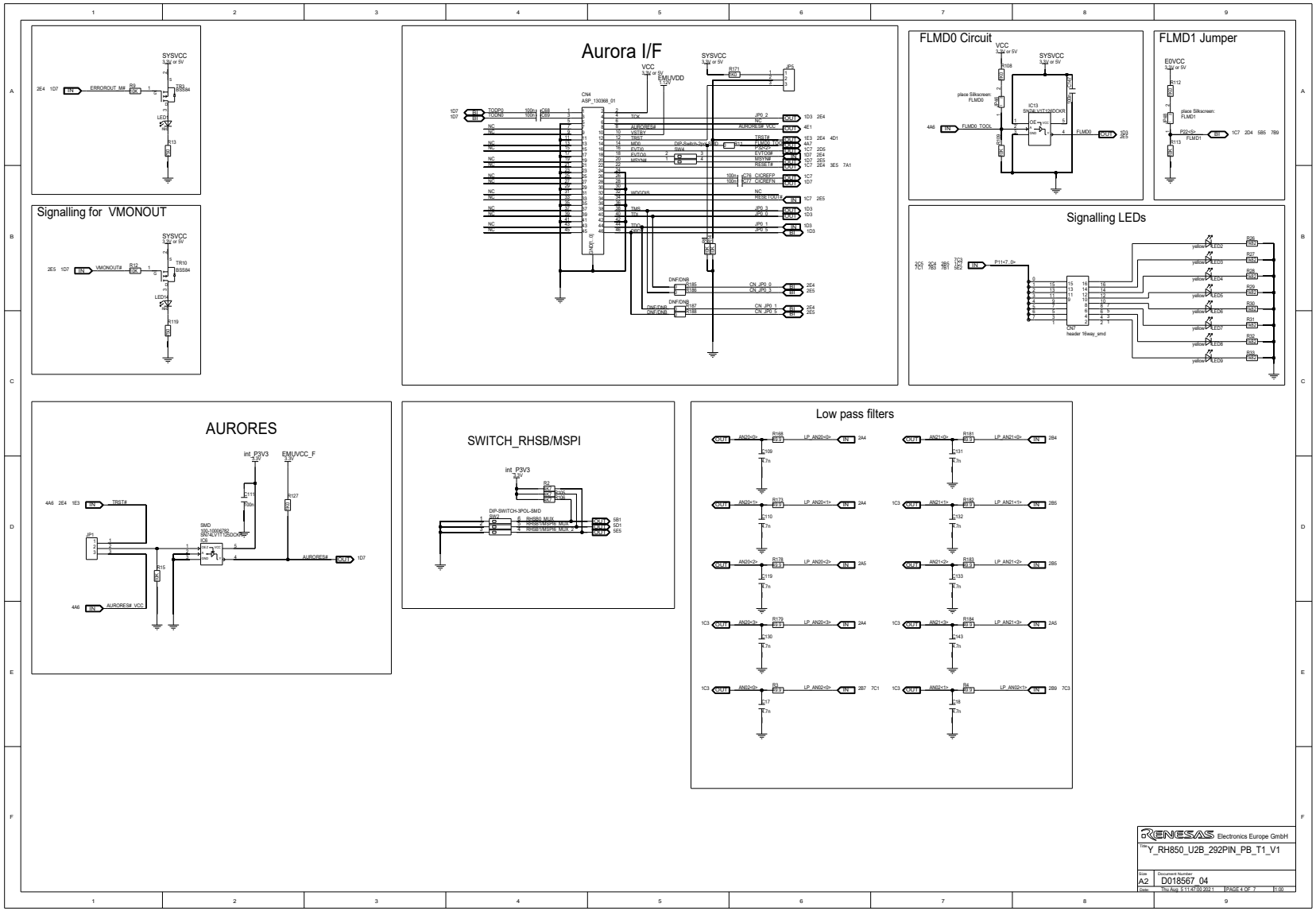
11.1.2 Page 2


CONNECTOR_top
CONNECTOR_left
CONNECTOR_down
RENESAS Electronics Europe GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
A2
D018567_04

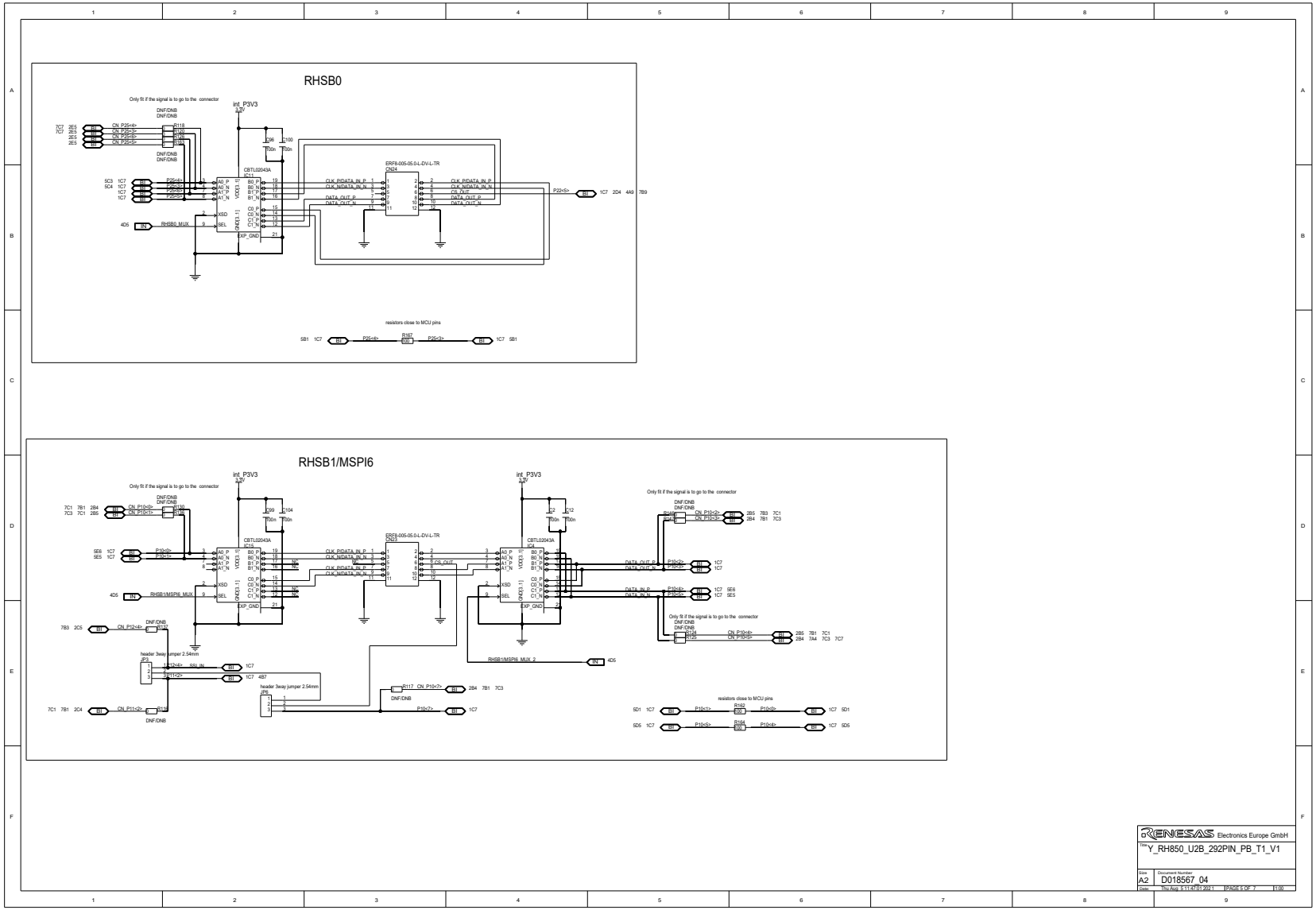
11.1.3 Page 3


VOLTAGE REGULATOR
VOLTAGE DISTRIBUTION
POWER SUPPLY
PUSH BUTTON FOR RESET
PULL UP PULL DOWN Connector
POWER LEDs
RENESAS Electronics Europe GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
D018567_04

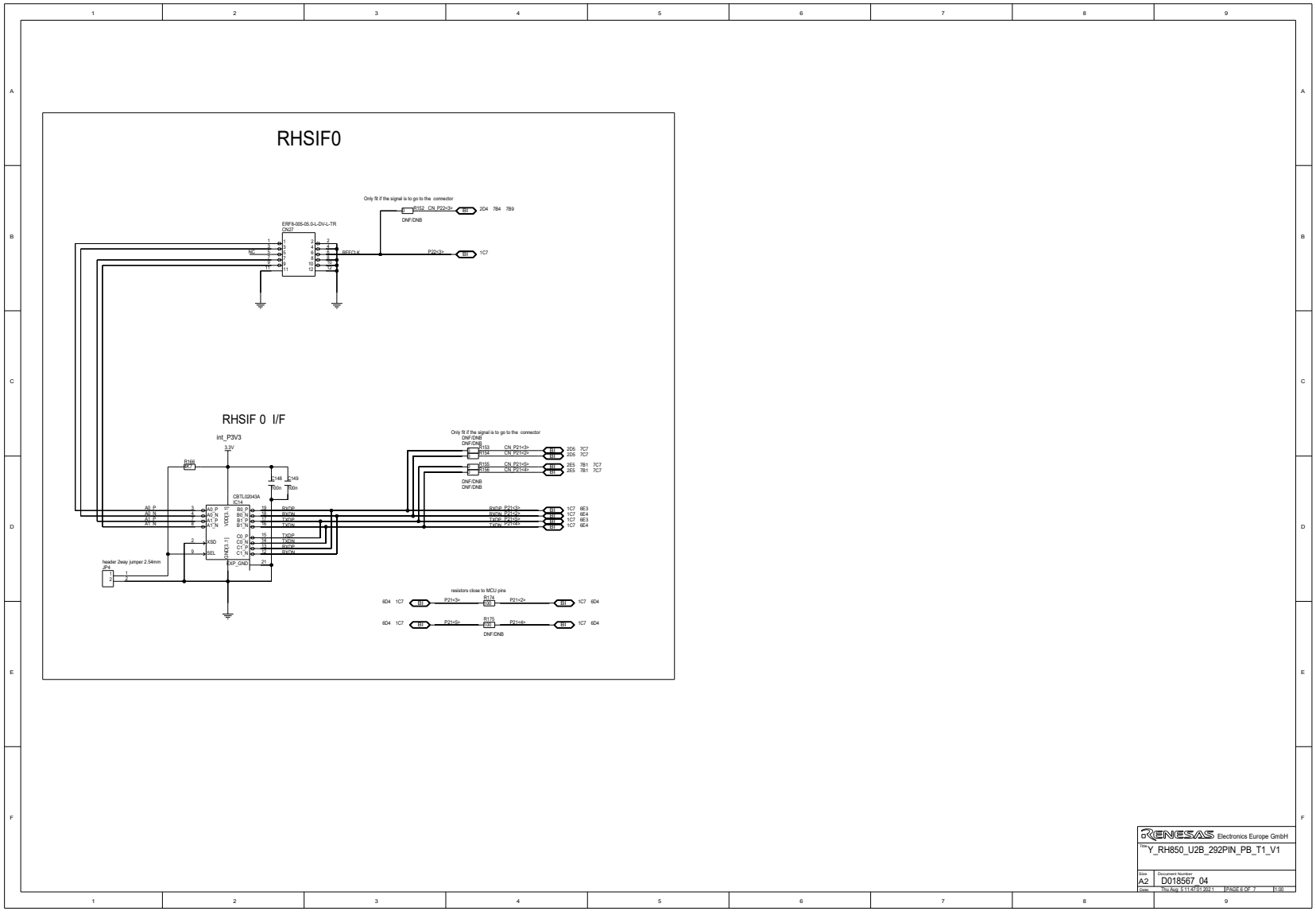
11.1.4 Page 4


Aurora I/F
FLMD0 Circuit
FLMD1 Jumper
Signalling for VMONOUT
Signalling LEDs
AURORES
SWITCH_RHSB/MSPI
Low pass filters
RENESAS Electronics Europe GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
D018567_04

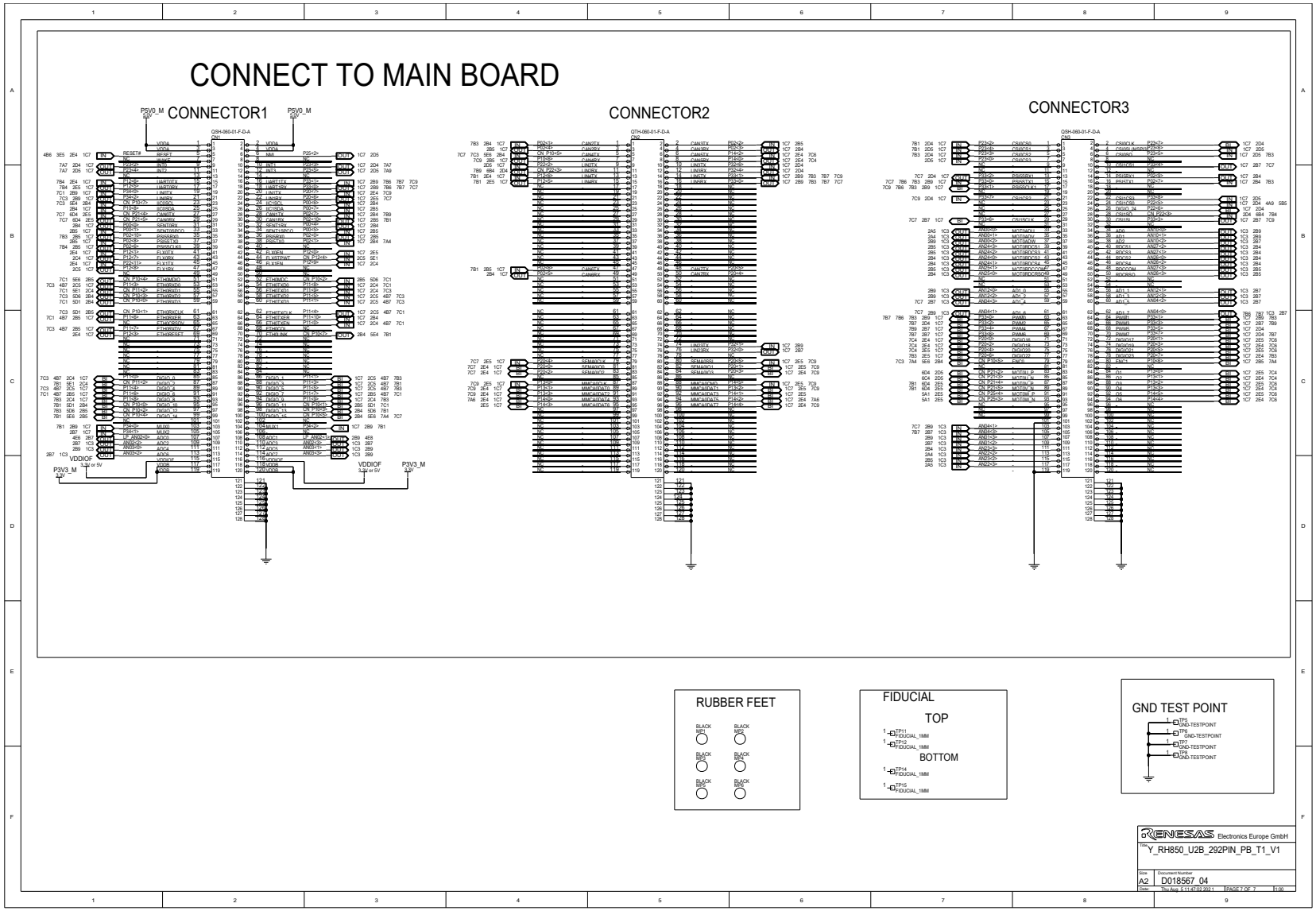
11.1.5 Page 5


RHSB0
RHSB1/MSPI6
Only fit if the signal is to go to the connector
resistors close to MCU pins
header 3way jumper 2.54mm
RENESAS Electronics Europe GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
D018567_04

11.1.6 Page 6

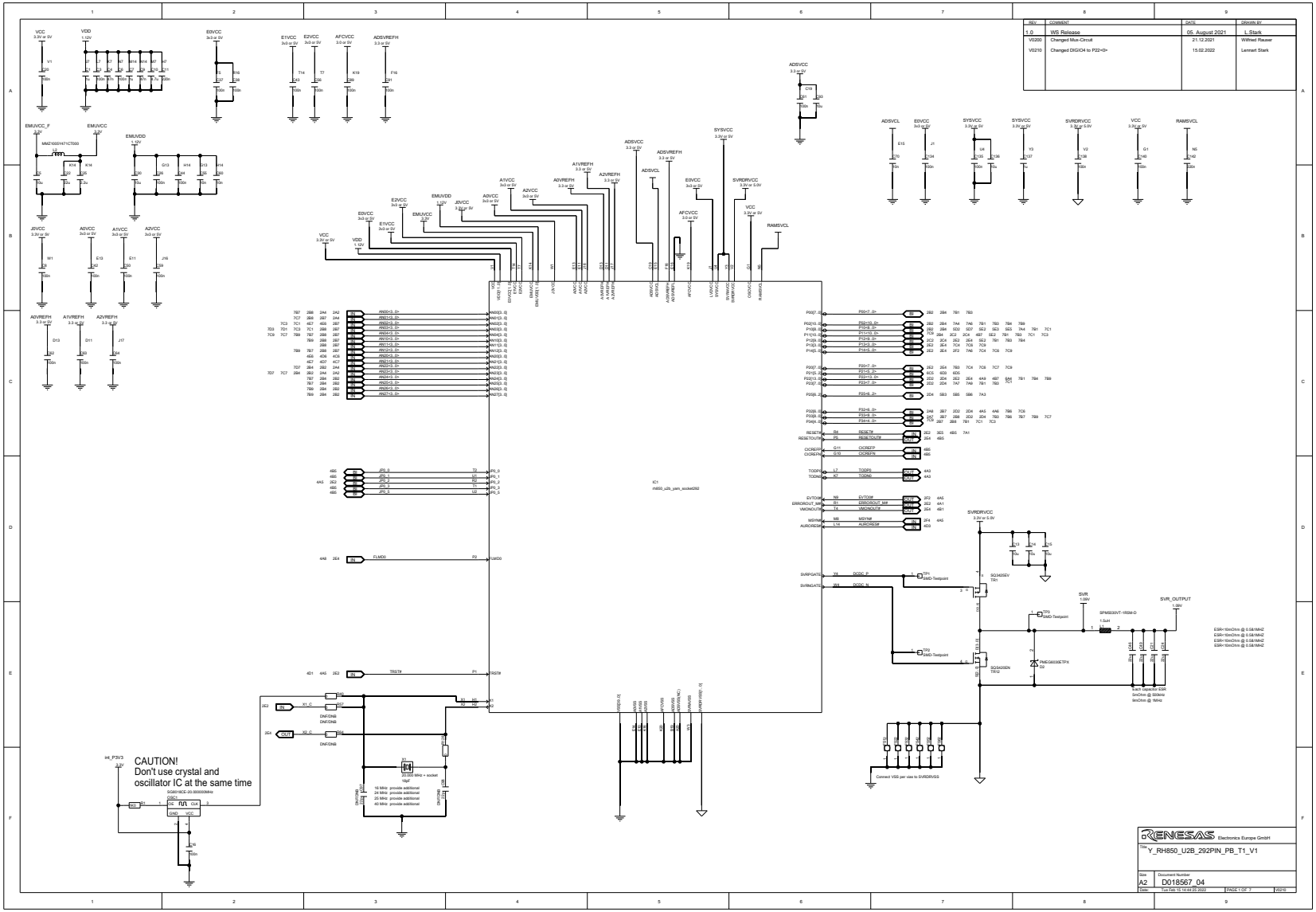

RHSIF0
RHSIF 0 I/F
int_P3V3
3.3V
header 2way jumper 2.54mm
JP4
resistors close to MCU pins
DNF/DNB
Only fit if the signal is go to the connector
RENESAS Electronics Europe GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
A2
D018567_04

11.1.7 Page 7

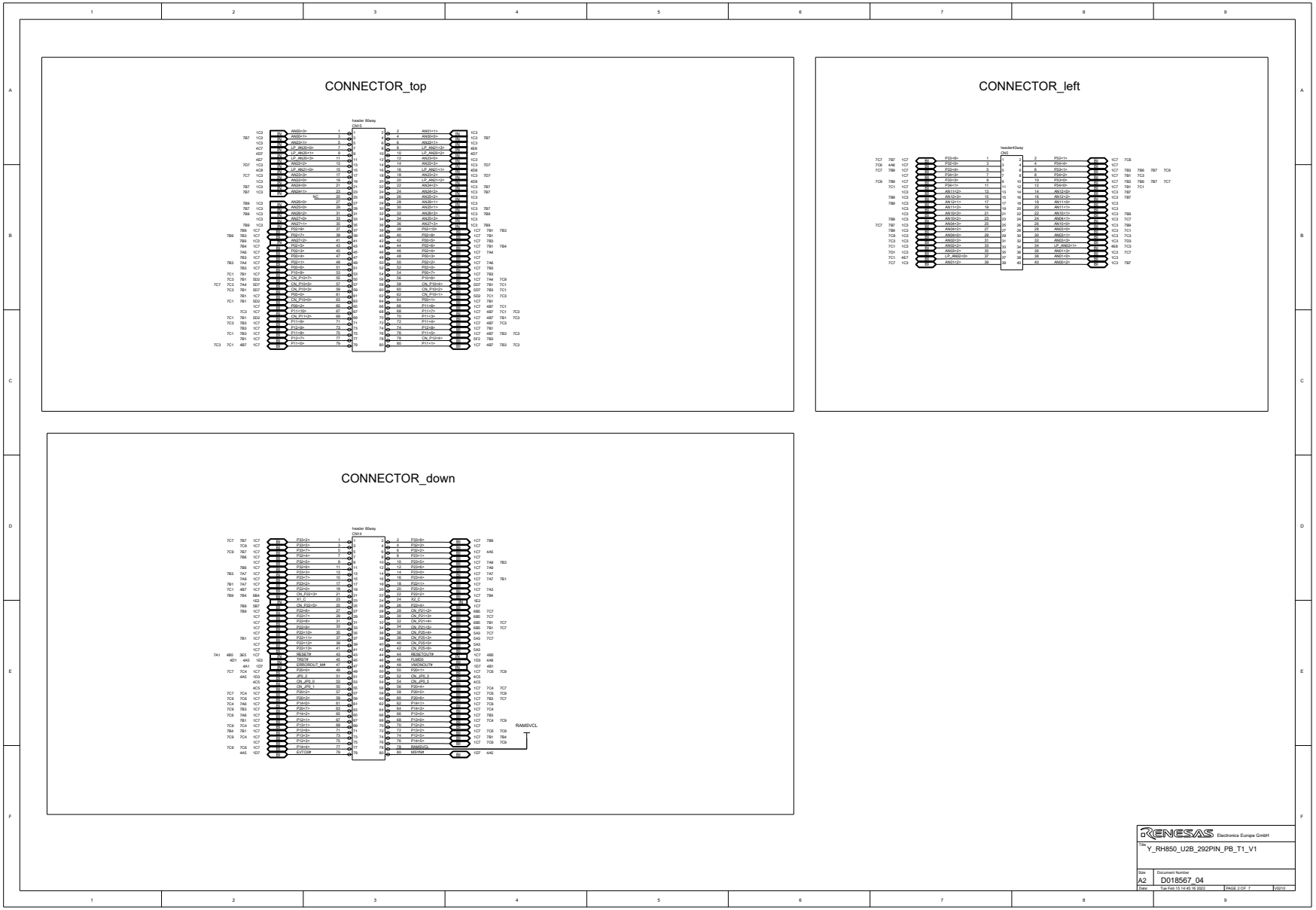

CONNECT TO MAIN BOARD
CONNECTOR1
CONNECTOR2
CONNECTOR3
RUBBER FEET
FIDUCIAL
TOP
BOTTOM
GND TEST POINT
RENESAS Electronics Europe GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
D018567_04

11.2 Board Version D018567_06_V02

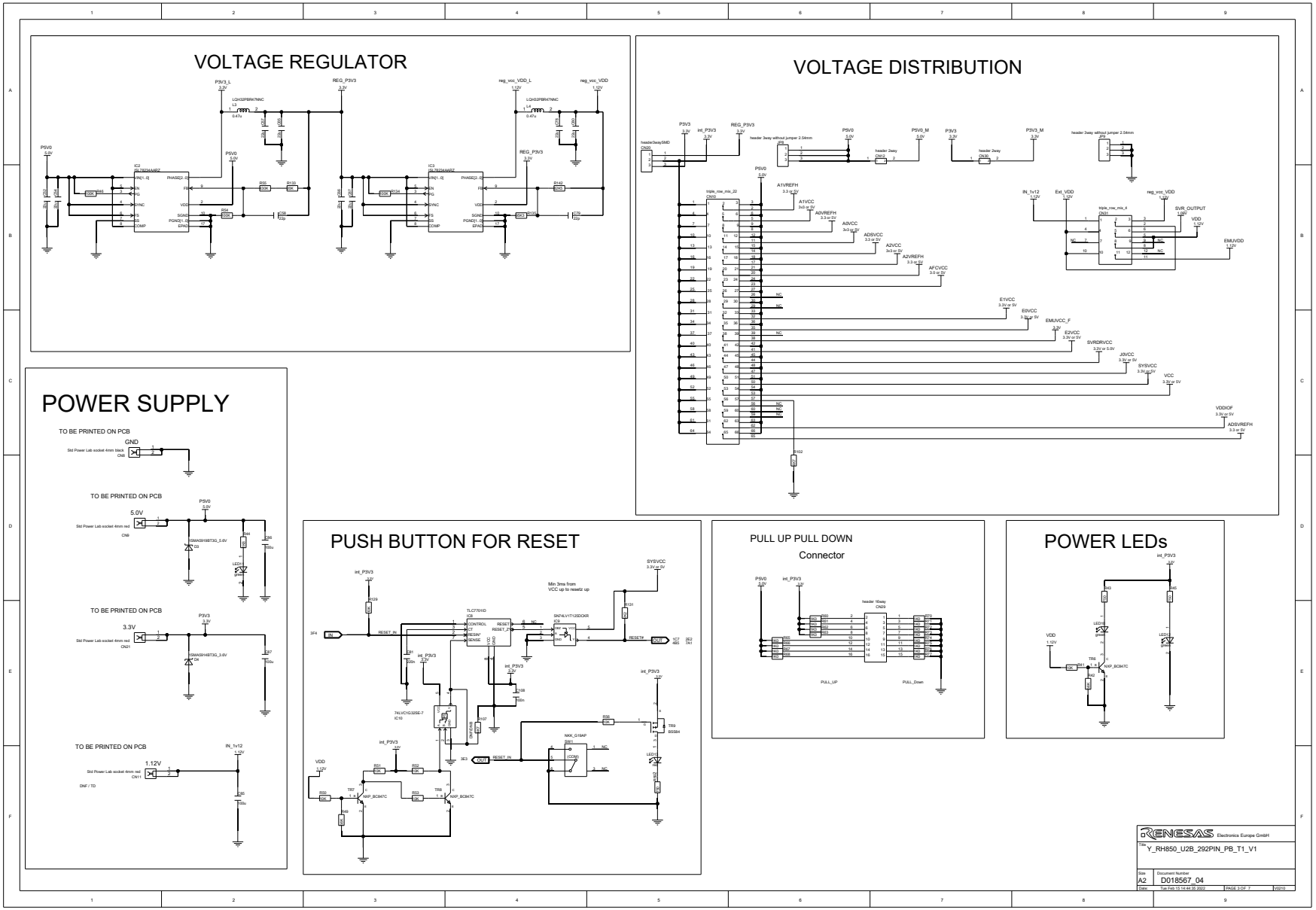
11.2.1 Page 1



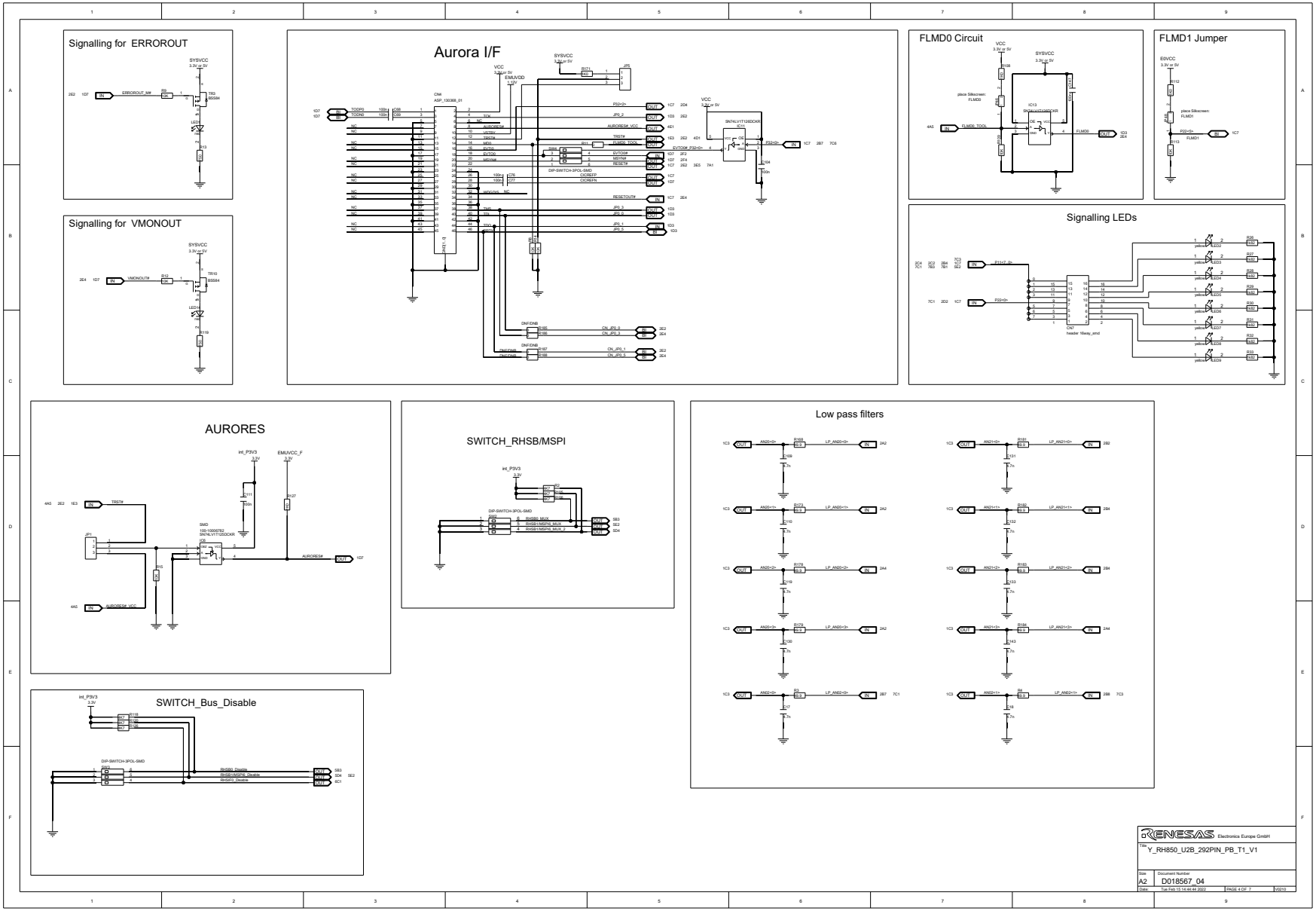
11.2.2 Page 2


CONNECTOR_top
CONNECTOR_left
CONNECTOR_down
RAMSVCL
RENESAS Electronics Europe GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
D018567_04
PAGE 2 OF 7

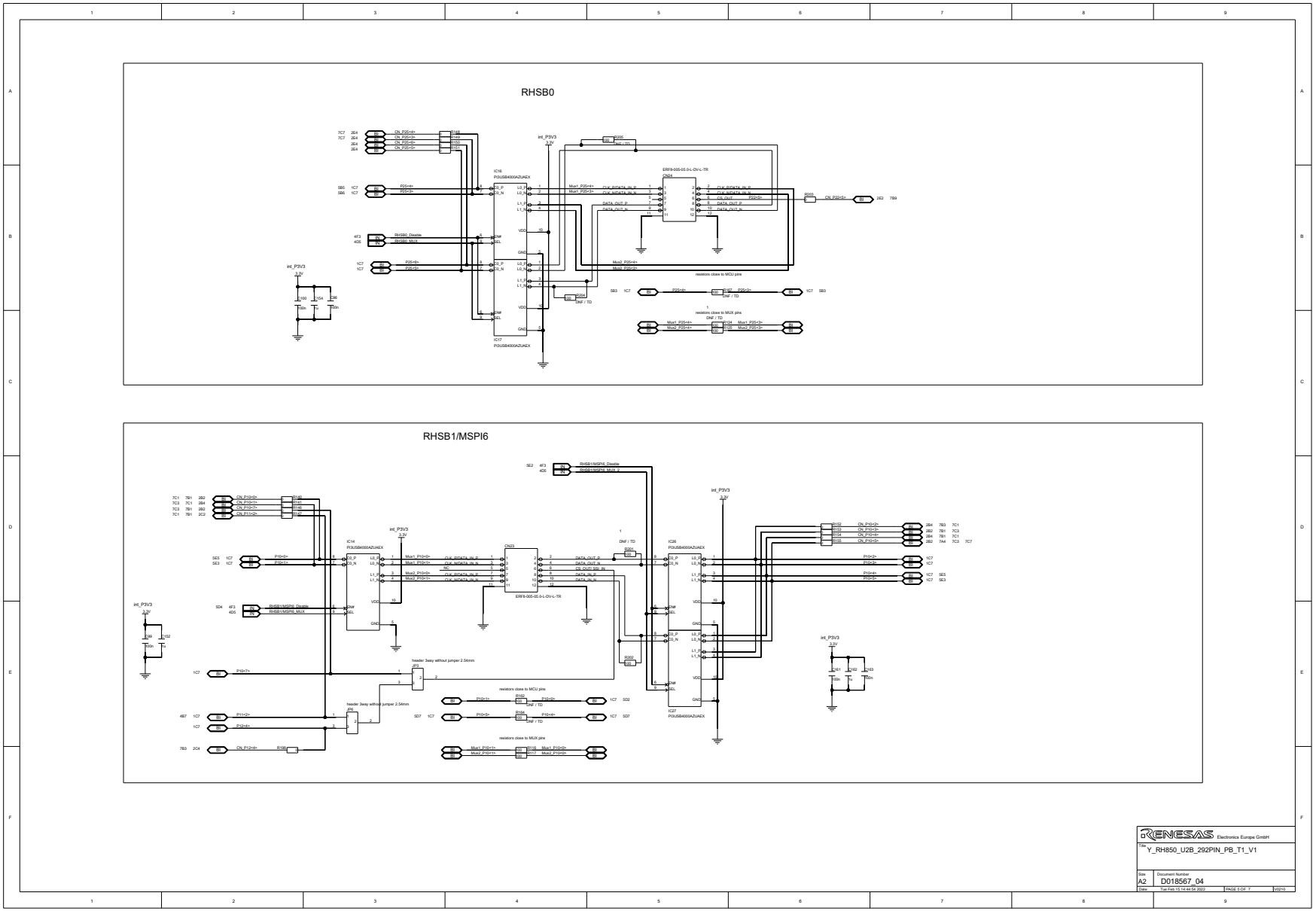
11.2.3 Page 3


VOLTAGE REGULATOR
VOLTAGE DISTRIBUTION
POWER SUPPLY
PUSH BUTTON FOR RESET
PULL UP PULL DOWN
Connector
POWER LEDs
RENESAS Electronics Europe GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
D018567_04

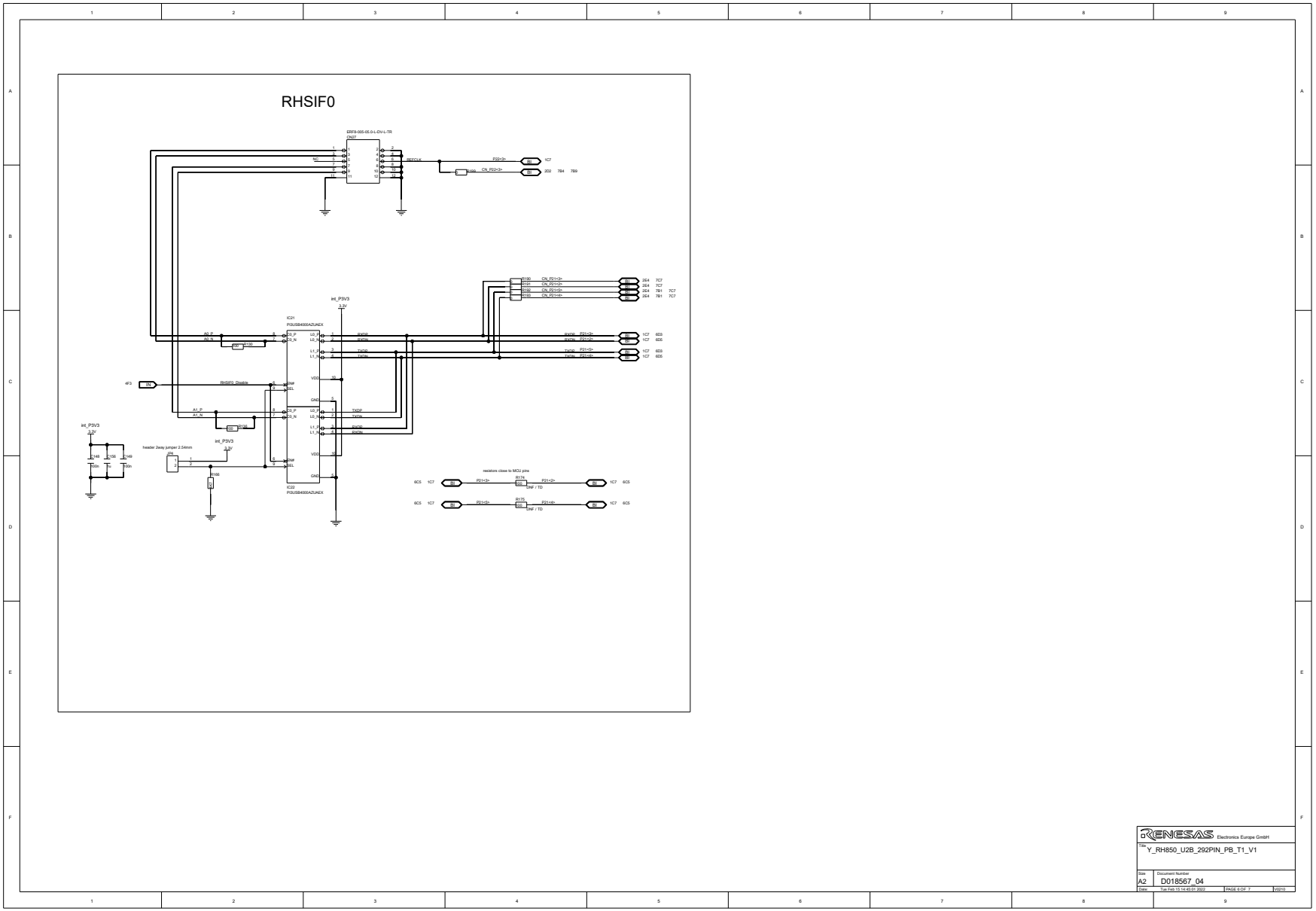
11.2.4 Page 4


Signalling for ERROROUT
Signalling for VMONOUT
Aurora I/F
FLMD0 Circuit
FLMD1 Jumper
Signalling LEDs
AURORES
SWITCH_RHSB/MSPI
Low pass filters
SWITCH_Bus_Disable
RENESAS Electronics Europe GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
D018567_04

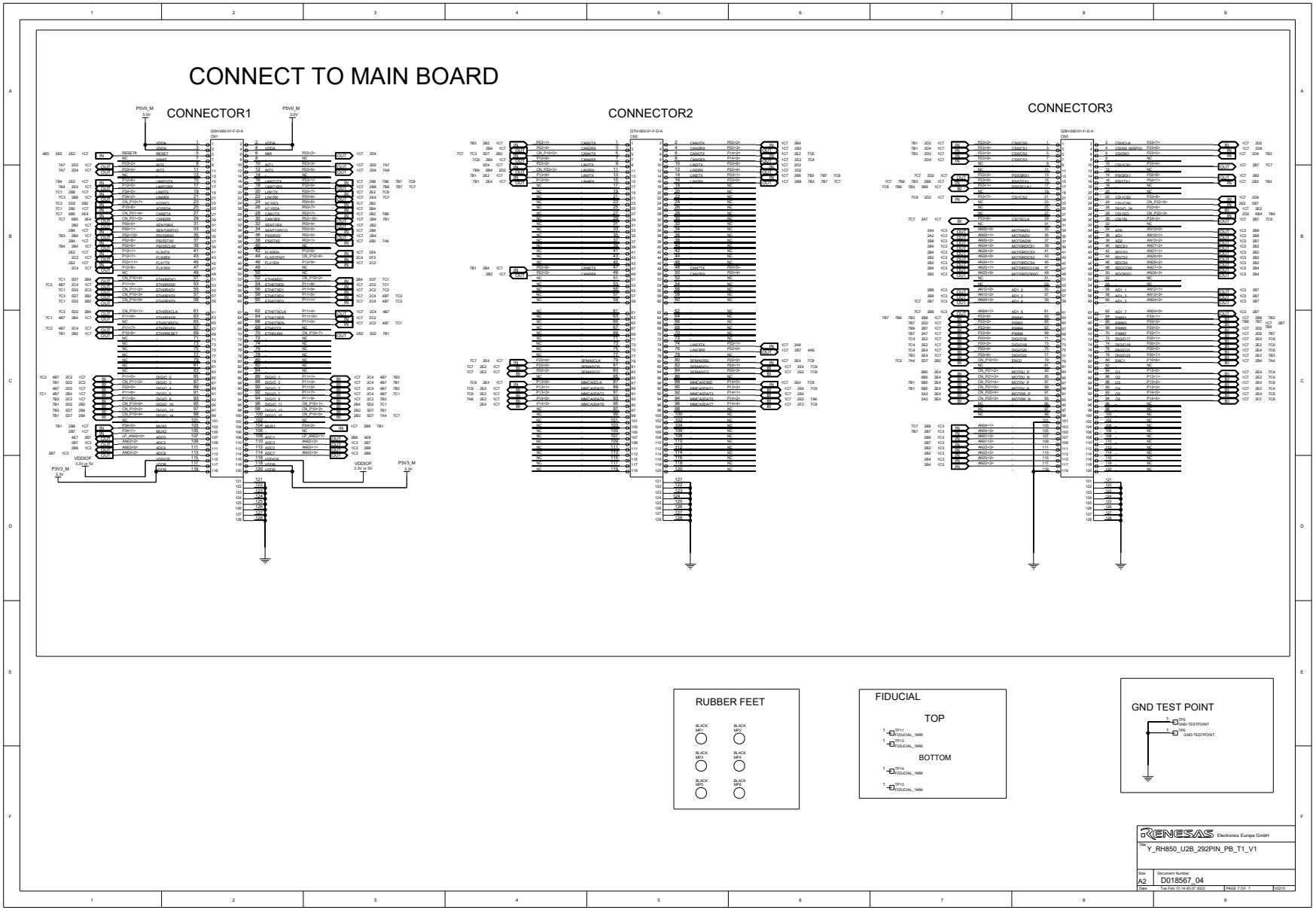
11.2.5 Page 5


RHSB0
RHSB1/MSPI6
RENESAS Electronics Europe GmbH
Title Y_RH850_U2B_292PIN_PB_T1_V1
Size A2
Document Number D018567_04
Date Tue Feb 13 14:44:54 2022
PAGE 5 OF 7
V0210

11.2.6 Page 6

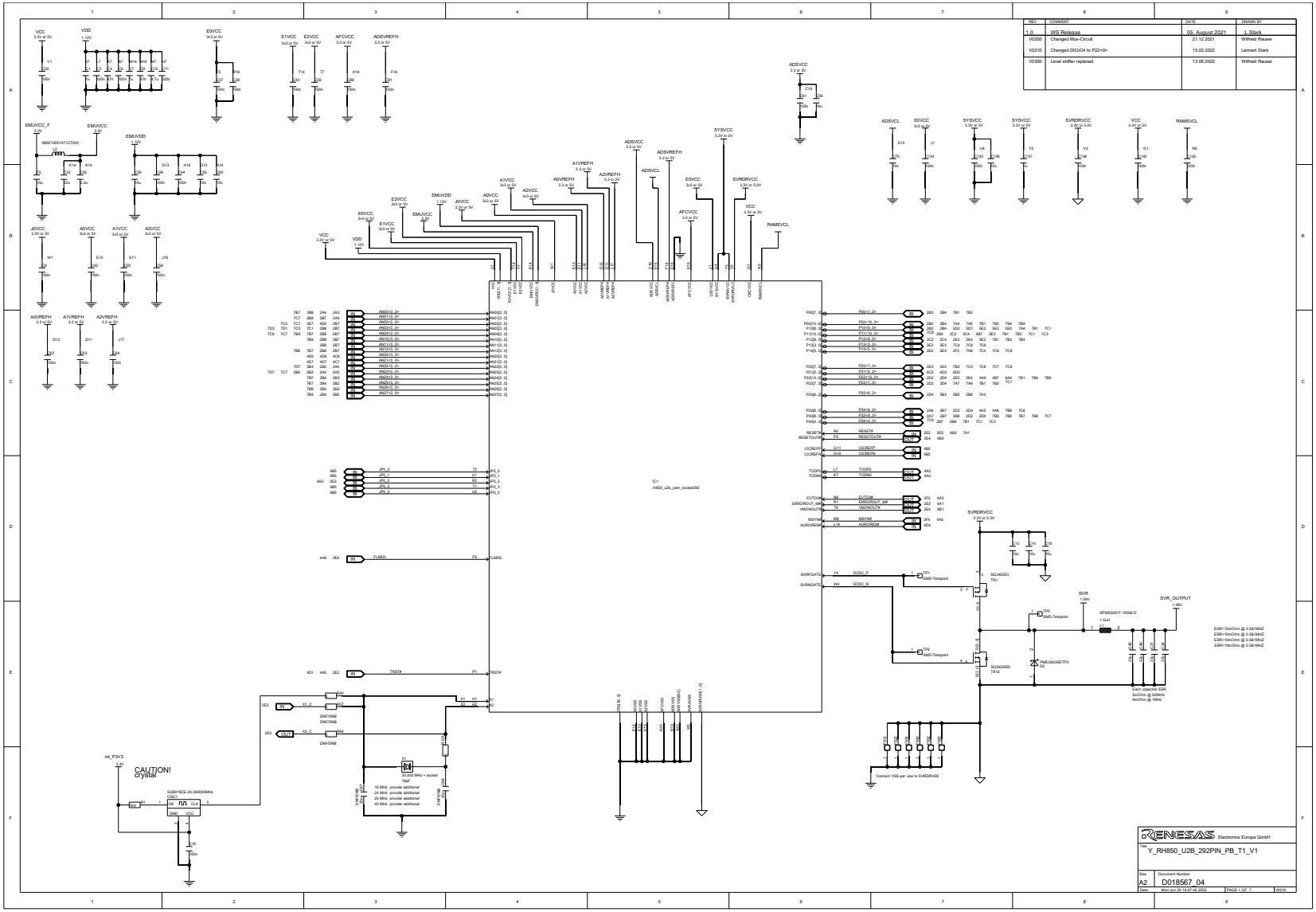

RHSIF0
Int_P3V3
header 2way jumper 2.54mm
resistors close to MCU pins
RENESAS Electronics Europe GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
D018567_04

11.2.7 Page 7

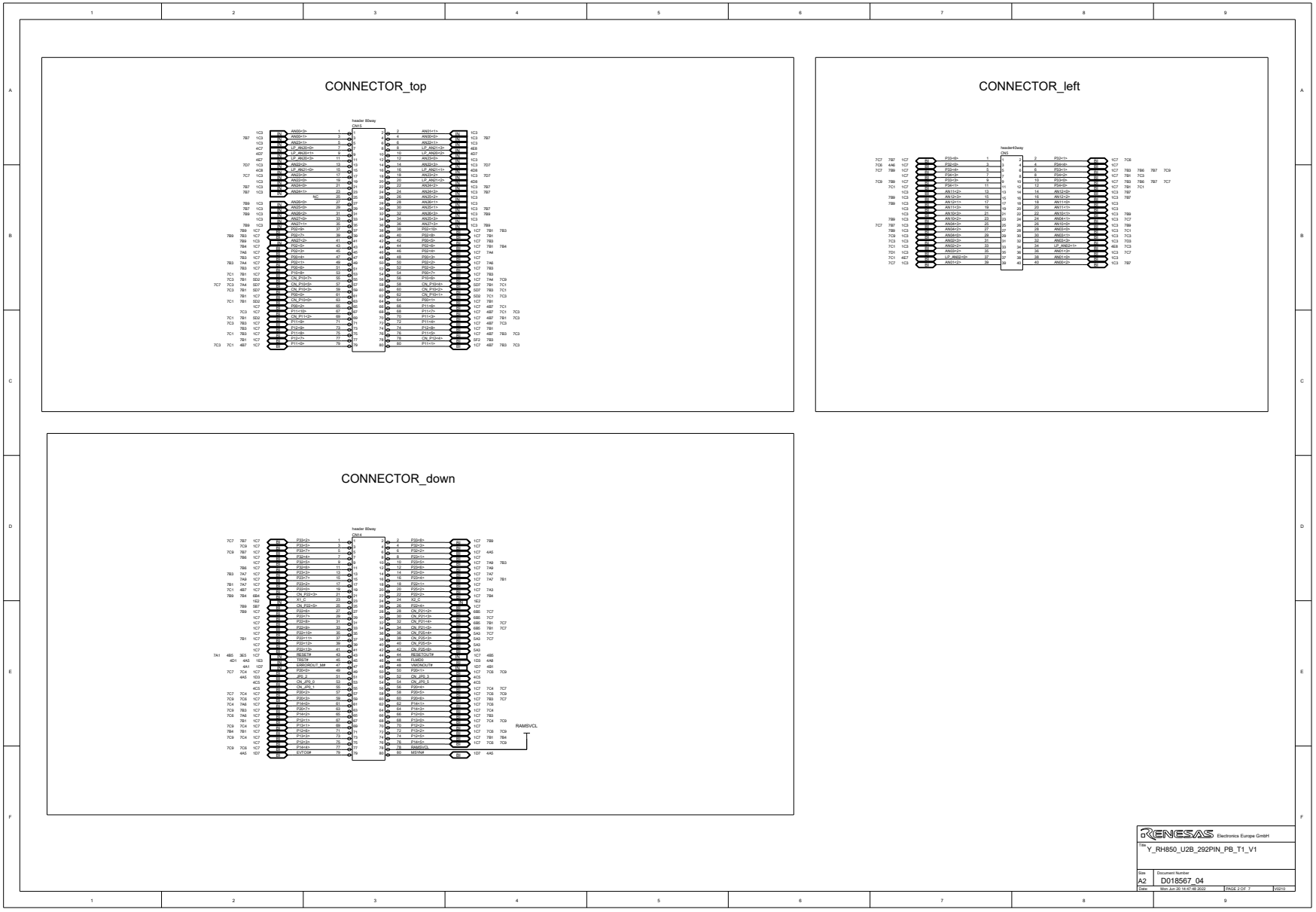

CONNECT TO MAIN BOARD
CONNECTOR1
CONNECTOR2
CONNECTOR3
RUBBER FEET
FIDUCIAL
TOP
BOTTOM
GND TEST POINT
RENESAS Electronics Europe GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
D018567_04

11.3 Board Version D018567_06_V03

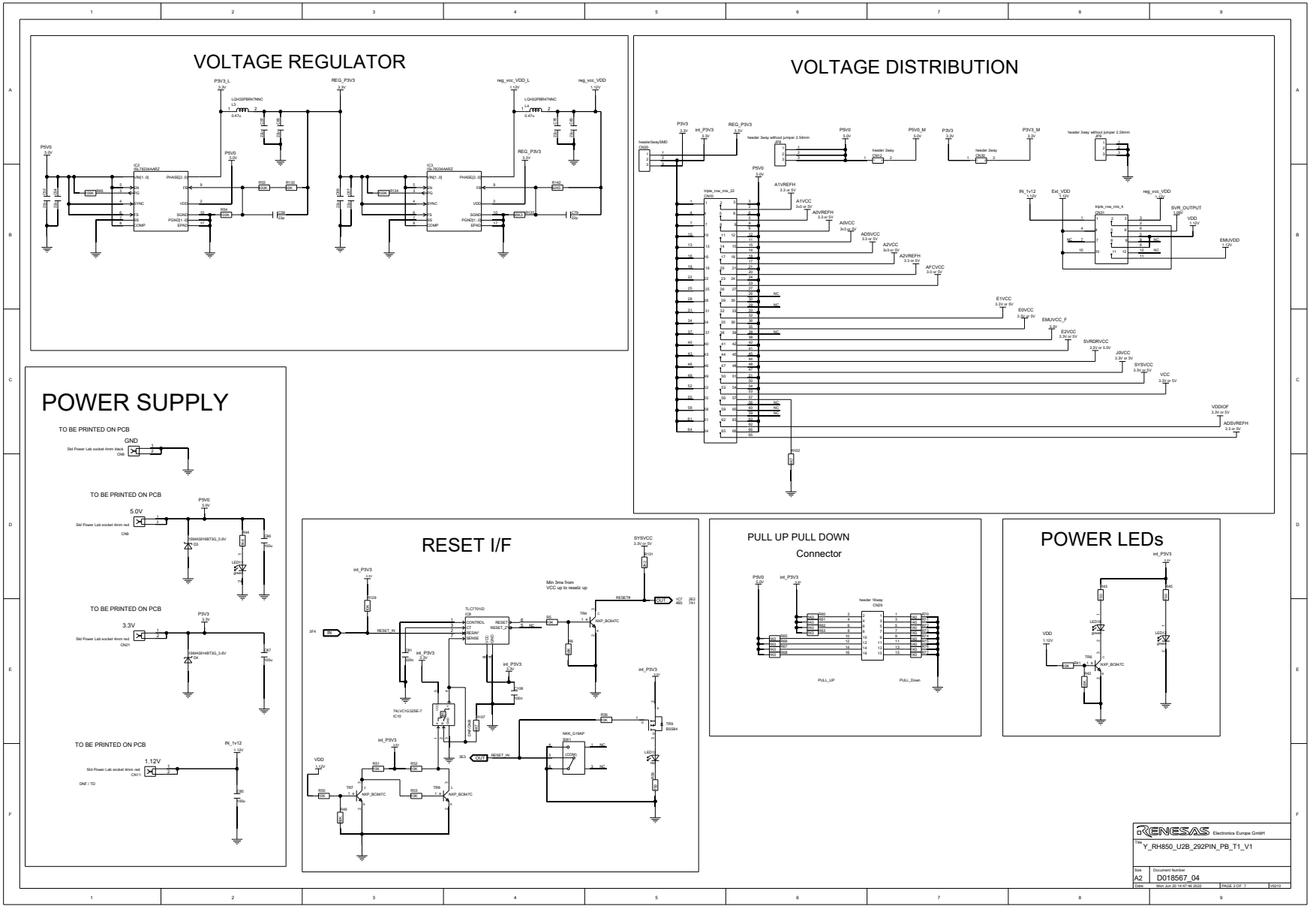
11.3.1 Page 1



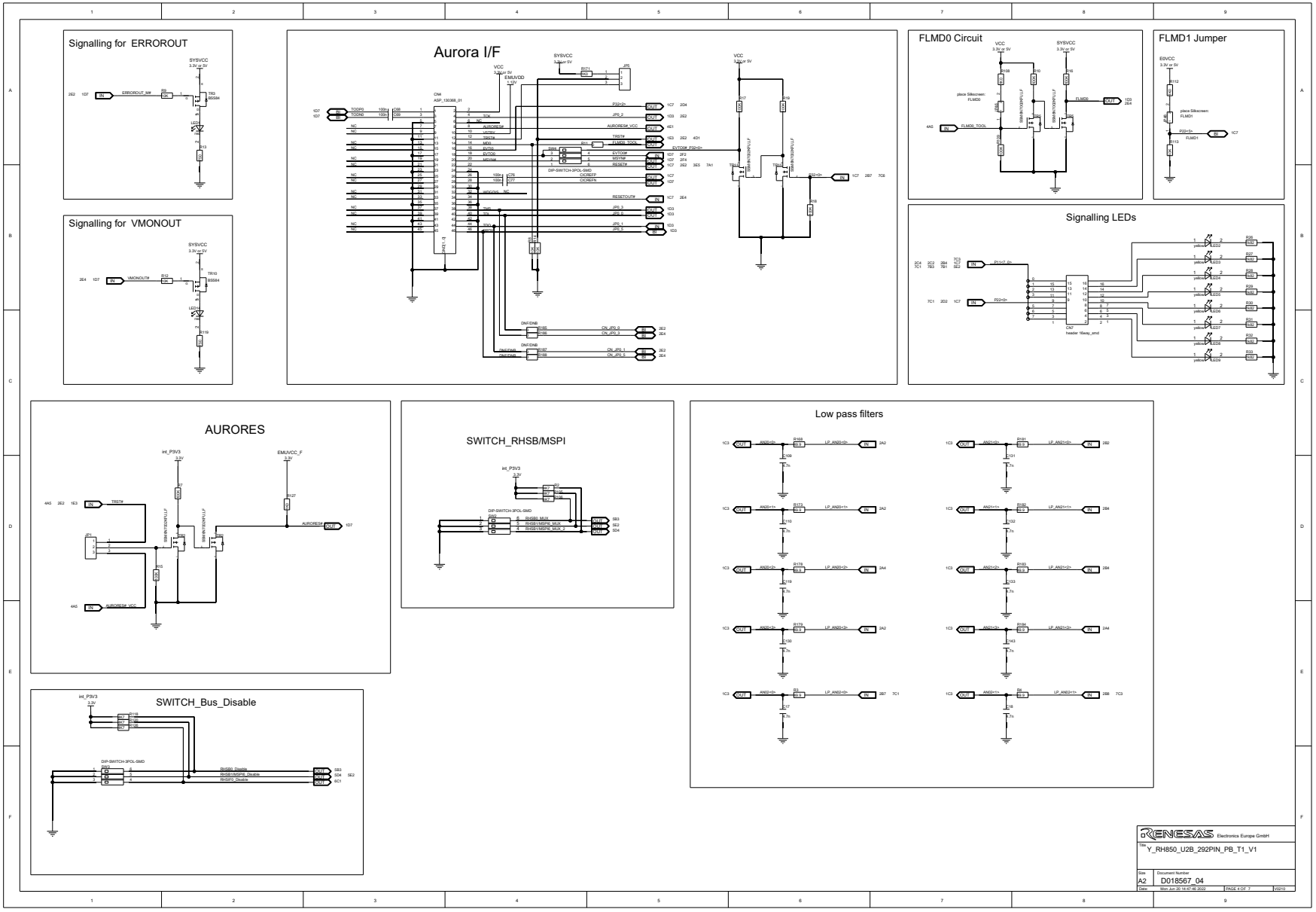
11.3.2 Page 2


CONNECTOR_top
CONNECTOR_left
CONNECTOR_down
RAMSVCL
RENESAS Electronics Europa GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
A2
D018567_04
Mon Jun 20 14:47:48 2022
PAGE 2 OF 7
V0210

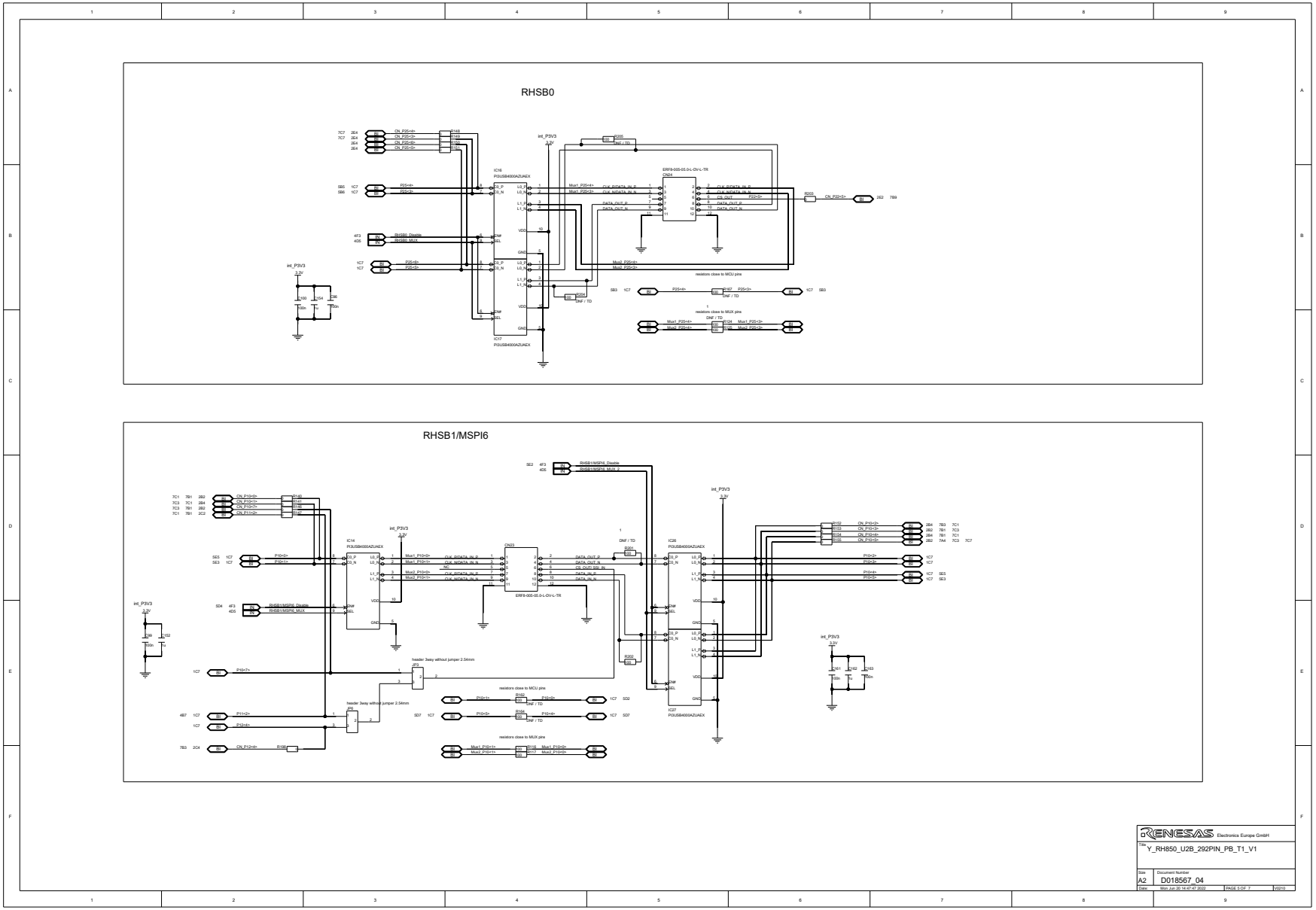
11.3.3 Page 3


VOLTAGE REGULATOR
VOLTAGE DISTRIBUTION
POWER SUPPLY
TO BE PRINTED ON PCB
GND
5.0V
3.3V
1.12V
RESET I/F
PULL UP PULL DOWN
Connector
POWER LEDs
RENESAS Electronics Europe GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
A2
D018567_04

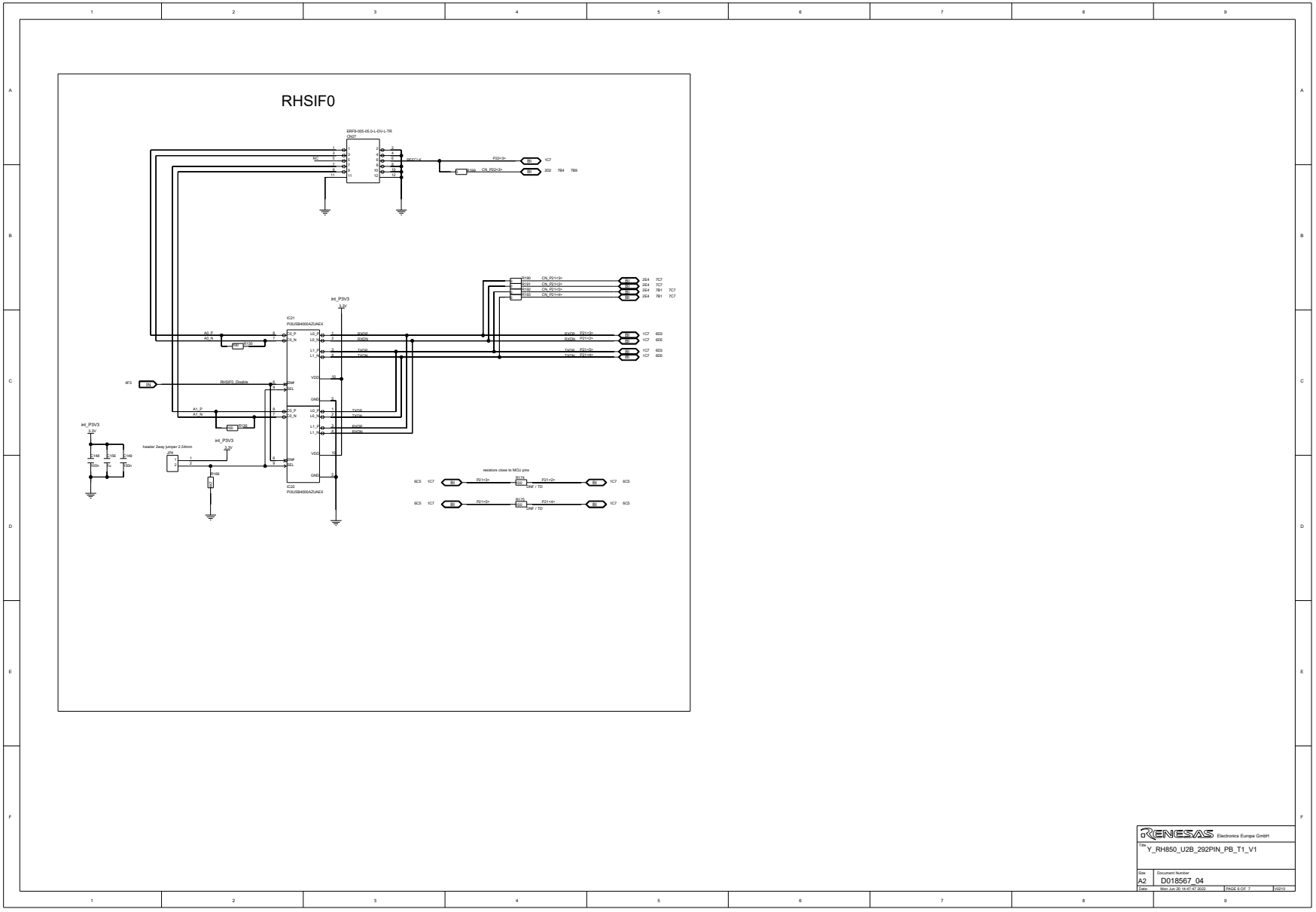
11.3.4 Page 4


Signalling for ERROROUT
Signalling for VMONOUT
Aurora I/F
FLMD0 Circuit
FLMD1 Jumper
Signalling LEDs
AURORES
SWITCH_RHSB/MSPI
Low pass filters
SWITCH_Bus_Disable
RENESAS Electronics Europa GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
D018567_04

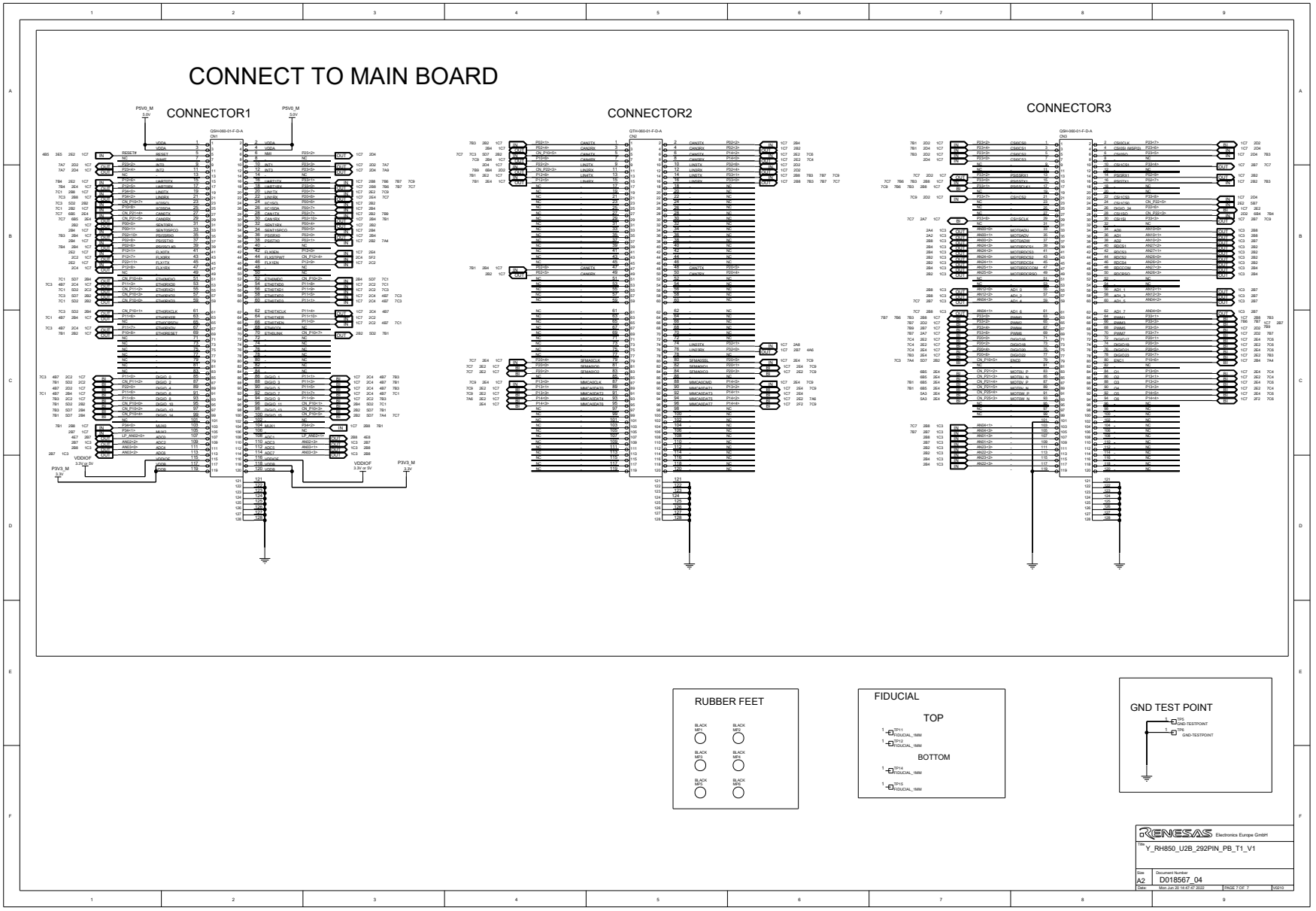
11.3.5 Page 5


RHSB0
RHSB1/MSPI6
RENESAS Electronics Europa GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
D018567_04

11.3.6 Page 6


RHSIF0
int_P3V3
3.3V
IC2Y
IC2Z
header 2way jumper 2.54mm
resistors close to MCU pins
DNF / TD
RENESAS Electronics Europe GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
Size A2
Document Number D018567_04
Mon Jun 20 14:47:47 2022
PAGE 6 OF 7
V0210

11.3.7 Page 7


CONNECT TO MAIN BOARD
CONNECTOR1
CONNECTOR2
CONNECTOR3
RUBBER FEET
FIDUCIAL
TOP
BOTTOM
GND TEST POINT
RENESAS Electronics Europa GmbH
Y_RH850_U2B_292PIN_PB_T1_V1
D018567_04

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
V1.00	2021-10-06	–	Initial release
V1.01	2021-10-11	18	Updated processor type names in Table 1.4 Type names for FCC and MP devices
V2.00	2022-06-10	–	New release for updated hardware
V2.01	2022-06-23	7	Corrected document CD number in *Table 1.1 Package Components for the Y-RH850-U2B-292PIN-PB-T1-V1*
V3.00	2022-11-04	90 - 96	Added circuit diagrams for board revision V03.
V3.01	2023-10-26	25, 73	Added precaution about power on of piggyback board without a microcontroller mounted. Caution in *3.1 Board Power Connection*. *9.3 Power On Piggyback Board Without RH850 Microcontroller installed*
V3.02	2025-05-15	36, 66	Added explanation for FLMD1 setting in Serial Programming Mode
		29	Updated explanation for core voltage generation in chapter *3.3 Device Core Voltage (VDD) Selection.*
		7	Updated package components list in *Table 1.1*.
V3.03	2026-03-20	18	Updated device list in *Table 1.4*.

RH850/U2B 292pin Piggyback Board V1 User's Manual: Piggyback Board

Publication Date: Rev.3.03 March 20, 2026

Published by: Renesas Electronics Corporation

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Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
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Renesas Electronics India Pvt. Ltd.
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Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 5.0

RH850/U2B 292pin

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