

Important Notes

Restrictions in Use

IDT's ZAMC4100 Application Board is designed for ZAMC4100 evaluation under application specific environmental conditions, e.g. thermal performance.

IDT's Application Kit must not be used for module production or production test setups.

Disclaimer

IDT shall not be liable for any damages arising out of defects resulting from

- (i) delivered hardware
- (ii) non-observance of instructions contained in this manual and in any other documentation provided to user, or
- (iii) misuse, abuse, use under abnormal conditions, or alteration by anyone other than IDT.

To the extent permitted by law, IDT hereby expressly disclaims and user expressly waives any and all warranties, whether express, implied, or statutory, including, without limitation, implied warranties of merchantability and of fitness for a particular purpose, statutory warranty of non-infringement, and any other warranty that may arise by reason of usage of trade, custom, or course of dealing.

Contents

1	Introduction	3
1.1.	Contents of Kit	3
1.2.	ZAMC4100 Application Board	3
1.3.	Pin and Signal Description	4
2	Hardware Description	6
2.1.	Power Supply	6
2.2.	Local Interconnect Network (LIN)	6
2.3.	Position Sensing	7
2.4.	External Temperature Measurement	7
2.5.	High-Side Drives (HS1-HS4), ECM	8
2.6.	Half-Bridge Drives (HB1-HB4)	8
2.7.	JTAG Connector (J1)	9
2.8.	General Purpose Input / Outputs (GPIO 0 to 7)	9
3	Application Design Guidelines	10
4	Related Documents	13
5	Glossary	14
6	Document Revision History	14
	Appendix A: Schematic	15
	Appendix B: Bill of Materials	16
	Appendix C: PCB Layout	17

List of Figures

Figure 1.1	ZAMC4100 Application Board	3
Figure 2.1	ZAMC4100 Application Kit – Power Supply	6
Figure 2.2	ZAMC4100 Application Kit – LIN	6
Figure 2.3	Application Kit – Position Sense	7
Figure 2.4	ZAMC4100 Application Kit – Analog Inputs.....	7
Figure 2.5	ZAMC4100 Application Kit – High-Side Drivers	8
Figure 2.6	ZAMC4100 Application Kit – Half-Bridge Drivers	8
Figure 2.7	ZAMC4100 Application Kit – JTAG Interface	9
Figure 2.8	ZAMC4100 Application Kit – JPIOs.....	9
Figure 3.1	ZAMC4100 Application Kit – PCB Structure.....	10
Figure 3.2	Motor Driver Position	11
Figure 3.3	Signal Vias Placement.....	11
Figure 3.4	Component Package and Recommended Footprint	12
Figure 3.5	Multi-via Connections	12
Figure 3.6	Local Heat-Sinks.....	13

List of Tables

Table 1.1	Component Description	4
Table 6.1	Bill of Materials.....	16

1 Introduction

This document describes the use of the ZAMC4100 Application Kit.

1.1. Contents of Kit

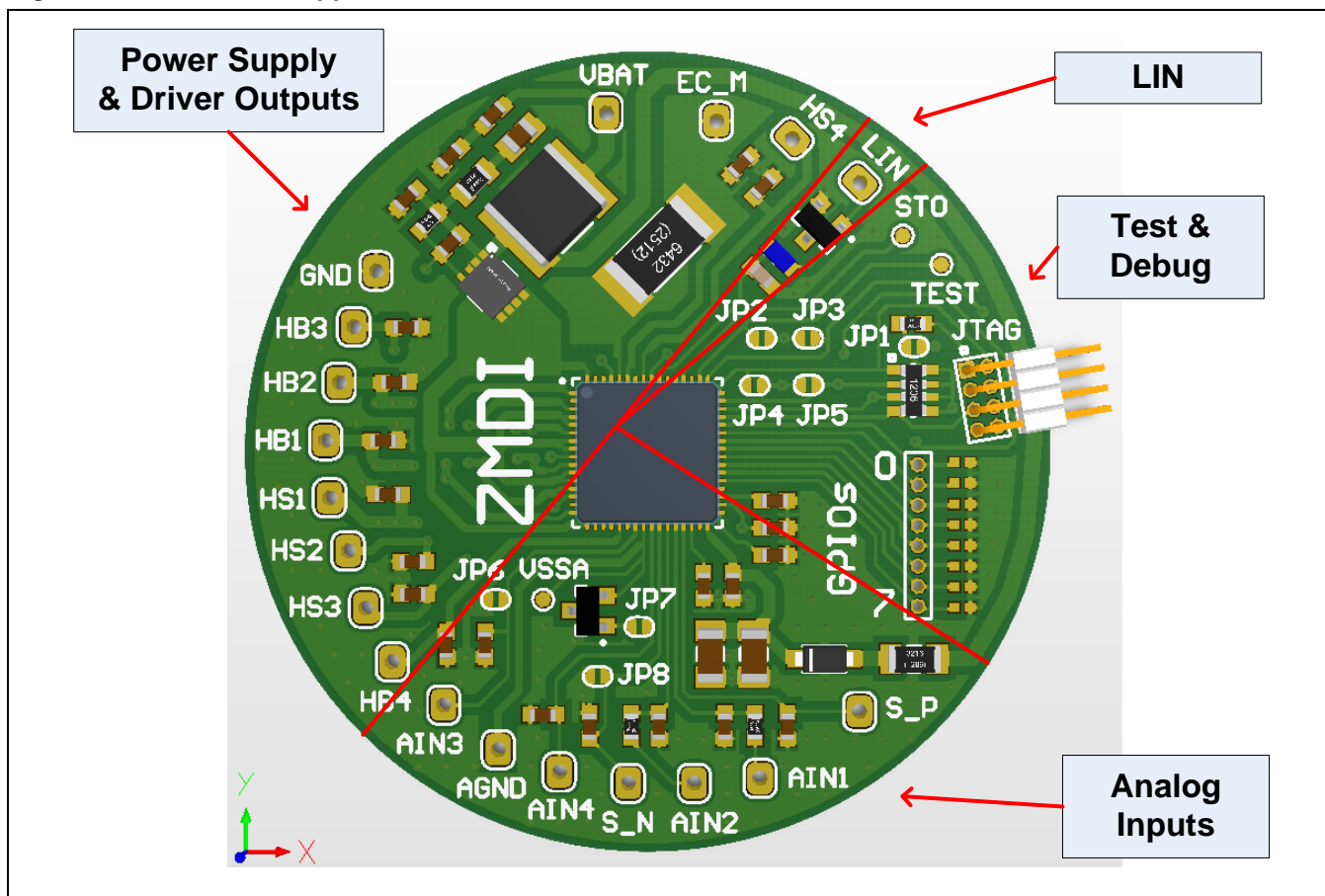
The kit consists of one part: the ZAMC4100 Application Board.

1.2. ZAMC4100 Application Board

The enclosed ZAMC4100 Application Kit is designed for evaluation of the ZAMC4100 Actuator and Motor Controller's performance under conditions typical for the intended application. It can be used for quick user prototyping, thermal performance evaluation under environmental stress, EMC components selection, etc.

Note: The on-board ZAMC4100 device is unprogrammed.

Figure 1.1 ZAMC4100 Application Board



1.3. Pin and Signal Description

See the schematic in Appendix A and Figure 1.1 for the connection points and signals given in Table 1.1.

Table 1.1 Component Description

Connector/ Test Point	Signal(s)	Function
J1	JTAG	Interface for MCU firmware download
J2	VBAT	Power supply input
J3	GND	Power ground. All signals are referenced to this voltage
J4	EC_M	Electrochromatic glass driver output
J5	LIN	Local Interconnect Network (LIN)
J6	HS1	High-side driver output 1
J7	HS2	High-side driver output 2
J8	HS3	High-side driver output 3
J9	HS4	High-side driver output 4
J10	AIN3	General purpose ADC input
J11	GPIOs	General purpose logical I/Os
J12	AIN4	General purpose ADC input
J13	AGND	Reference signal ground for off-board analog sensors
J14	HB1	Half-bridge driver output 1
J15	HB2	Half-bridge driver output 2
J16	HB3	Half-bridge driver output 3
J17	HB4	Half-bridge driver output 4
J18	S_P	Positive power supply for external position sensors
J19	AIN1	Analog input for external position sensor 1
J20	AIN2	Analog input for external position sensor 2
J21	S_N	Negative power supply for external position sensors
JP1	3.3V	Connects the internal ZAMC4100 3.3V regulator output to JTAG connector
JP2	TEST	Connect TEST pin to GND when not used; mandatory for normal operation
JP3	TRSTN	Connect TRSTN pin to GND when not used for enhanced EMC robustness
JP4	TCK	Connect TCK pin to GND when not used for enhanced EMC robustness

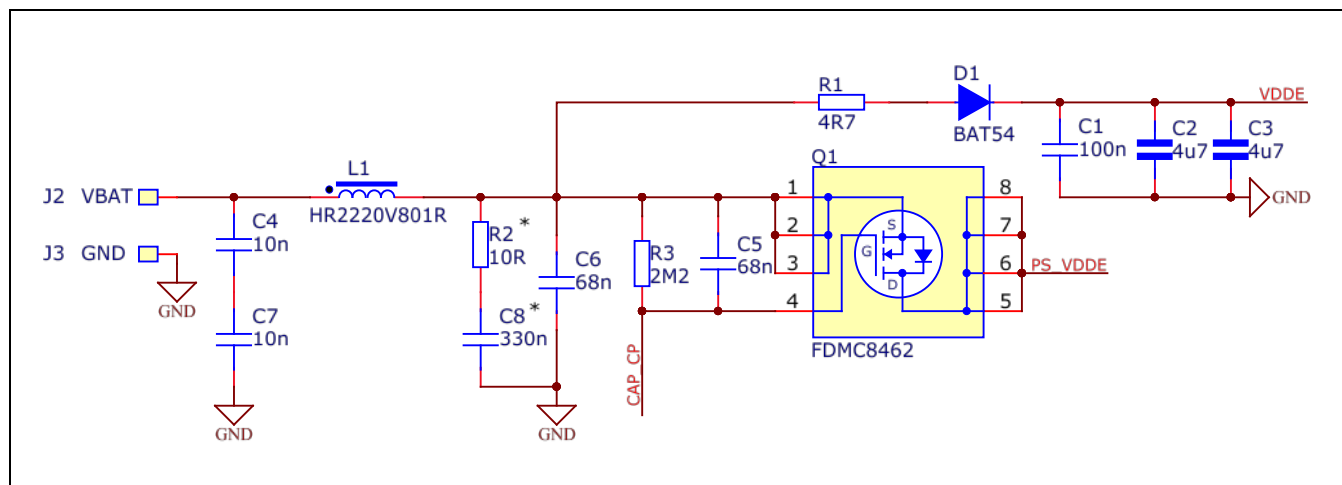
Connector/ Test Point	Signal(s)	Function
JP5	TMS	If TMS pin is not used, connect it to GND for enhanced EMC robustness
JP6	AIN3	If AIN3 pin is not used, connect it to GND for enhanced EMC robustness
JP7	AIN4	Enables the on-board temperature sensor
JP8	S_N	Connects the negative reference ADC input to GND in ratiometric mode
TP1	STO	Used for debugging; in NORMAL Mode this is the internal ZAMC4100 power-on reset (POR) signal
TP2	TEST	Used for debugging
TP3	VSSA	Sense ground reference point for analog input signals
X1 to X8	GPIO0 to 7	If not used, connect GPIOs to GND; if used, add pull-down resistors or filtering capacitors here

2 Hardware Description

2.1. Power Supply

Reverse polarity protection is provided by the Q1 P MOSFET with low ON-resistance and a low driving voltage (see Figure 2.1). PS_VDDE is the supply for the output drivers. VDDE supplies the remaining circuits in the ZAMC4100 (microcontroller, communication, ADC, etc.). The values of R2 and C8 in the snubber circuit are typical, and might differ from one application to another.

Figure 2.1 ZAMC4100 Application Kit – Power Supply

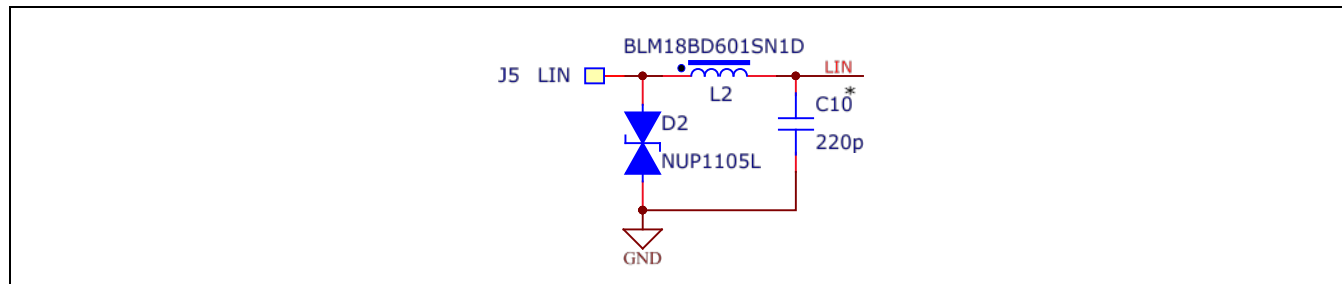


2.2. Local Interconnect Network (LIN)

The kit's LIN interface allows bidirectional communication with the ZAMC4100.

* The value shown in Figure 2.2 for C10 is the maximum value specified by the LIN 2.2/SAE J2602-2 standard. The actual value is application-specific since the LIN bus capacitance depends on cable length and number of LIN nodes.

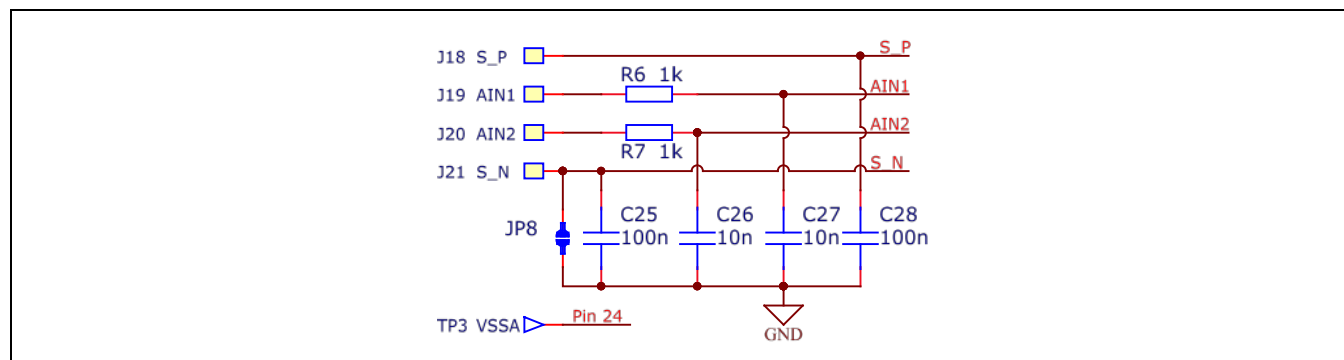
Figure 2.2 ZAMC4100 Application Kit – LIN



2.3. Position Sensing

The ZAMC4100 controller provides power supplies (S_P and S_N) for external potentiometers. They are used for sensing the mirror position signals: AIN1 and AIN2. Test point TP3 is a reference ground point.

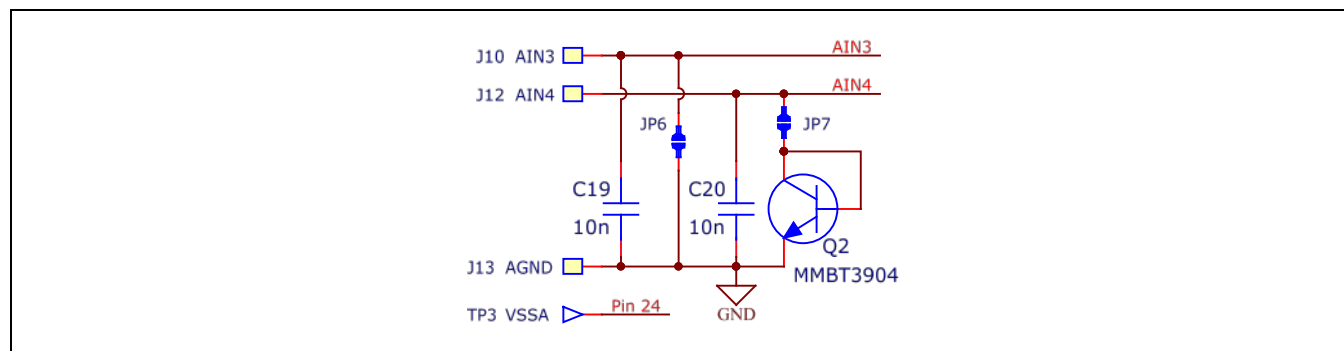
Figure 2.3 Application Kit – Position Sense



2.4. External Temperature Measurement

Analog inputs AIN3 and AIN4 allow connections to external sensors. The onboard temperature sensor Q2 can be connected to AIN4 if JP7 is closed. If AIN3 is not used, use a jumper on JP6 to ground the AIN3 pin to improve EMC. TP3 is a reference ground point.

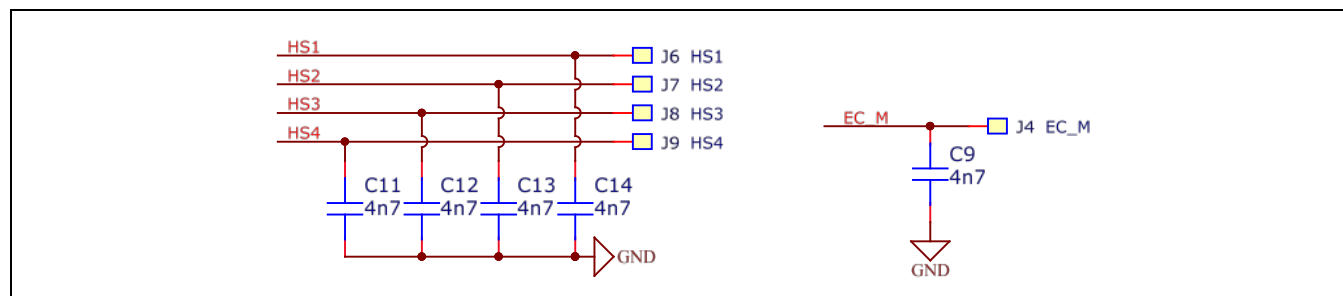
Figure 2.4 ZAMC4100 Application Kit – Analog Inputs



2.5. High-Side Drives (HS1-HS4), ECM

There are four high-side drivers that allow control of external loads. Contemporary vehicle-side mirror modules offer features that can be managed with these drivers, including heater (anti-fog feature), paddle lamps, blind-spot indication, and electrochromatic (ECM) glass.

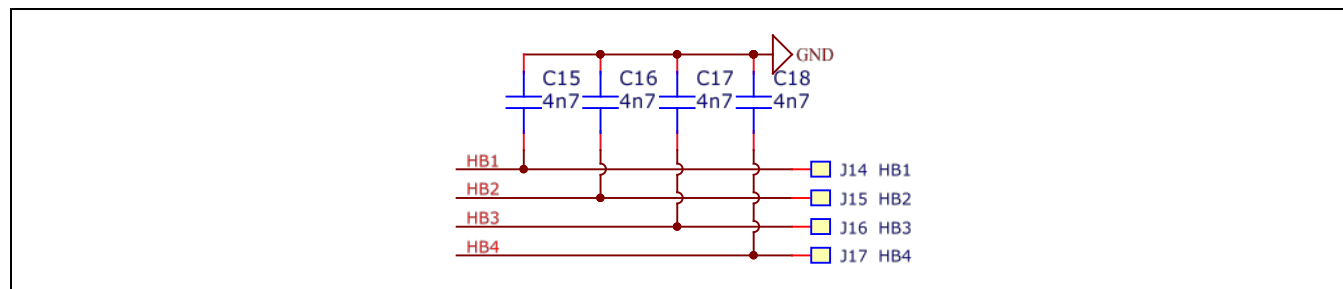
Figure 2.5 ZAMC4100 Application Kit – High-Side Drivers



2.6. Half-Bridge Drives (HB1-HB4)

Four half-bridge drivers allow control of three DC motors typically used for control of X/Y position and folding/unfolding of a mirror.

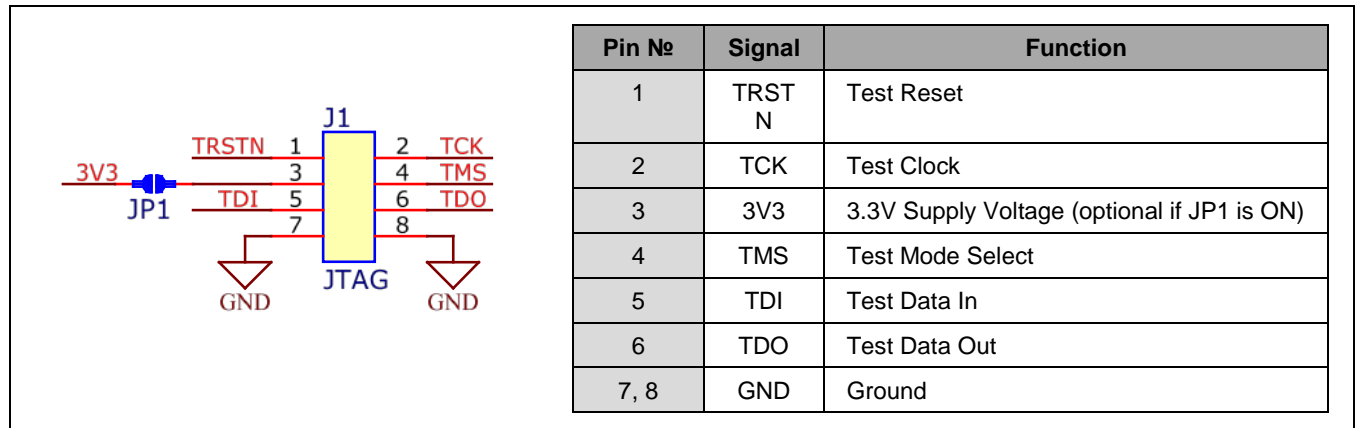
Figure 2.6 ZAMC4100 Application Kit – Half-Bridge Drivers



2.7. JTAG Connector (J1)

The ZAMC4100 offers a JTAG interface for programming and debugging. All the JTAG signals have weak pull-up resistors on board (100kΩ). The pin descriptions for the dedicated connector (J1) and signal explanations are given in Figure 2.7.

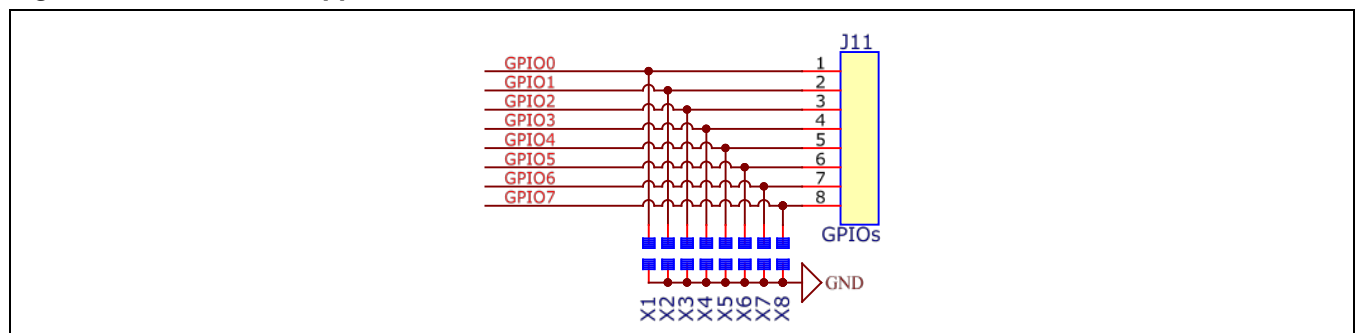
Figure 2.7 ZAMC4100 Application Kit – JTAG Interface



2.8. General Purpose Input / Outputs (GPIO 0 to 7)

The ZAMC4100 has eight general-purpose input/outputs, which are accessible on J11. X1 to X8 are provisional footprints, which can be used to fit external components depending on the application.

Figure 2.8 ZAMC4100 Application Kit – JPIOs



3 Application Design Guidelines

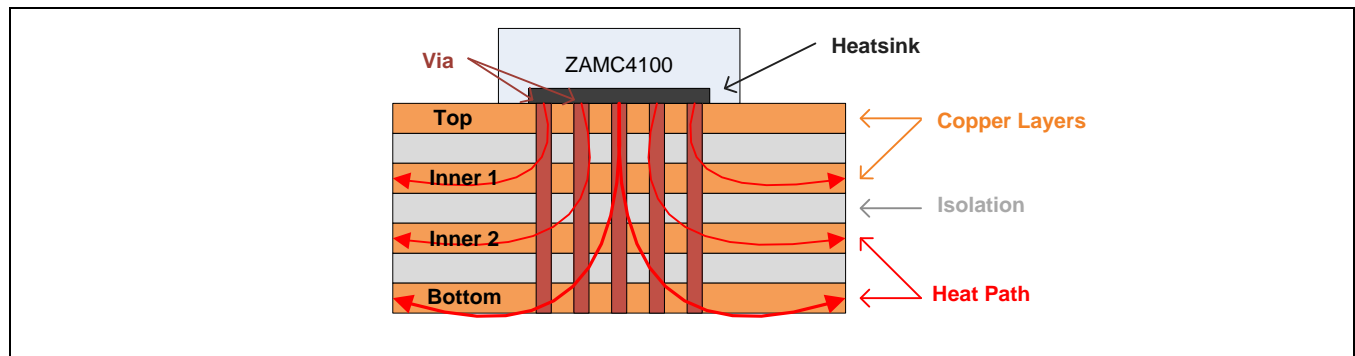
This chapter provides recommended design rules for PCB layout in order to achieve optimal performance.

Layout design should ensure the following:

- Low noise analog input signals (position sensor, temperature sensor, etc.)
- Low-ohm tracks for the high current drivers
- Heat dissipation for the power components
- Electromagnetic compatibility (EMC)
- Compact design

These requirements are fulfilled by using a four-layer PCB structure as shown in Figure 3.1.

Figure 3.1 ZAMC4100 Application Kit – PCB Structure



The main layer functions are the following:

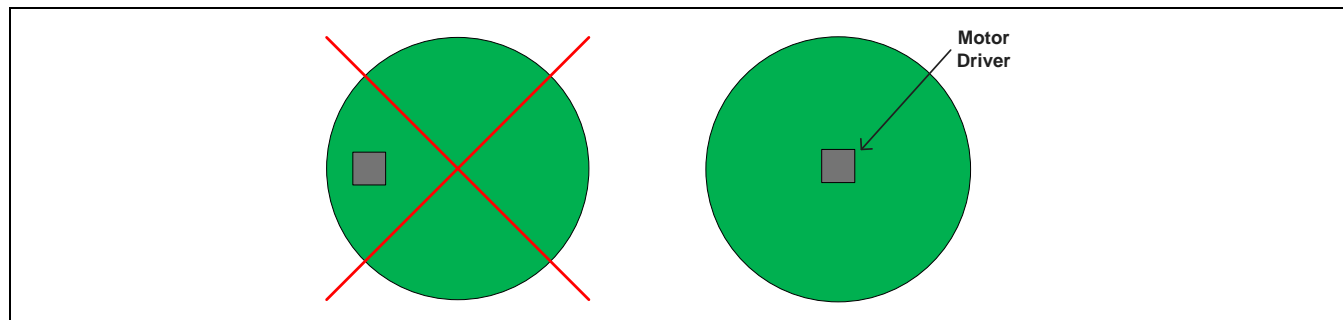
- **Top:** components, power supply traces, local heat-sinks
- **Inner 1:** heat sink, electrical shield between signal traces
- **Inner 2:** signal layer, heat sink
- **Bottom:** heat sink, electrical shield

Electroless nickel immersion gold (ENIG) finish is recommended for the bottom layer and no solder mask. Each copper layer should be at least 2oz (70μm) thick.

When designing a motor driver application board, the following rules are recommended:

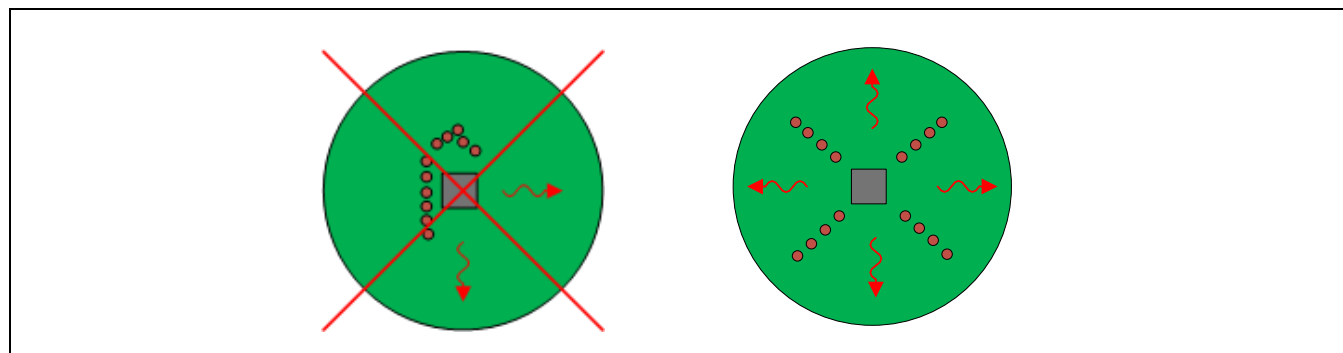
1. The main power is dissipated by the ZAMC4100. It should be placed in the center of the PCB as shown in Figure 3.2.

Figure 3.2 Motor Driver Position



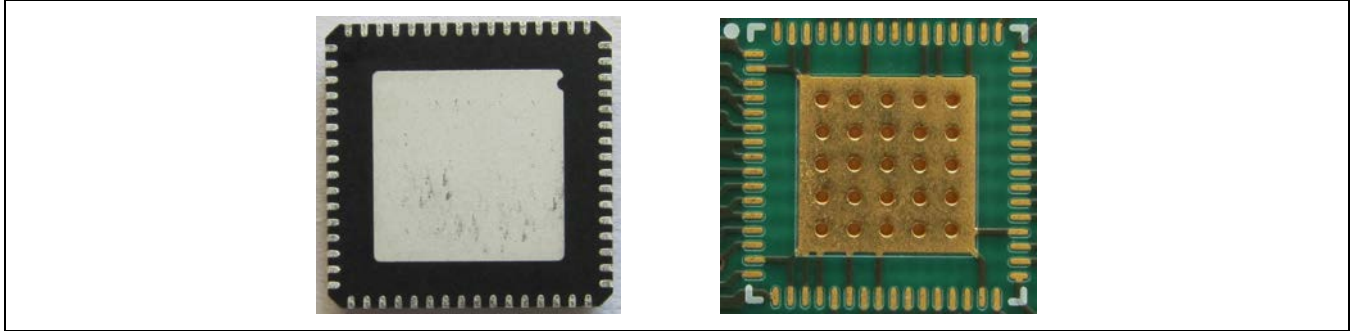
2. Signal vias can block temperature dissipation in all layers if improperly placed and close to each other. Heat dissipation should be from the motor driver to the board periphery as shown in Figure 3.3.

Figure 3.3 Signal Vias Placement



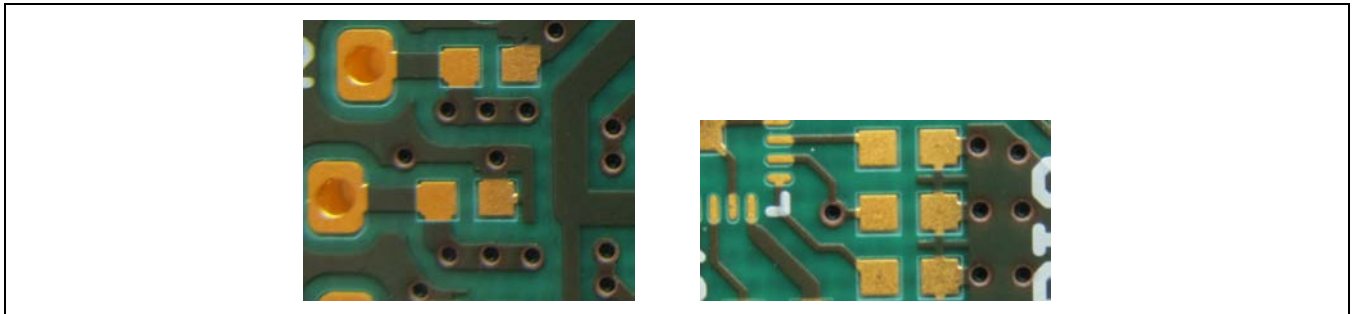
3. Power dissipated in QFN package should be led away through the thermal pad. The footprint should contain a pad with vias grid as shown in Figure 3.5.

Figure 3.4 Component Package and Recommended Footprint



4. Avoid layer changes for power supply tracks (i.e., route on top layer only).
5. When a high current track switches to an internal layer, its width should be doubled. This will compensate for the temperature increase of the tracks due to power dissipation.
6. Vias increase the line resistance and impedance. Use a multi-via if a track layer is changed.
 - Use high-current traces for the drivers, which keeps the line resistance low
 - Use bypass capacitors, which keeps the equivalent impedance low

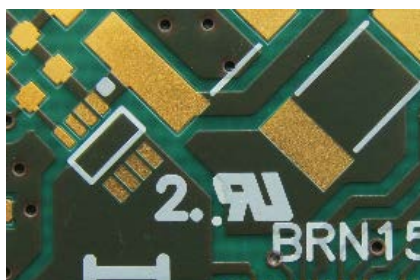
Figure 3.5 Multi-via Connections



7. Place stitching vias with a direct connection to copper pours (no thermal relief) in order to achieve
 - Level ground potentials, which prevents current ground loops on the board
 - Level PCB temperature among different layers

8. Use PCB copper areas as local heat sinks for components where needed. Components' pads should have a direct connection to the copper pour (no thermal relief) to retain high temperature conductance, as shown in Figure 3.6.

Figure 3.6 Local Heat-Sinks



9. Using thin input and sense signals tracks is recommended for low capacitance and better EMI immunity. However, due to the double copper layer thickness (70μm) keep these tracks at least 0.2mm (8 mil) wide.
10. The bypass capacitors should be placed as close to the ZAMC4100 as possible. This improves the board EMC.
11. Connectors should be placed at the board periphery.
12. Through-hole pads for soldering wires should be used. This improves both electrical and mechanical connections.
13. Multi-layer ceramic capacitors X7R and COG/NPO are recommended.

4 Related Documents

Document
ZAMC4100 Actuator and Motor Controller Data Sheet
ZAMC4100 Evaluation Kit Description

Visit the ZAMC4100 product page www.IDT.com/ZAMC4100 or contact your nearest sales office for the latest version of these documents.

5 Glossary

Term	Description
ASIC	Application Specific Integrated Circuit
ASSP	Application Specific Standard Product
LIN	Local Interconnect Network
ECM	Electrochromatic Mirror
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ENIG	Electroless Nickel Immersion Gold
PCB	Printed Circuit Board

6 Document Revision History

Revision	Date	Description
1.00	May 11, 2015	First release of document.
	April 12, 2016	Changed to IDT branding.

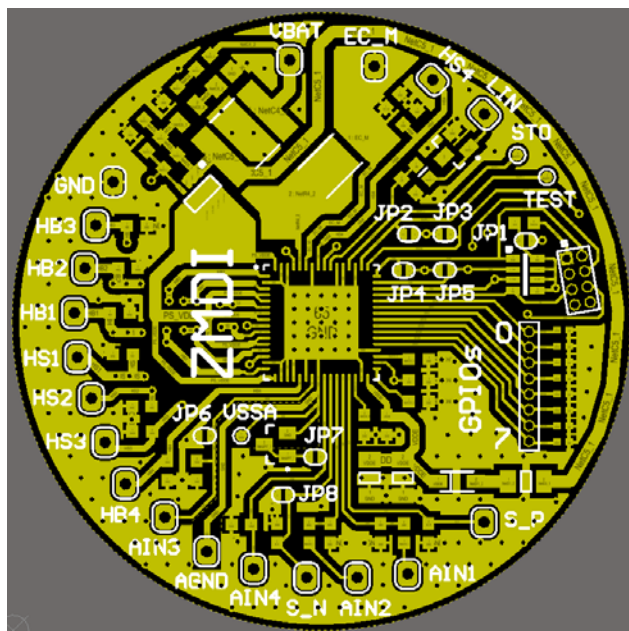
Appendix B: Bill of Materials

Table 6.1 Bill of Materials

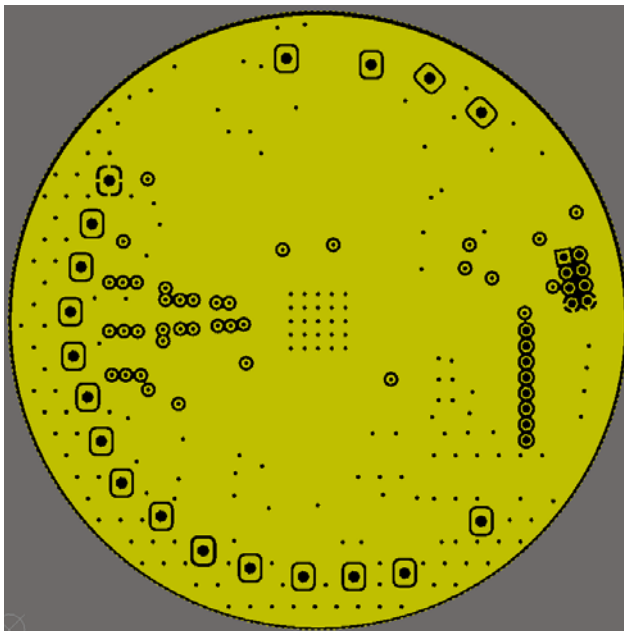
Nº	Designator	Component Description	Package	Manufacturer	Part Number	Quantity
1	C1, C25, C28	Cap 100nF 50V X7R	0603	Multicomp	MC0603B104K500CT	3
2	C2, C3	Cap 4.7µF 50V X7R	1206	Multicomp	MC1206B475K500CT	2
3	C4, C7, C19, C20, C26, C27	Cap 10nF 50V X7R	0603	Vishay	VJ0603Y103KXASW1BC	6
4	C5, C6	Cap 68nF 50V X7R	0603	TDK	CGA3E2X7R1H683K080AA	2
5	C8	Cap 330nF 50V X7R	0805	TDK	C2012X7R1H334K125AA	1
6	C9, C11, C12, C13, C14, C15, C16, C17, C18	Cap 4.7nF 50V X7R	0603	Multicomp	MC0603B472K500CT	9
7	C10	Cap 220pF 100V COG	0603	Multicomp	MC0603N221J100CT	1
8	C21, C22, C23	Cap 47nF 50V X7R	0603	TDK	CGA3E2X7R1H473K080AA	3
9	C24	Cap 220nF 50V X7R	0603	TDK	C1608X7R1H224K080AB	1
10	D1	Sch Diode 30V 200mA	SOD-123	NXP	BAT54H,115	1
11	D2	TVS LIN	SOT-23	ON Semiconductor	NUP1105LT1G	1
12	J1	Header Male 2x4 RA Gold	TH 1.27mm	FCI	20021122-0000D1LF	1
13	L1	Ferrite Bead 800R 8A	2220	Laird Technologies	HR2220V801R-10	1
14	L2	Ferrite Bead 600R 200mA	0603	Murata	BLM18BD601SN1D	1
15	Q1	N MOSFET 40V 20A 8mR@4.5Vgs	Power 33	Fairchild	FDMC8462	1
16	Q2	NPN 40V 200mA	SOT-23	NXP	MMBT3904	1
17	R1	Res 4.7R 1% 250mW	1206	WELWYN	ASC1206-4R7FT5	1
18	R2	Res 10R 1% 125mW	0805	WELWYN	ASC0805-10RFT5	1
19	R3	Res 2.2M 1% 50V	0603	WELWYN	ASC0603-2M2FT5	1
20	R4	Res 47R 1% 1W	2512	WELWYN	ASC2512-47RFT4	1
21	R5	Res 100k 1%	0603	Yageo	RC0603FR-13100KL	1
22	R6, R7	Res 1k 1% 100ppm	0603	WELWYN	ASC0603-1K0FT5	2
23	RN1	Res Matrix 4x100k	1206	Vishay	CRA06S083100KFKTR	1
24	U1	IDT Mirror Controller	QFN64 9x9mm	IDT	ZAMC4100GA	1
25	J1 - Mating	Female Connector 2x4	1.27mm	3M	45108-010030 + 3448-45108	1

Appendix C: PCB Layout

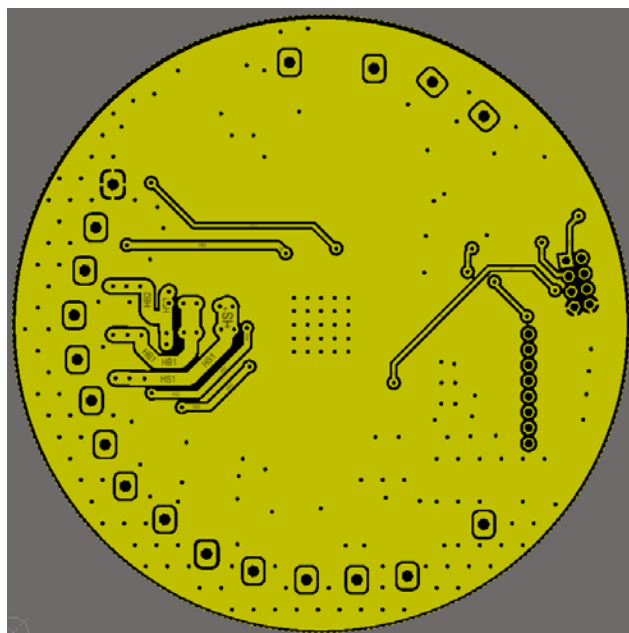
Top Layer and Service Print



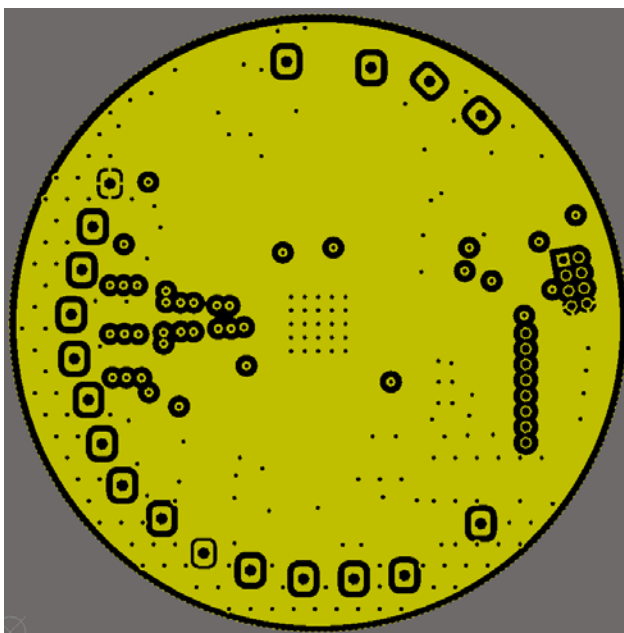
Inner Layer 1



Inner Layer 2



Bottom Layer, Top View



IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.