Restrictions:

IDT's ZSPM8015-KIT Open-Loop Evaluation Board is designed for evaluation of the ZSPM9015, laboratory setup, and module development only. The Evaluation Board must not be used for module production and production test setups.

IDT shall not be liable for any damages arising out of defects resulting from (i) delivered hardware (ii) non-observance of instructions contained in this manual, or (iii) misuse, abuse, use under abnormal conditions or alteration by anyone other than IDT. To the extent permitted by law, IDT hereby expressly disclaims and User expressly waives any and all warranties, whether express, implied, or statutory, including, without limitation, implied warranties of merchantability and of fitness for a particular purpose, statutory warranty of non-infringement and any other warranty that may arise by reason of usage of trade, custom, or course of dealing.

Important Safety Reminder: These procedures can result in high currents, which can cause severe injury or death and/or equipment damage. Only trained professional staff should connect external equipment and operate the software.

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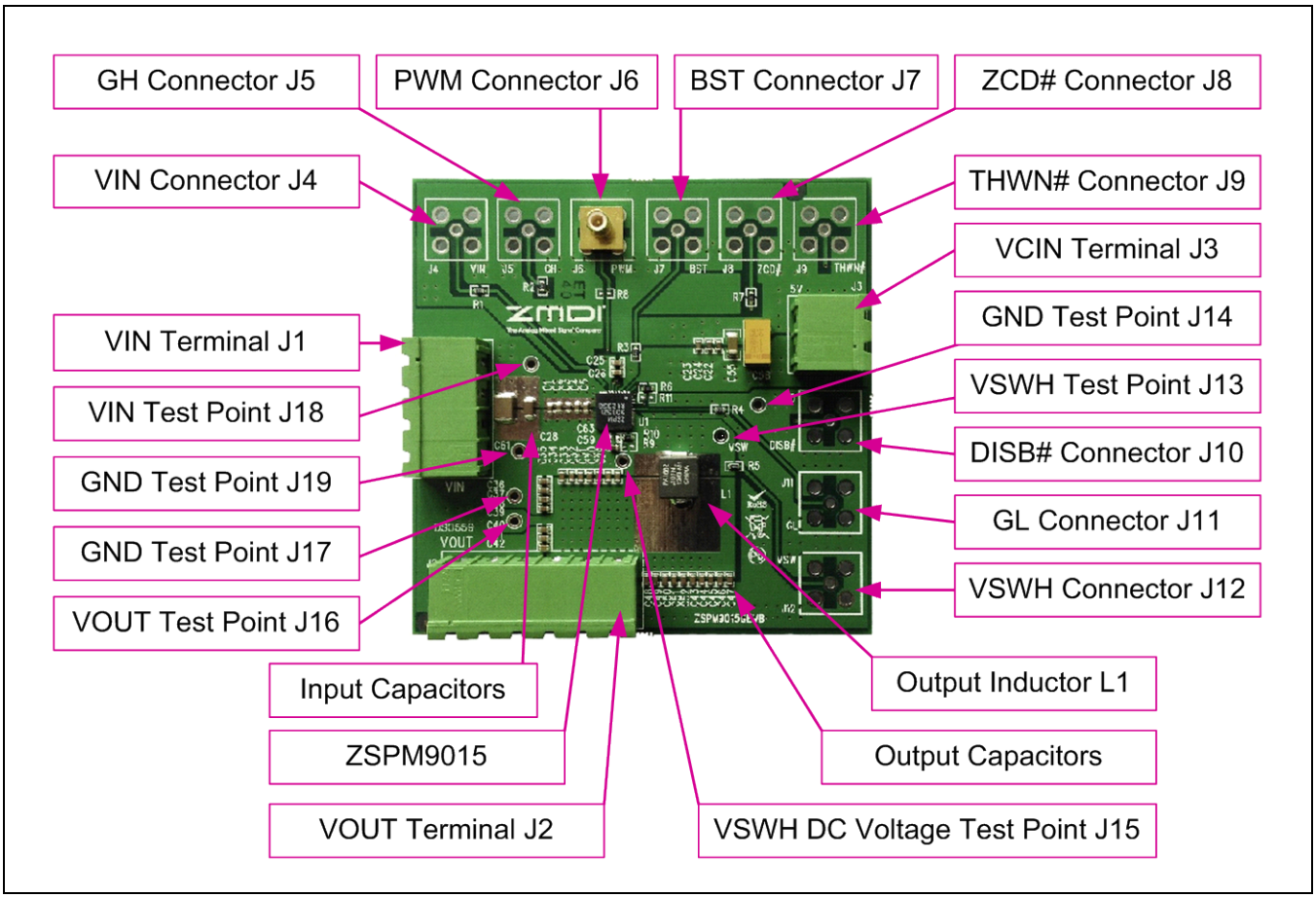
1 Introduction

1.1. ZSPM8015-KIT Open-Loop Evaluation Board Overview

The ZSPM8015-KIT single-phase open-loop evaluation board is a design platform providing the minimum circuitry needed to characterize critical performance of the ZSPM9015, a 6x6 mm DrMOS driver plus MOSFET module. The scope of this user guide includes using the ZSPM8015-KIT Evaluation Board for internal testing as a reference and for customer support. See section 3.2 for the test equipment needed for the evaluation.

This document provides details of the construction of the ZSPM8015-KIT as a guide for modifying the Evaluation Board as needed for the user's specific application.

Figure 1.1 ZSPM8015-KIT Open-Loop Evaluation Board – Top View



The ZSPM9015 DrMOS device is a fully optimized integrated driver plus MOSFET power stage solution for high-current synchronous buck DC-DC applications. The device integrates a driver IC, two power MOSFETs and a bootstrap Schottky diode in a space-saving, 6x6mm, 40-pin QFN package. This integrated approach optimizes the complete switching power stage for the driver and MOSFET in terms of dynamic performance, system inductance and the power MOSFET's on-resistance. Package parasitic and layout issues associated with conventional fully discrete solutions are greatly reduced. This integrated approach results in a significant reduction of board space, maximizing footprint power density. The ZSPM9015 solution is based on the Intel™ DrMOS 4.0 specification.

Key Features of the ZSPM9015

- Ultra-compact 6x6 mm QFN, 72% space saving compared to conventional full discrete solutions
- Fully optimized system efficiency: > 93% peak
- Clean switching waveforms with minimal ringing
- High current handling: up to 35A
- V_{IN}: 4.5V to 25V (typical 12V)
- Tri-state PWM input capable of 3.3V and 5V
- Zero-current detection and under-voltage lockout (UVLO)
- Thermal shutdown and warning flag for over-temperature conditions
- Driver output disable function (DISB# pin)
- Integrated Schottky diode technology in low side MOSFET
- Integrated bootstrap Schottky diode
- Adaptive gate drive timing for shoot-through protection
- Optimized for switching frequencies up to 1 MHz
- Based on the Intel® 4.0 DrMOS standard

2 Evaluation Board Description

The ZSPM8015-KIT Open-Loop Evaluation Board is designed to demonstrate the optimized small-size, high-efficiency performance of the ZSPM9015 DrMOS multi-chip module. The board is a high density, high-efficiency design, with a 1 MHz operating frequency and peak efficiency of over 93% with a 1.0V V_{OUT} condition. This board also demonstrates the ease of layout for printed circuit board artwork.

The board was designed as an open-loop control to have only common passive components in a synchronous buck converter without a PWM controller. The open-loop control method is more reliable and flexible, allowing performance testing with identical conditions. Since the ZSPM9015 pin map is industry standard, it is easy to compare its performance to other DrMOS devices without changing other components.

See Appendix B for the schematic for the Evaluation Board. See Appendix A for the Evaluation Board's physical specifications and layouts for the individual layers of the circuit board.

Table 2.1 ZSPM8015-KIT Open-Loop Evaluation Board Electrical Specifications

Parameter	Description	Notes
Switching Device	ZSPM9015	
PWM Control	0~100% duty by pulse generator	Open-loop control
VIN for Main DC/DC	12V DC typical (25V max)	Set by power supply 1
VCIN for Gate Driver Vcc	5V DC typical	Set by power supply 2
V_{OUT}	PWM duty cycle	Set by pulse generator
f_{SW}	PWM switching frequency	Set by pulse generator
Maximum I_{OUT}	Maximum current handled by the ZSPM9015 (see ZSPM9015 data sheet for details)	Set by electronic load

Table 2.2 ZSPM8015-KIT Open-Loop Evaluation Board Test Point Descriptions

Test Point	Test Point Name	Notes
J4	VIN	Connector for VIN test point
J5	GH	Connector for GH test point (pin 6 on the ZSPM9015)
J7	BST	Connector for boot-strap test point (BOOT pin 4 on the ZSPM9015)
J9	THWN#	Connector for THWN# test point (pin 38 on the ZSPM9015)
J11	GL	Connector for GL test point (pin 36 on the ZSPM9015)
J12	VSWH	Connector for VSWH test point (pins 15, 29 to 35, and pad 43 on the ZSPM9015)

Test Point	Test Point Name	Notes
J13 – J14	VSWH - GND	Differential measurement pair
J15	VSWH DC Voltage	Filtered VSWH pin voltage for efficiency measurements
J16 – J17	VOUT - GND	Differential measurement pair
J18 – J19	VIN - GND	Differential measurement pair

Table 2.3 ZSPM8015-KIT Open-Loop Evaluation Board Connection Point Descriptions

Test Point	Test Point Name	Notes
J1-3, J1-4	VIN	VIN supply (pins 9 to 14, and pad 42 on the ZSPM9015)
J1-1, J1-2	PGND (VIN)	Ground connection point (relative to VIN)
J2-1, J2-2, J2-3	VOUT	VOUT connection
J2-4, J2-5, J2-6	PGND (VOUT)	Ground connection point (relative to VOUT)
J3-1	GND (VCIN)	Ground connection point (relative to VCIN)
J3-2	VCIN	VCIN test point (pin 2 on the ZSPM9015)
J6	PWM	PWM drive logic (pin 40 on the ZSPM9015)
J8	ZCD#	ZCD# enable point (ZCD_EN# pin 1 on the ZSPM9015)
J10	DISB#	DISB# test point (pin 39 on the ZSPM9015)

3 Test Setup and Procedure

3.1. Output Inductor

The output inductor fitted on the ZSPM8015 Evaluation Board has been selected for 1MHz operation. If the board is operated at a lower frequency, the inductor value should be increased accordingly to suit test conditions.

Table 3.1 Inductor Value vs. Switching Frequency for VIN up to 25V

Switching Frequency	Minimum Inductor Values
300kHz	360nH
500kHZ	220nH
1MHZ	100nH

3.2. Test Setup

The following equipment is recommended for the using the Evaluation Board to test/evaluate the ZSPM9015.

Efficiency Measurements:

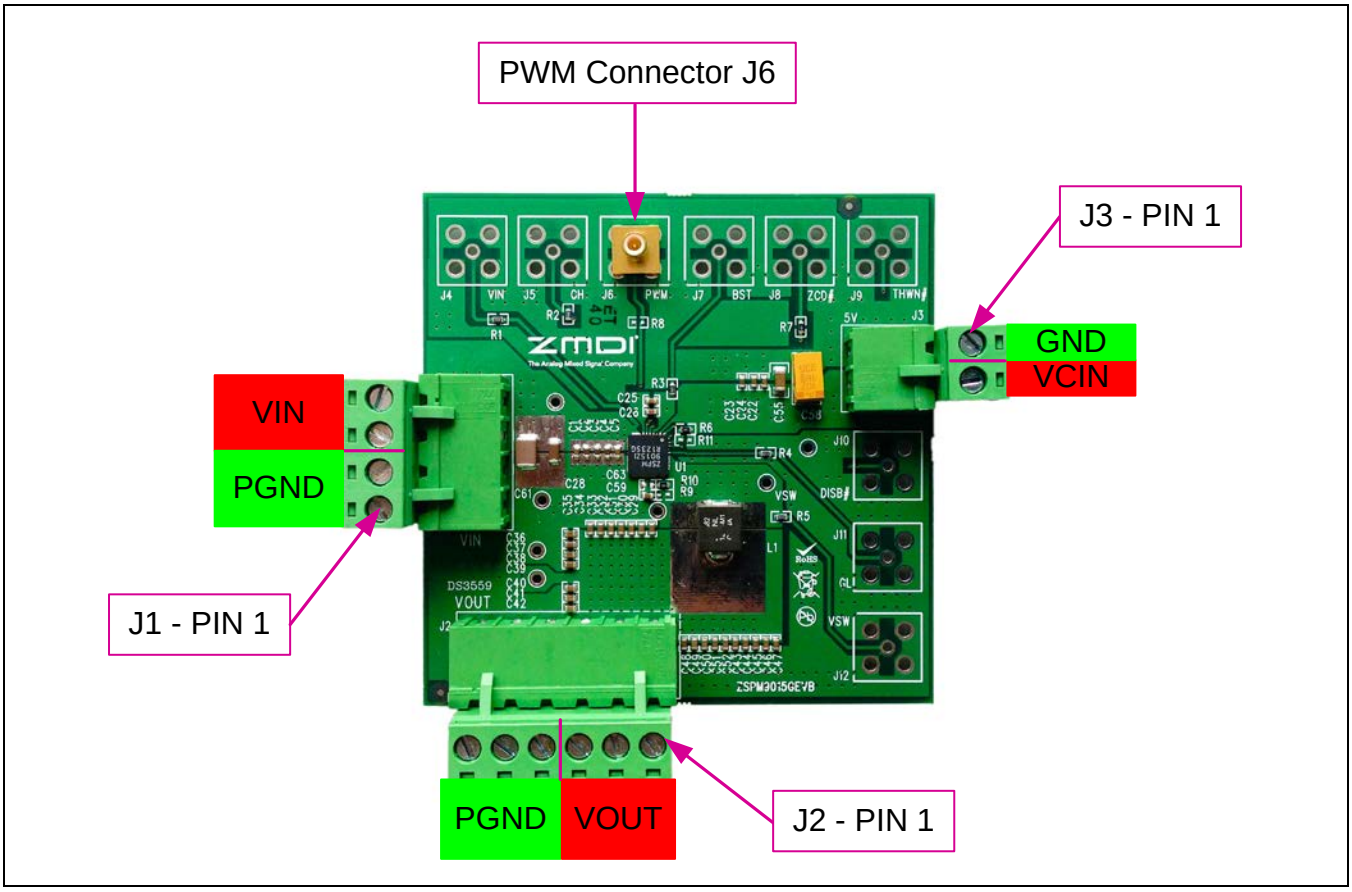
- Power supply 1 for VIN and I_{IN} rated for at least 20V / 10A.
- Power supply 2 for VCIN; rated for at least 10V / 1A.
- Pulse generator for PWM pulse signaling.
- Electronic load rated for 3V / 40A.
- Precise voltmeter to measure input and output voltage.
- Precise current sense resistors in series with each power rail to measure input and output currents. See Table 3.3 for recommended values.
  Recommendation: For efficiency measurements, use precise current sense resistors in series with the input and output power rails. Some vendors offer high-current, high-precision shunt resistors that perform well in this application. They are designed and calibrated at the factory to have a standard accuracy of ±0.25 %.

Waveform Measurements:

- Power supply 1 for VIN and I_{IN}; rated for at least 20V / 10A.
- Power supply 2 for VCIN; rated for at least 10V / 5A.
- Pulse generator for PWM pulse signaling.
- Electronic load; rated for 3 V / 60 A.
- Precise voltmeter to measure input and output voltage.
- Four-channel oscilloscope; bandwidth (BW) of at least 1GHz.
- For measuring fast-switching waveforms such as VSWH, an active differential probe provides the best accuracy. It should be rated for at least 25V differential input and a BW of at least 500MHz. A standard single-ended probe with a BW of at least 500 MHz will also provide acceptable results.

The output cables for the board must be made with large gauge wire to ensure that they do not cause excessive heating of the board by copper loss. In a normal test setup, use two parallel audio cables with 8-gauge thickness for the maximum 35A output current. The cables maybe secured using the supplied screw terminal connectors.

Figure 3.1 ZSPM8015-KIT Open-Loop Evaluation Board – Connection Points



The board has been designed to accommodate standard SMB-type connectors but to allow flexibility for user preference, they have not been fitted except for the position of J6 (PWM input). Suggested suitable connectors are given in Table 3.2.

Table 3.2 Possible SMB Connectors

Connector Type	Description	Manufacturer	Manufacturer Part Number
SMB Connector	Straight Through, 50Ω	MOLEX	73404-2300
SMB Connector	Straight Through, 50Ω	Amphenol Connex	142138

Table 3.3 Test Equipment Used

Equipment Type	Name	Notes
Power Supply 1	Agilent E3633A	
Power Supply 2	Agilent E3633A	
Pulse Generator	Agilent 81101A	
Electronic Load	Chroma 6312/63106	High-current electronic load
Voltmeter	Agilent 34970A	Multi-channel DMM or data logger
Current Sense Resistor	Deltec	1mΩ / 20A for I_{IN} 50mΩ / 5A for I_{CIN} 0.25mΩ / 100A for I_{OUT}
Oscilloscope	Tektronix DPO7104	

3.3. Evaluation Board Setup and Evaluation Procedures

Use the following procedures when operating the ZSPM8015-KIT Open-Loop Evaluation Board. For this example setup, a PWM pulse generator is used to control V_{OUT}.

Operating Conditions

- VIN for main conversion: 12V typical
  VCIN for gate driver logic for gate driving power: 5 V typical
- V_{OUT} for output load: 1.2V typical (set by PWM duty cycle from pulse generator – approximately 100ns @ 1MHz)
- PWM pulse: 5V high and 0V low, 1MHz f_{SW}, 10% duty cycle (depending on V_{OUT})

Operating Procedures

Important: Since the ZSPM9015 does not have a specific power sequence for VIN, VCIN, DISB#, and PWM, it is possible to turn on the board with any power-up sequence. However, to get proper operation and to avoid sudden extreme conditions caused by user errors, always using the following power up sequence is recommended.

Important: During the following procedures, do not turn on the power supplies until indicated in the steps.

1. Connect the electronic load to the J2 terminals - VOUT (J2-1, J2-2, J2-3) and PGND (J2-4, J2-5 J2-6).
2. Connect power supply 1 to the J1 terminals - VIN (J1-3, J1-4) and PGND (J1-1, J1-2).
3. Connect power supply 2 to the J3 terminals – VCIN (J3-2) and GND (J3-1).
4. Connect the pulse generator to the J6 PWM connector.
5. Set the pulse generator for high and low levels (5V and 0V respectively), f_{SW} (1MHz), duty cycle (10% - 100ns)

6. Connect oscilloscope channels and probes to the desired voltage nodes; for example, CH1 PWM, CH2 GH, CH3 VSWH, and CH4 GL. SeeTable 2.2 for descriptions of the test points.

   Important: Ensure that probes for voltage measurements are in place before powering up the board in step 13 and ensure that probes do not create any unwanted shorts since the board has very thin traces and sensitive noise immunity. If a short situation occurs, the board could malfunction or be damaged.

7. Set oscilloscope channels to appropriate voltage and time divisions.
8. Set the power supply 1 output voltage and current: 12V / 10A typical.
9. Set the power supply 2 output voltage and current: 5V / 1A typical.
10. Set the electronic load operating mode and current level: CC (constant current) / 1A typical.
11. Turn on power supply 1. Check the 12V at the VIN terminal (across J1) and the VIN sense points (J18 - J19). Check that no voltage is present on the VOUT terminal (across J2) or the VOUT sense points (J16 - J17).
12. Turn on power supply 2. Check the 5V at the VCIN terminals (J3). Check that no voltage is present on the VOUT terminal (across J2) or VOUT sense points (J16 - J17).
13. Turn on the pulse generator to supply pulses to the PWM connector on board. The board will turn on and all switching waveforms will appear on the oscilloscope.
14. Check that all input and output voltages and currents show proper values; e.g., V_{IN} = 12V, V_{OUT} = 1.2V, etc. An example of the switching voltage at VSWH (f_{SW}=500kHz) is shown in Figure 4.3.
15. Apply the value needed for load current by setting the electronic load; for example, 1 to 10A for light loads, 10 to 20A for medium loads, or >30A for heavy loads.
16. Set all user-definable parameters such as VIN, ZCD#, DISB#, VCIN, f_{SW}, VOUT, and I_{OUT} as needed to test the board with various conditions.

3.4. Evaluation Board Operation and Part Description

This section describes the Evaluation Board operation and components.

3.4.1. ZCD# Operation

When the Zero Current Detection (ZCD) feature is disabled (ZCD_EN# pin is high), the ZSPM9015 will operate in the normal PWM Mode in which the synchronous buck converter works in Synchronous Mode. In this mode, the internal low-side MOSFET of the ZSPM9015 turns on and off according to the PWM signal. The power stage operates in Continuous Conduction Mode (CCM), allowing the inductor current to go negative if there are low output current values.

If the ZCD_EN# pin is set low, then the ZSPM9015 will operate in the ZCD Mode, and in this mode, the ZSPM9015 can prevent discharging of the output capacitors as the filter inductor current attempts reverse current flow. If the PWM goes high, the GH pin will go high after the non-overlap delay time. During this period, the ZCD timer is inactive and thus reset. If the PWM goes low, the GL pin will go high after the non-overlap delay time and stay high for the duration of the ZCD timer. During this period, ZCD operation is disabled. Once this timer has expired, the VSWH pin will be monitored for zero current detection and the GL pin will go low if a zero-current condition is detected.

The board is configured with ZCD operation off by default, ZCD# is pulled high via R7. For ZCD operation, pull the ZCD_EN# pin low via J8.

3.4.2. Bootstrap Capacitors C25 and C26

Positions for two bootstrap capacitors are located on the top side of the board. The typical value for these ceramic bootstrap capacitors on the BOOT pin is 100nF / 50V / 0603 / X5R or better in terms of physical size and temperature characteristic. On the ZSPM9015 board, C25 and C26 have been populated with 100nF capacitors.

3.4.3. Pull-up Resistor R7 from ZCD_EN# Pin to VCIN Pin

The R7 pull-up resistor is located on the top side of the Evaluation Board between VCIN and the ZSPM9015's ZCD_EN# pin. This 1kΩ pull-up resistor is used on the ZCD_EN# pin to ensure the 5V HIGH level on the ZCD_EN# pin and therefore Zero Current Detection is off by default. For ZCD operation, pull the ZCD_EN# pin low via J8.

3.4.4. Pull-up Resistor R6 from DISB# Pin to VCIN Pin

The R6 pull-up resistor is located on the top side of the board between VCIN and the ZSPM9015's DISB# pin. This 1kΩ pull-up resistor is used on the DISB# pin to ensure the 5V HIGH level on the DISB# pin and therefore the ZSPM9015 is on by default. To disable the ZSPM9015, pull the DISB# pin low via J10.

3.4.5. THWN# Pin

The THWN# pin is an indicator for the over-temperature warning flag, which will go low if the temperature of the gate driver is too high. The THWN# pin is an open-drain output that can be monitored through J9. When the gate driver temperature is lower than 150°C, the THWN# pin will remain high impedance. If the gate driver temperature rises to 150°C or higher, the THWN# pin will be pulled low.

3.4.6. RC Snubber Components R9 and C63

The R9 resistor and C63 capacitor positions are located on the bottom of the board are not populated. The RC snubber for reducing VSWH pin spikes and ringing comprises R9 and C63. Their values can be calculated based on snubber theory for the operating conditions of the board. The recommended ranges of values are 0 to 3.3Ω for R9 and 0 to 2.2nF for C63.

3.4.7. RC Filter Components R10 and C59

R10 and C59 are located on the bottom side of the board. The default condition of the board is that R10=1kΩ and C59=1µF providing RC filtering for the VSWH pin voltage. The resulting filtered voltage can be measurement via J15.

This RC filter changes the VSWH AC voltage to a VSWH DC voltage that can be used to measure DC voltage on the VSWH node. This information can be used to calculate the power loss at the VSWH node. Note that some low-end voltmeters or digital multimeters cannot measure the correct DC value of the VSWH node, leading to an incorrect power loss computation and therefore an incorrect efficiency result.

4 Evaluation Board Performance

4.1. Efficiency and Power Loss Calculation

For power loss and efficiency calculations, refer to the equations below and Figure 4.1. Note: Component labels in Figure 4.1 are for a typical application and do not correspond to the Evaluation Board labels. See the schematic in Appendix B for corresponding components.

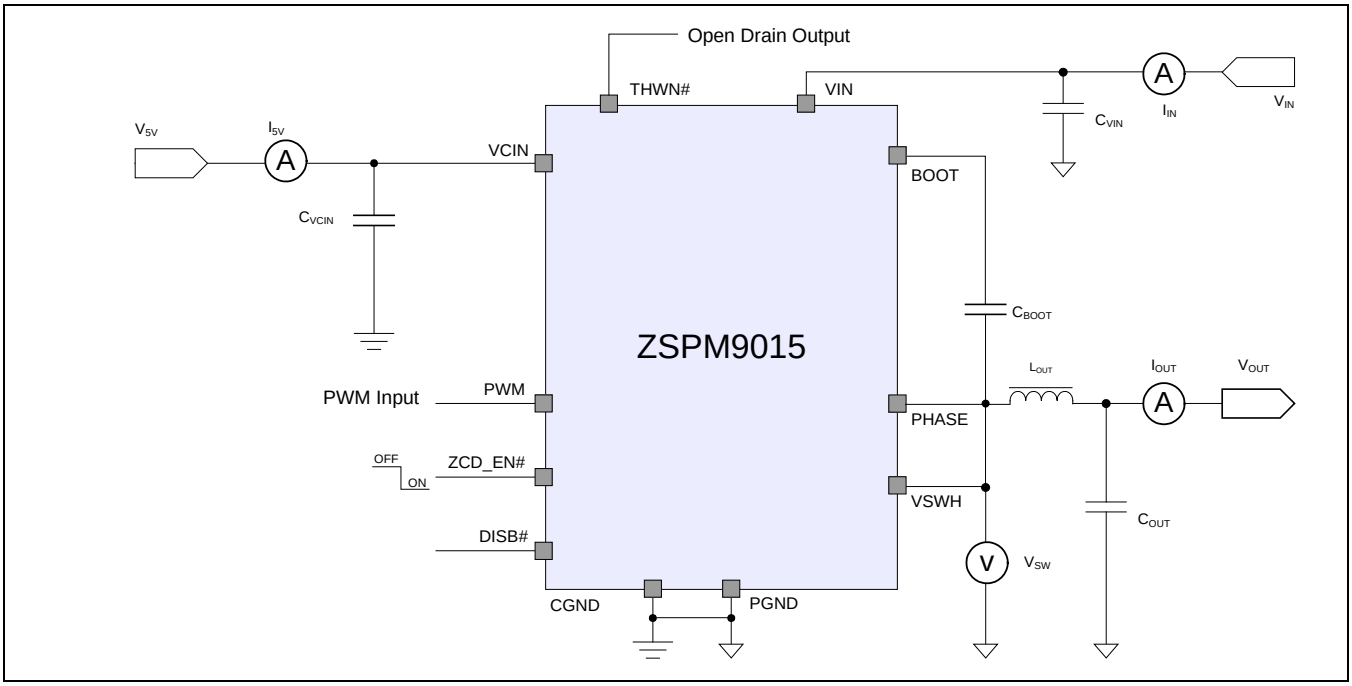
$$P_{IN\_TOT} = P_{IN} + P_{DRV} = (V_{IN} * I_{IN}) + (V_{DRV} * I_{DRV}) \quad \text{(Watts)} \tag{1}$$

$$P_{OUT} = V_{OUT} * I_{OUT} \quad \text{(Watts)} \tag{2}$$

$$P_{LOSS} = P_{IN\_TOT} - P_{OUT} \quad \text{(Watts)} \tag{3}$$

$$\text{Efficiency} = \frac{P_{OUT}}{P_{IN\_TOT}} x100\% = \frac{P_{OUT}}{(P_{IN} + P_{DVR})} x100\% \tag{4}$$

Figure 4.1 Circuit Diagram for Power Loss Measurement



4.2. Efficiency and Power Loss Measurement

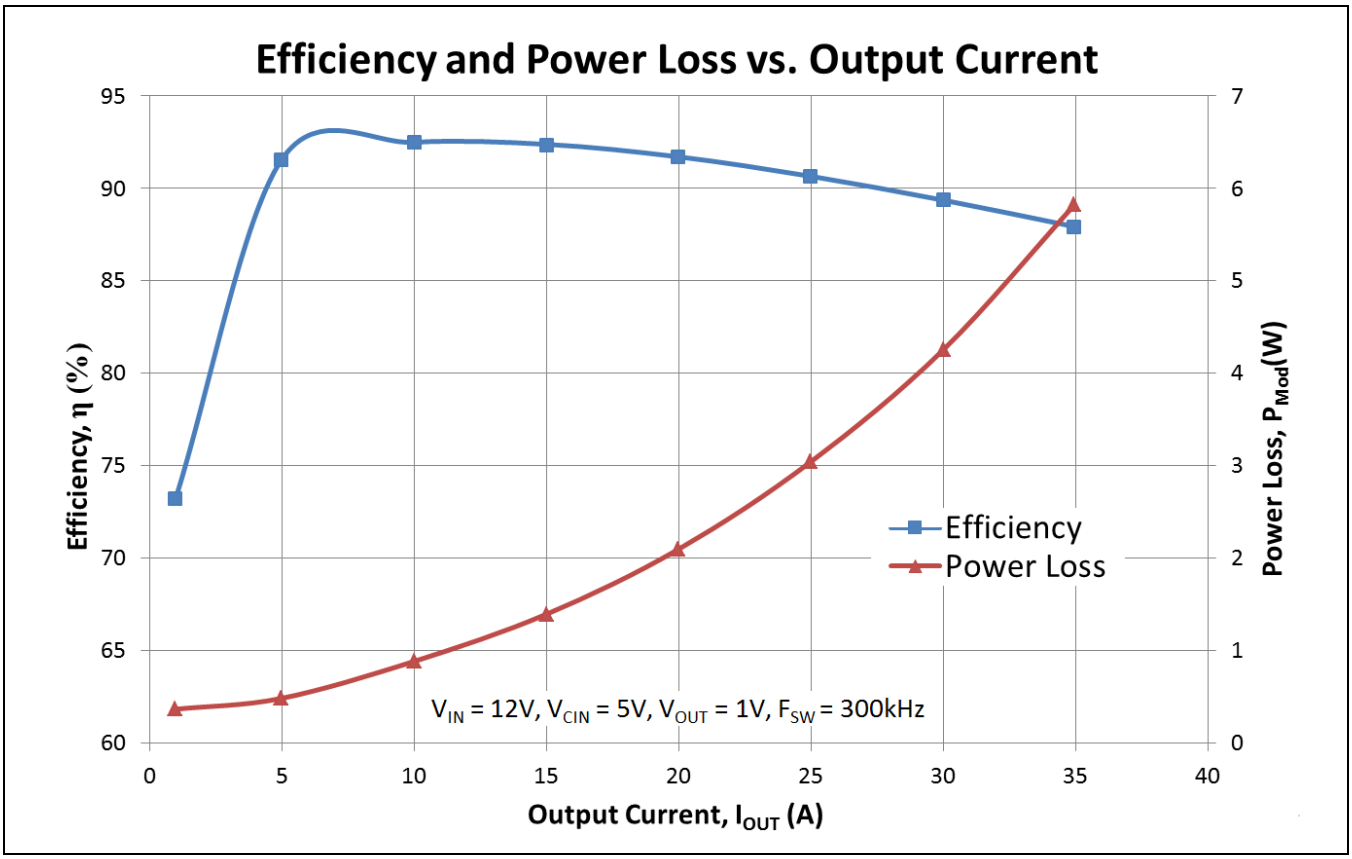
Table 4.1 shows an example of test setup parameters for efficiency and power loss measurements.

Table 4.1 Efficiency Test Conditions

VIN	VCIN	VOUT	f_{SW}	Inductor	I_{OUT}	Cooling
12V	5V	1V	300kHz	360nH	0 to 35A, 5A step, 3 minute soaking	No

Figure 4.2 shows the measured and calculated efficiency and power loss of the ZSPM8015-KIT Open-Loop Evaluation Board with the test conditions above.

Figure 4.2 Efficiency and Power Loss vs. I_{OUT}



4.3. Switching Waveform Measurements

Figure 4.3 illustrates a switching waveform example.

Figure 4.3 Switching Waveform (V_{IN}=12V, V_{OUT}=1.2V, f_{SW}=500kHz, I_{OUT}=0A)

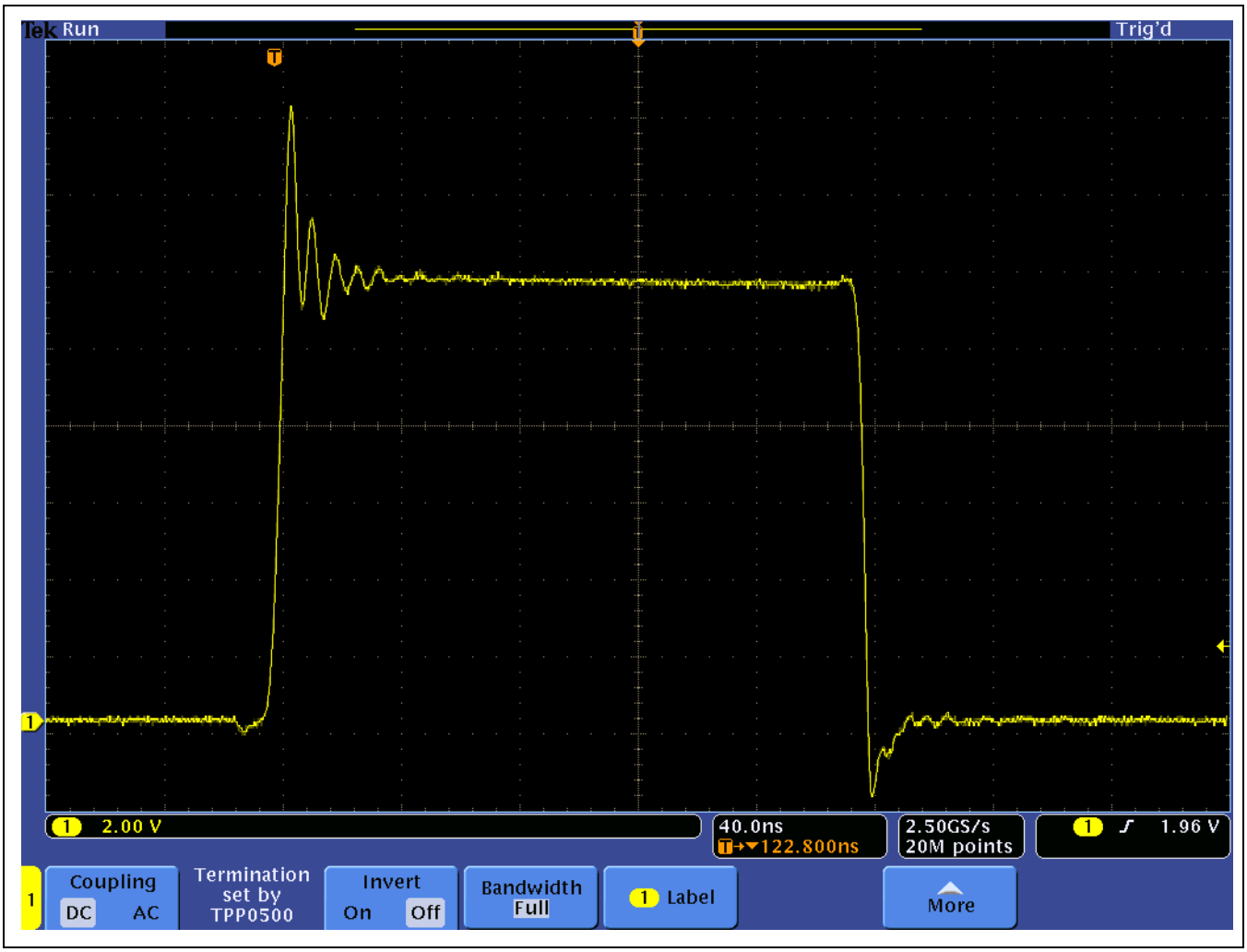
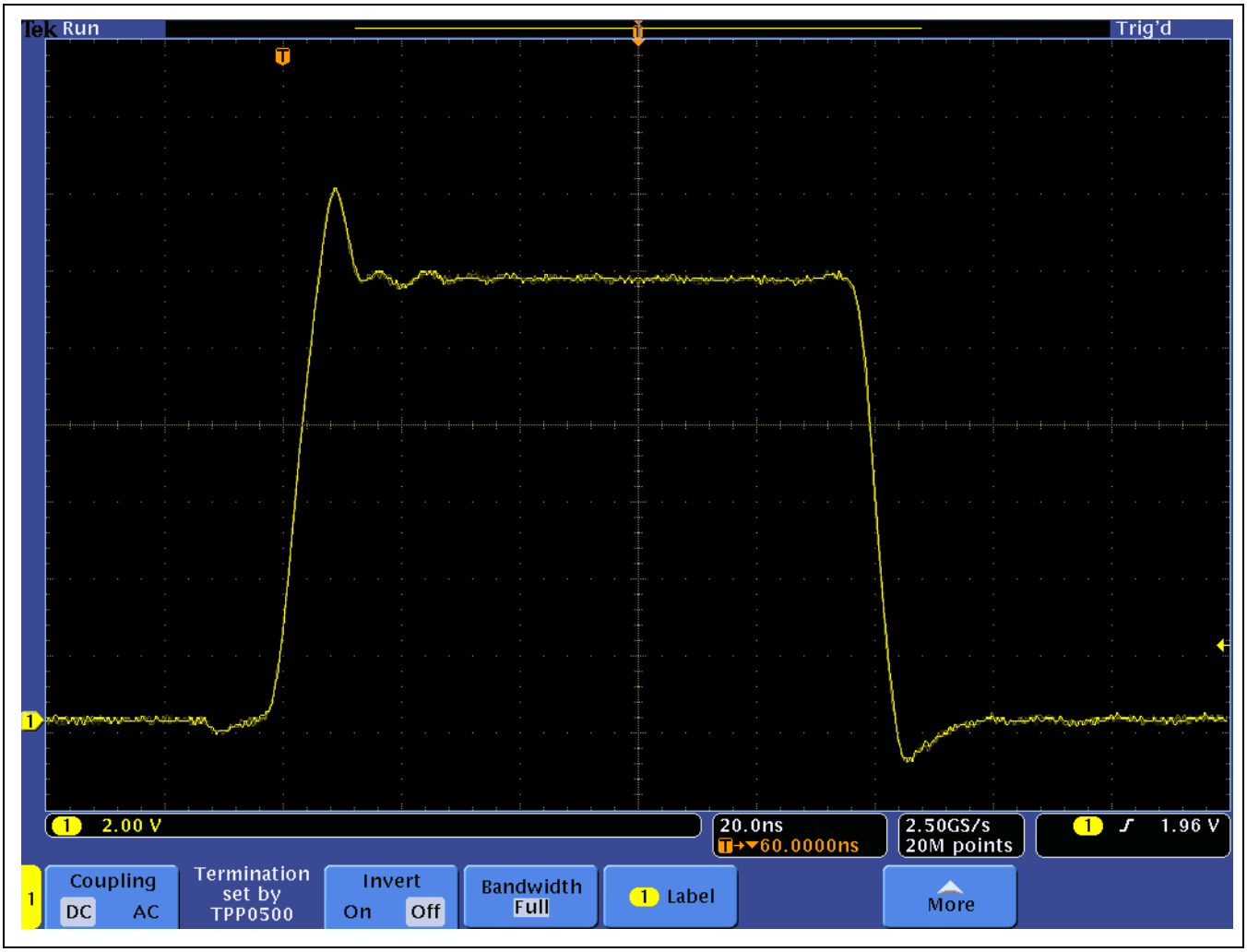


Figure 4.4 Switching Waveform (V_{IN}=12V, V_{OUT}=1.2V, F_{SW}=1MHz, I_{OUT}=0A)



5 Evaluation Board Bill of Materials

Table 5.1 shows the complete bill of materials for the ZSPM8015-KIT Open-Loop Evaluation Board. Also see the schematic given in Appendix A.

Table 5.1 Bill of Materials

Qty	Reference	Value	Size	Notes
2	C25-26	100nF, 16V, 10%	0402	MLCC, X7R
24	C29-52	10µF, 4V, 20%	0402	MLCC, X7R
20	C1-16,C22-24, C59	1µF, 25V, 10%	0402	MLCC, X7R
2	C27-28	10µF, 1206	1206	MLCC, X7R
4	C54-57	10µF, 6.3V, 1206	1206	MLCC, X7R
2	C60-61	22µF, 25V	1812	BR-113
1	C58	100µF, 16V, 20%, TANT	Case	MLCC, X7R
1	J1	TERM BLOCK HDR 4POS R/A 5.08MM		TE P/N 796638-4
1	J2	TERM BLOCK HDR 6POS R/A 5.08MM		TE P/N 796638-6
1	J3	TERM BLOCK HDR 2POS R/A 5.08MM		TE P/N 796638-2
1	L1	105 nH, 235mΩ	7 x 7.15 mm	WURTH P/N 744302010
1	U1	DRMOS	QFN40	ZSPM9015 DrMOS
5	R1-5	10Ω, 1%	0402	
3	R6-7, R10	1kΩ, 1%	0402	
1		PCB	0603	
1	J6	CONN JACK SMB STRAIGHT 50 OHMS	0603	

6 Related Documents

Documents Related to All Products
ZSPM9015 Data Sheet
ZSPM9015 Feature Sheet

Visit IDT's website www.IDT.com or contact your nearest sales office for the latest version of these documents.

7 Definitions of Acronyms

Term	Description
DISB	Driver Output Disable Function
HS	High Side
LS	Low Side
NC	No Connection
ZCD	Zero Current Detection

8 Document Revision History

Revision	Date	Description
1.00	May 22, 2013	First release.
	April 12, 2016	Changed to IDT branding.

Appendix A: ZSPM8015-KIT Physical Specifications and Layout

A.1 Evaluation Board Physical Specifications

Figure A1 shows the physical information for the individual layers of the board. The board's physical parameters are typical of values used for standard desktop and server motherboard design.

- Board size: 70 x 70 mm
- Copper layer count: 6 layer
- Board total thickness: 2.066mm
- Outer layer copper thickness: 1.5oz (0.5oz base + 1oz plating)
- Inner layer copper thickness: 1oz for IN1/IN2/IN5/IN6; 2oz for IN3 and IN4
- Via design rule: 0.25mm for drill hole, 0.4mm for pad diameter

Figure A1 ZSPM8015-KIT Open-Loop Evaluation Board Stack-up Structure

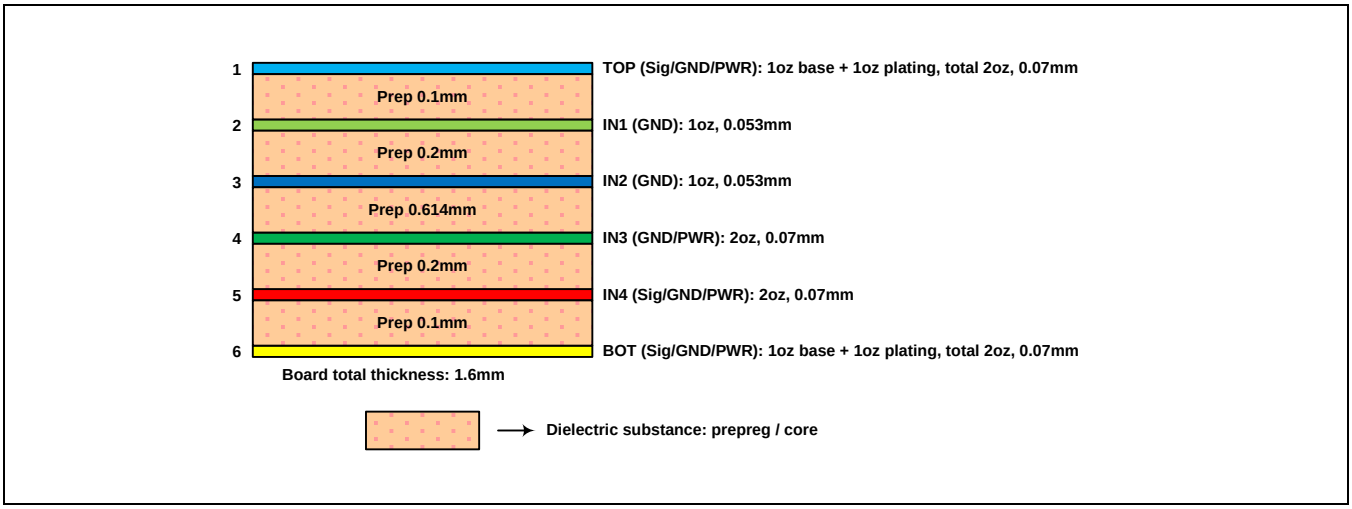
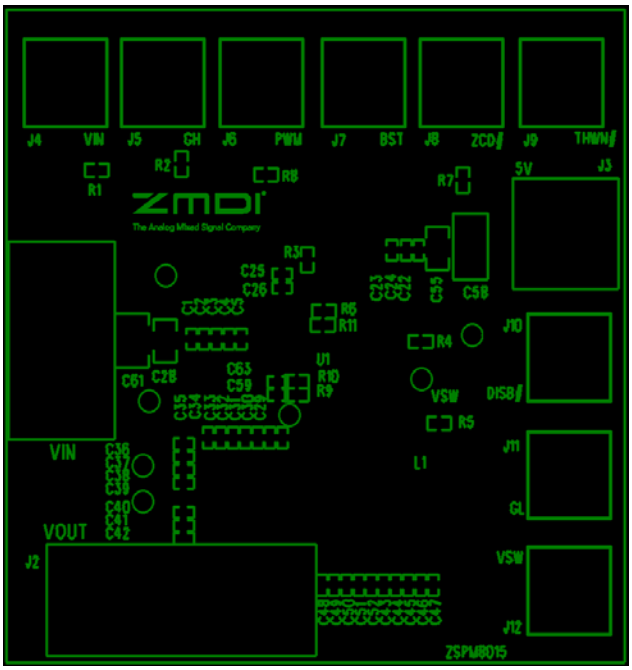
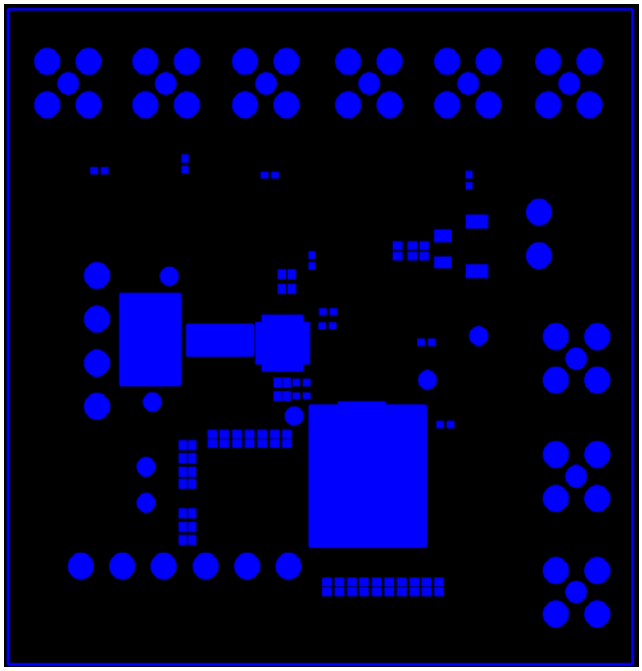


Figure A2 Evaluation Board Layout

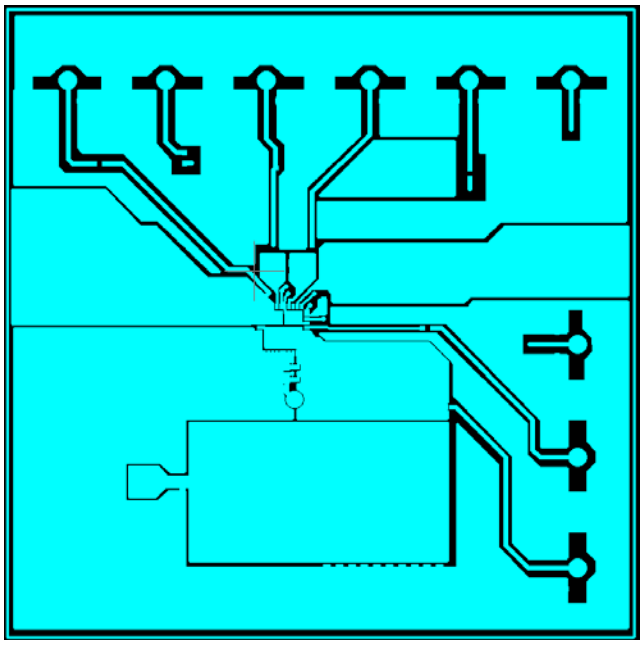
SST Layer



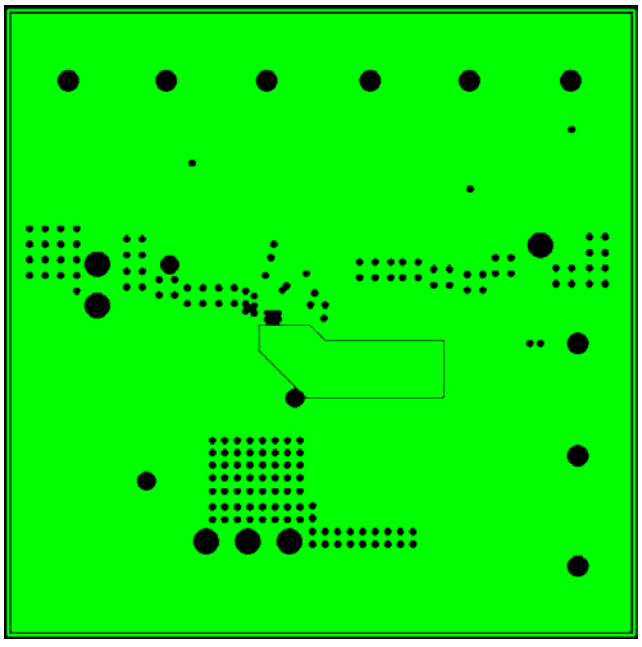
SMT Layer



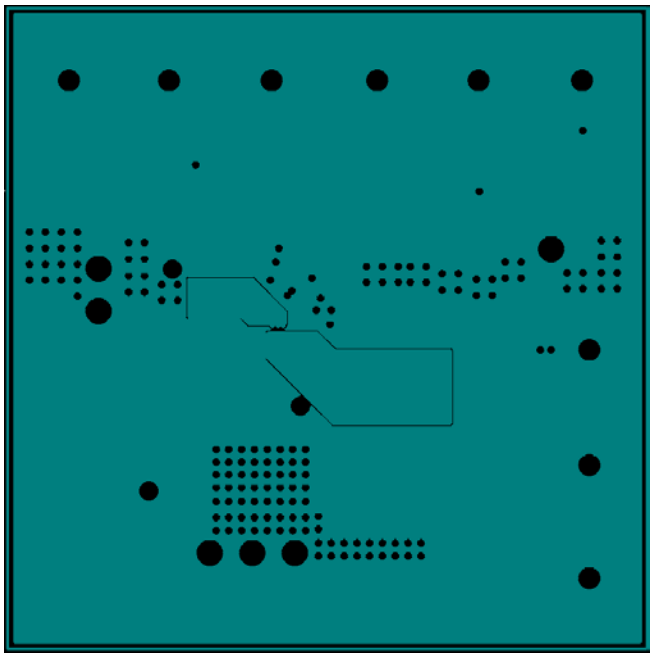
TOP Layer



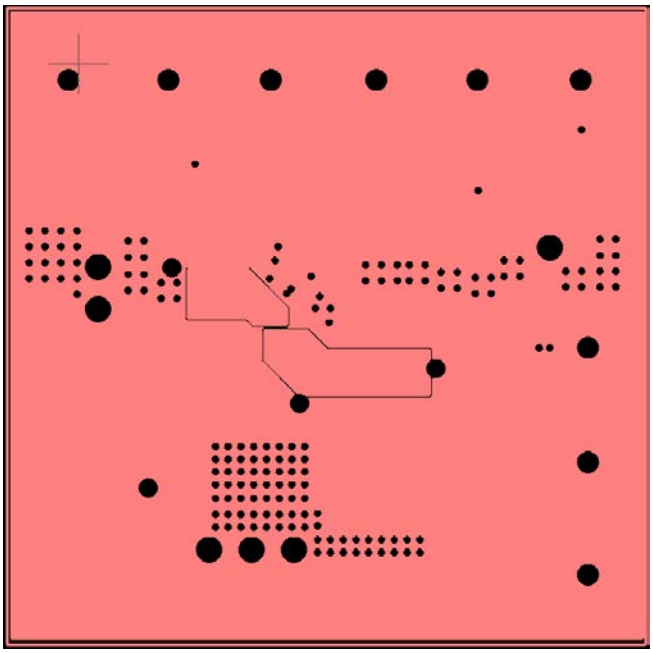
IN1 Layer



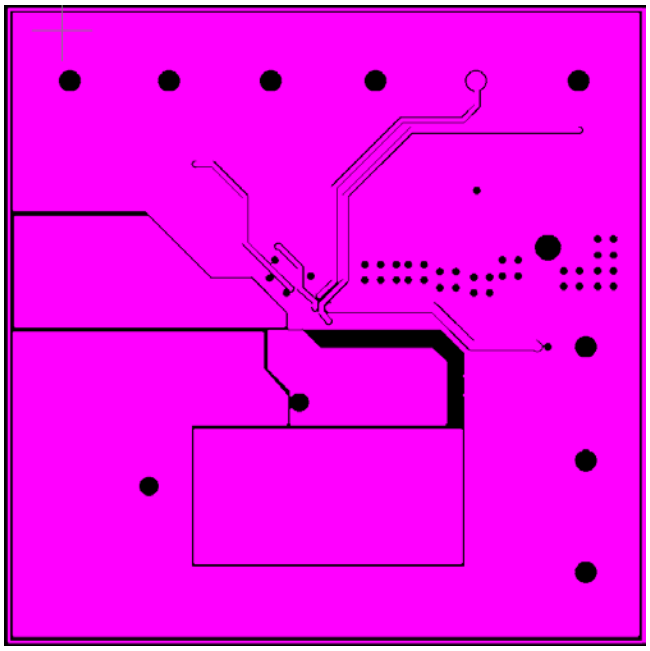
IN2 Layer



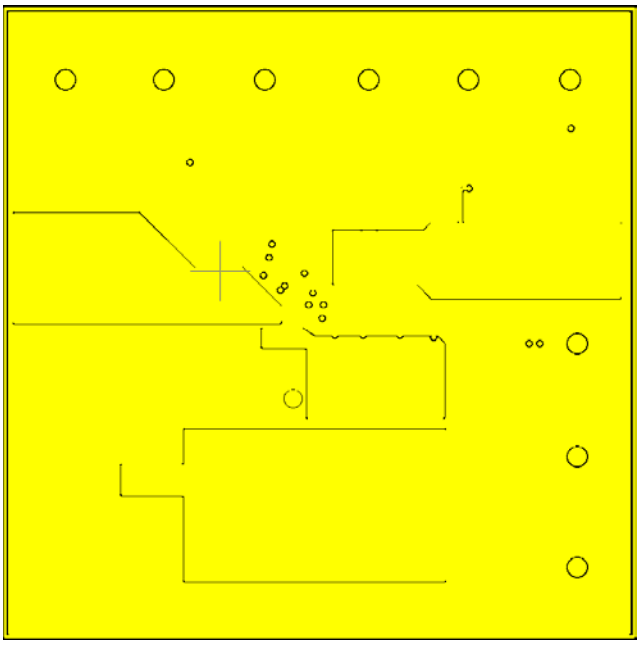
IN3 Layer



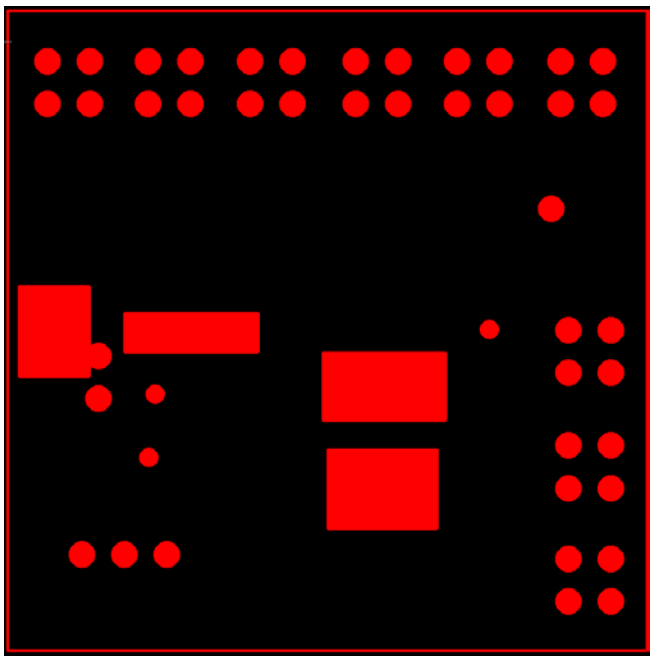
IN4 Layer



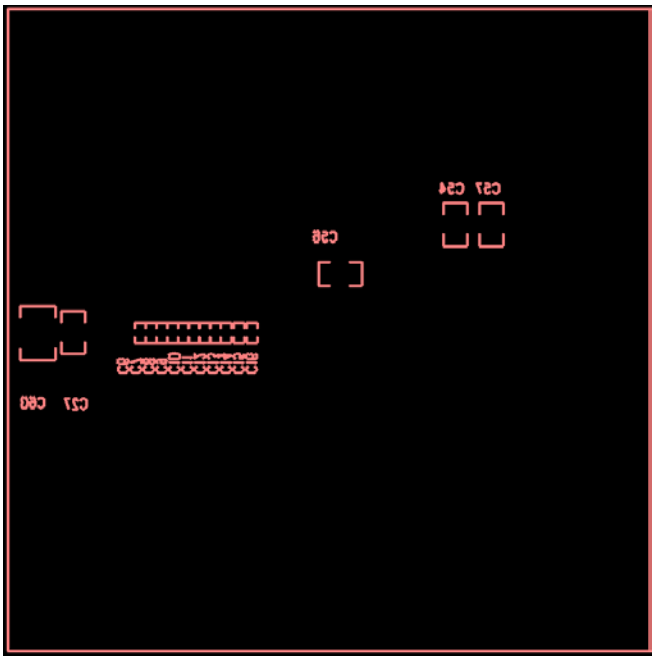
BOTTOM Layer



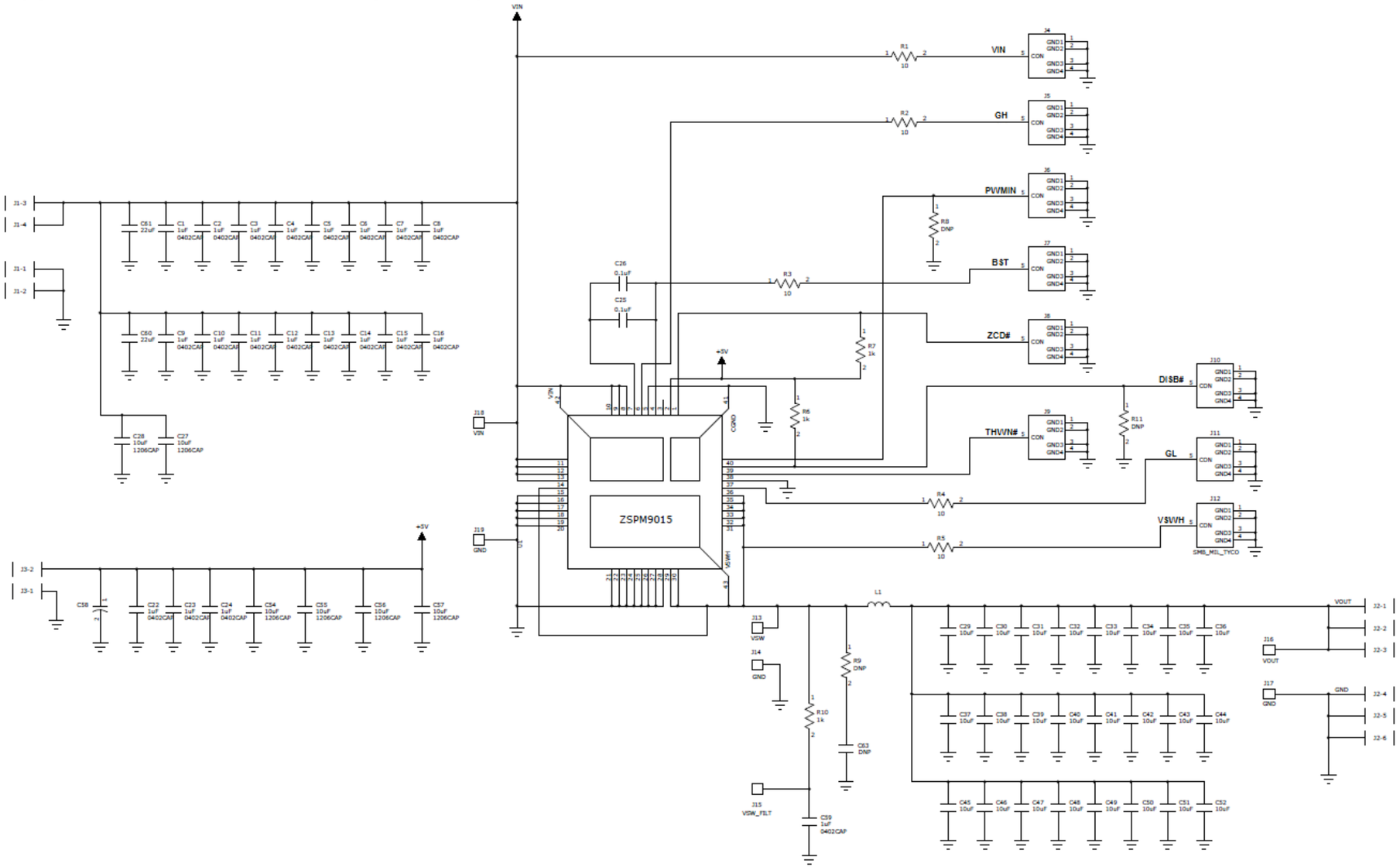
SMB Layer



SSB Layer



Appendix B: ZSPM8015-KIT Open-Loop Evaluation Board Schematic



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