

# IDT 70T3509M SYNCHRONOUS DUAL-PORT

## STATATIC RAM Test Cases List

This document defines the test cases which are together with testbench defined in [2] used to verify the functional behavior and timing of the IDT70T3509M SRAM memory VITAL model. Test environment has two main parts: Package, that generates abstract stimuli information and Test bench that interfaces directly to the model under test, driving logical stimuli and accepts its responses.

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## 1 Introduction

This document defines the test cases which are together with testbench defined in [2] used to verify the functional behavior and timing of the IDT70T3509M SRAM memory VITAL model. Test-Cases apply on SRAMmemory models listed in the Table 1.

**Table 1.** Fifo memory models

<i>Model name</i>	<i>Memory size</i>	<i>Clock Rate</i>
IDT70T3509M	1M x 36b	133 MHz

Functional behavior and timing is described in the appropriate data sheets [1].

Since these models have similar functional behavior they will be verified using the same testcases with different parameters for each specific model.

Test cases are grouped in several sequences:

- read operations
- write operations
- interrupt operations
- Sleep mode operations
- Collision situations
- Setup hold violations

Each sequence consists of series of Positive and Negative tests

## 2 Test sequences

### 2.1 Series 1 – Read from left and right ports in flow through and pipeline mode

#### 2.1.1 Positive, read from left port

**Description:** Test if read in flow through or pipeline mode returns good data on data bus.

**What is being verified:** Read on left port in every mode.

**Method of verification:** Assert CE and OE pins. With PLFTL signal control pipeline or flow through mode of read.

#### 2.1.2 Positive, Read from right port in every mode

**Description:** Test read on right port.

**What is being verified:** That read operation on right port return good data.

**Method of verification:** Assert all control signals for read operation and read from right port. With PLFTR pin control pipeline or flow through operation. Wait for 15 ns and read data from data bus.

### 2.1.3 Positive, Read from both ports at same time.

**Description:** Test read on both ports.

**What is being verified:** That read operation on both ports return good data.

**Method of verification:** Assert all control signals for read operation and read from both ports. With PLFT pins control pipeline or flow through operation. Wait for 15 ns and read data from data bus.

## 2.2 Series 2 – Positive, CNTEN pin asserted during read

### 2.2.1 Positive, Read from left port, address increment only.

**Description:** Test flow through read on left port with address increment pin asserted

**What is being verified:** Address is incremented if CNTENLNeg pin is asserted.

**Method of verification:** On first cycle do the plain read operation. On next cycle assert CNTEN pin and de assert ADSNeg. Check read data after 15 ns.

### 2.2.2 Positive, Read from right port, address increment only.

**Description:** Test flow through read on right port with address increment pin asserted

**What is being verified:** Address is incremented if CNTENRNeg pin is asserted.

**Method of verification:** On first cycle do the plain read operation. On next cycle assert CNTEN pin and de assert ADSNeg. Check read data after 15 ns.

### 2.2.3 Positive, Read from both ports, address increment only

**Description:** Test flow through read on right port with address increment pin asserted

**What is being verified:** Address is incremented if CNTENRNeg pin is asserted.

**Method of verification:** On first cycle do the plain read operation. On next cycle assert CNTEN pin and de assert ADSNeg. Check read data after 15 ns.

### 2.2.4 Positive, Read from left port, address increment only pipeline mode.

**Description:** Test pipeline read on left port with address increment pin asserted

**What is being verified:** Address is incremented if CNTENLNeg pin is asserted.

**Method of verification:** On first cycle do the plain read operation. On next cycle assert CNTEN pin and de assert ADSNeg. Check read data after 15 ns.

### 2.2.5 Positive, Read from right port, address increment only pipeline mode

**Description:** Test pipeline read on right port with address increment pin asserted

**What is being verified:** Address is incremented if CNTENRNeg pin is asserted.

**Method of verification:** On first cycle do the plain read operation. On next cycle assert CNTEN pin and de assert ADSNeg. Check read data after 15 ns.

### 2.2.6 Positive, Read from both ports, address increment only pipeline mode

**Description:** Test pipeline read on right port with address increment pin asserted

**What is being verified:** Address is incremented if CNTENRNeg pin is asserted.

**Method of verification:** On first cycle do the plain read operation. On next cycle assert CNTEN pin and de assert ADSNeg. Check read data after 15 ns.

## 2.3 Series 3 – Positive, Write operation

### 2.3.1 Positive, Write to left port

**Description:** Test write operation on left port

**What is being verified:** Writing to left port of memory

**Method of verification:** Write data on left port. Assert control signal for write. After that read written data to check for correctness of written data.

### 2.3.2 Positive, Write to right port

**Description:** Test write operation on right port

**What is being verified:** Writing to right port of memory

**Method of verification:** Write data on right port. Assert control signal for write. After that read written data to check for correctness of written data.

### 2.3.3 Positive, Write to both ports

**Description:** Test write operation on both ports simultaneously.

**What is being verified:** Writing to both ports of memory.

**Method of verification:** Write data on both ports. Assert control signal for write. After that read written data to check for correctness of written data.

## 2.4 Series 4- Positive, Interrupt flag generation

### 2.4.1 Positive, Set interrupt flag on right port

**Description:** Test interrupt flag generation

**What is being verified:** Interrupt flag generation.

**Method of verification:** Write to address FFFFE to set interrupt flag on right side.

### 2.4.2 Positive, Set interrupt flag on left port

**Description:** Test interrupt flag generation

**What is being verified:** Interrupt flag generation.

**Method of verification:** Write to address FFFFF to set interrupt flag on left side.

### 2.4.3 Positive, Reset interrupt flag on left port

**Description:** Test interrupt flag generation

**What is being verified:** Interrupt flag generation.

**Method of verification:** Read from address FFFFE to reset interrupt flag on left side.

### 2.4.4 Positive, Reset interrupt flag on right port

**Description:** Test interrupt flag generation

**What is being verified:** Interrupt flag generation.

**Method of verification:** Read from address FFFFF to reset interrupt flag on left side.

## 2.5 Series 5- Positive, Sleep Mode

### 2.5.1 Positive, Sleep Mode on left port

**Description:** Test Sleep Mode

**What is being verified:** That chip is deselected in sleep mode

**Method of verification:** Set ZZL pin and enter sleep mode. Try to read from sleep mode. Output should be HIZ.

### 2.5.2 Positive, Sleep Mode on right port

**Description:** Test Sleep Mode

**What is being verified:** That chip is deselected in sleep mode

**Method of verification:** Set ZZR pin and enter sleep mode. Try to read from sleep mode. Output should be HIZ.

## 2.6 Series 6- Positive, Collision

### 2.6.1 Positive, Write to left port and read from right on same address

**Description:** Test Collision.

**What is being verified:** Write to left port, and read on right, but on same address.

**Method of verification:** First synchronize clocks on left and right port so that skew time between them is violated. Writing on left port and reading on right from same location will result in collision. Read data should be X.

### 2.6.2 Positive, Write to same location on both ports

**Description:** Test Collision.

**What is being verified:** Write to left port, and write on right, but on same address.

**Method of verification:** First synchronize clocks on left and right port so that skew time between them is violated. Writing on left port and write on right from same location will result in collision. Written data should be X to indicate that collision.

### 2.6.3 Positive, Write to same location on both ports

**Description:** Test Collision.

**What is being verified:** Write to left port, and write on right, but on same address.

**Method of verification:** First synchronize clocks on left and right port so that skew time between them is violated. Here are swapped roles of left and right clocks. Writing on left port and write on right from same location will result in collision. Written data should be X to indicate that collision.

### 2.6.4 Positive, Write to right port and read from same location on left port

**Description:** Test Collision.

**What is being verified:** Write to right port, and read on left, but on same address.

**Method of verification:** First synchronize clocks on left and right port so that skew time between them is violated. Writing on right port and reading on left from same location will result in collision. Read data should be X.

## 2.7 Series 7- Negative, Violations

### 2.7.1 Negative, Setup violation on CE signal

**Description:** Test Violation.

**What is being verified:** Setup violation on CE signal



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**Method of verification:** Set CE signal to be near to clk signal. This will cause violation in setup checker for this signal. Warning is issued.

## References

- 1 - [1] Integrated Device Technology DSC-5682/9, MARCH 2005
- [2] idt\_dp\_testbench\_struct.odt