

致尊敬的顾客

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瑞萨电子公司网址：<http://www.renesas.com>

2010年4月1日
瑞萨电子公司

【发行】瑞萨电子公司（<http://www.renesas.com>）

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二极管

变容二极管

1. 变容二极管的特性

1.1 可变电容二极管

可变电容二极管 (Variable Capacitance Diode) 一般被称为变容二极管，它不同于利用PN结整流作用的整流二极管 / 开关二极管以及利用齐纳击穿 / 雪崩击穿的稳压二极管，而是利用反向偏压使二极管的PN结电容发生变化。

以往，可变电容二极管用于TV调谐器、FM调谐器等的AFT/AFC以及FM调制，现在，主要作为调谐器件来使用。

最近，为了能够应用于汽车导航、个人电脑、数字播放等新型传输媒介，调谐器也在不断追求超小型化及高性能化。特别是随着近年来市场的迅速扩大，多被用于以手机等为中心的移动式通信设备的VCO频率调整。

【注】[VCO: Voltage Control Oscillator (电压控制振荡器)]

1.1.1 基本工作原理

如果在PN结外加反向偏压，就会在PN结表面产生无自由电子的耗尽层，但耗尽层的宽度会根据反向偏压的大小而变化。耗尽层越宽、结电容就越小，相反耗尽层越窄、则结电容越大。总之，可变电容二极管的耗尽层宽度是根据反向偏压 V_R 来变化的，也就是说，该二极管是利用结电容变化的二极管。

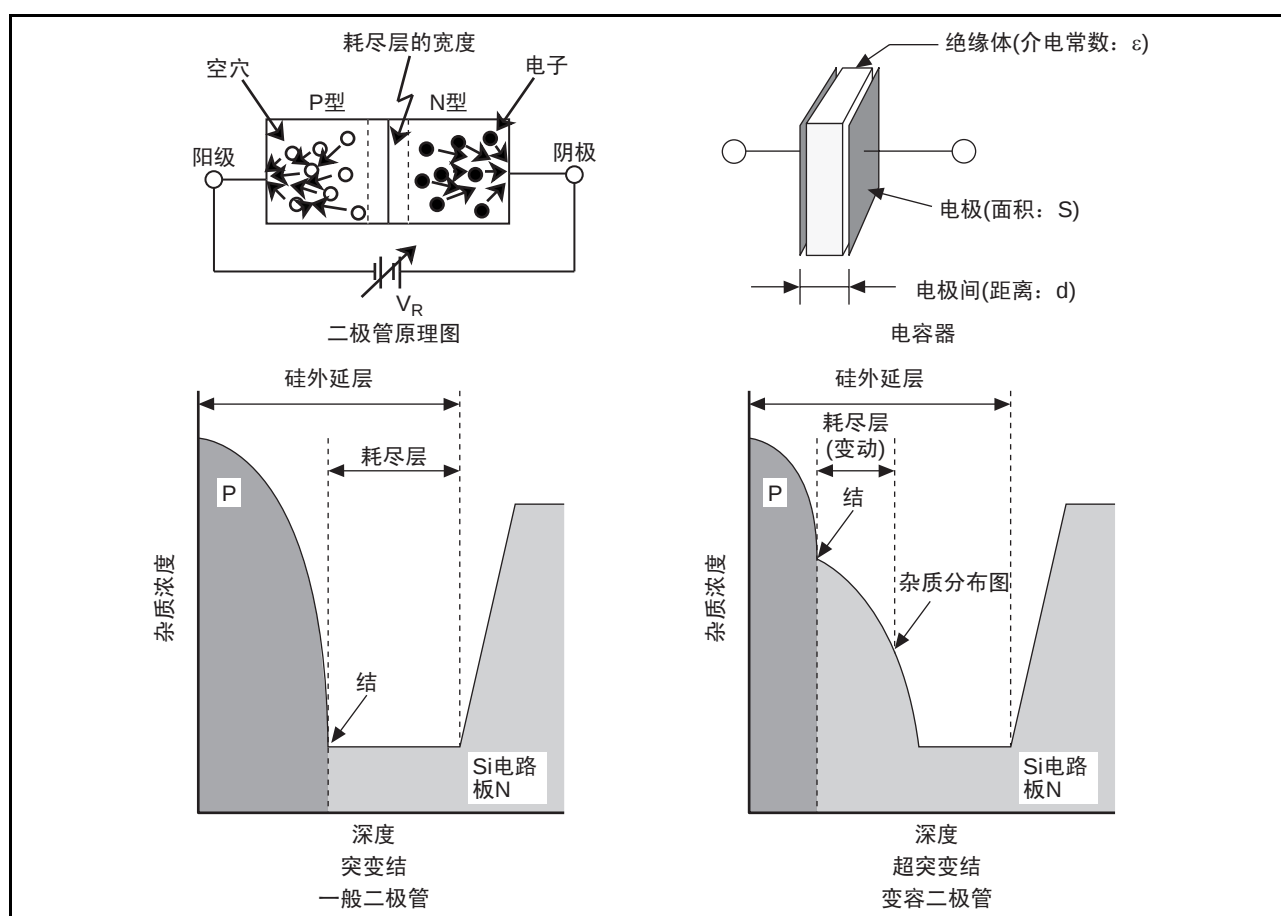


图1.1 工作说明图

如图1.1所示，电容器的电容C用下面的公式来表示。

$$C = \frac{\varepsilon \cdot S}{d}$$

S: 结面积 ε : 耗尽层的介电常数 d: 耗尽层的宽度

变容二极管中的结电容可以和电容器的电容使用相同的公式来表示。并且，电容的变化依存于图1.1中所示的杂质浓度。由于该杂质浓度是在制造工艺中产生的，因此需要采用特别的办法。

1.1.2 变容二极管的特性

二极管的反向（饱和区域）为不流入电流的区域。该区域为电容成分，可以与电容器同时使用。

变容二极管用于由本身具有的电容值(C)和线圈的电感(L)构成的调谐电路中。调谐频率(f)用下面的公式来表示：

$$f = \frac{1}{2\pi\sqrt{C \cdot L}}$$

调谐频率(f)会随着电容值(C)的变化而变化，而作为二极管的一个特点是，电容值(C)会根据外加电压发生改变。因此，通过控制二极管上的外加电压可获得所希望的调谐频率。

另外，为了满足所要求的频率以及频率范围，必须使二极管的电容值和电容变化比等具有多种变化。

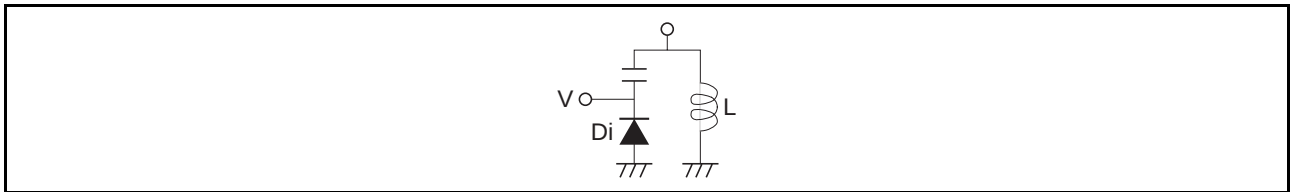


图1.2 调谐电路

1.2 C工艺

瑞萨变容二极管为了获得更适当的工艺，正在由以往的工艺（B工艺）向C工艺发展。特别是在C工艺中，由于电压—电容特性（CV特性）一致且电容变化比大，因此可以进行接收频率的宽带化。另外，串联电阻小，优化了性能指数。（图1.3）

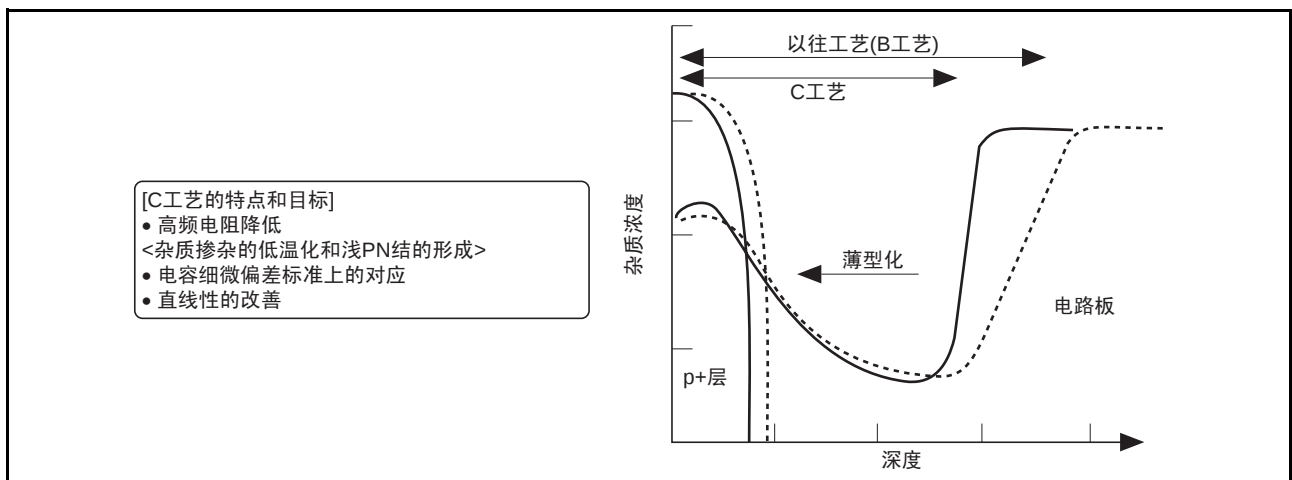


图1.3 C工艺的特点和杂质分布图比较

2. 变容二极管的应用例子

2.1 不同调谐电压的新产品开发路线图（调谐器VC）

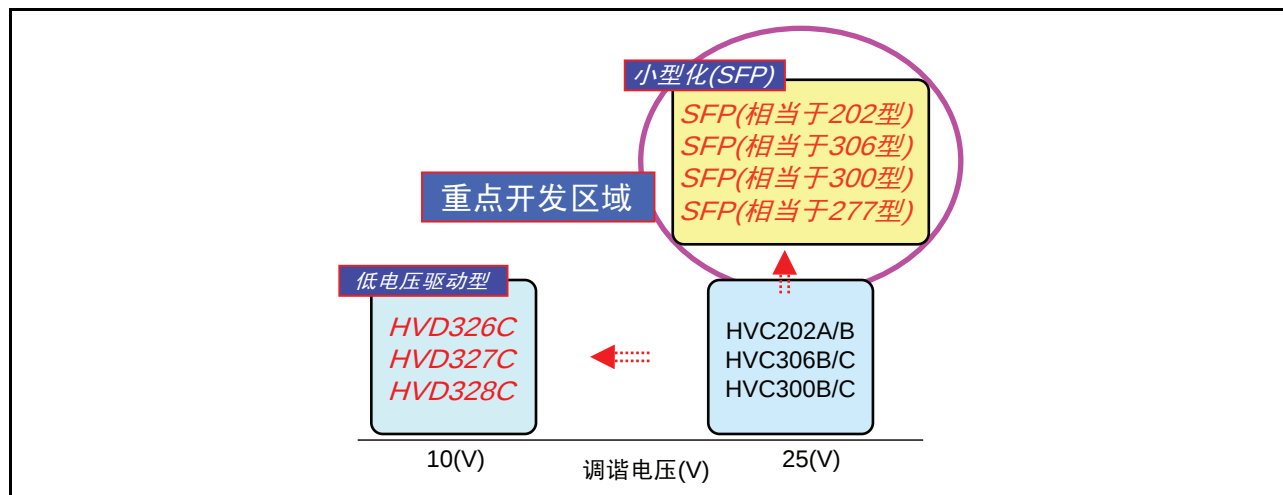


图 2.1 不同调谐电压的新产品开发路线图（调谐器VC）

2.2 不同频率的新产品开发路线图 (VCO)

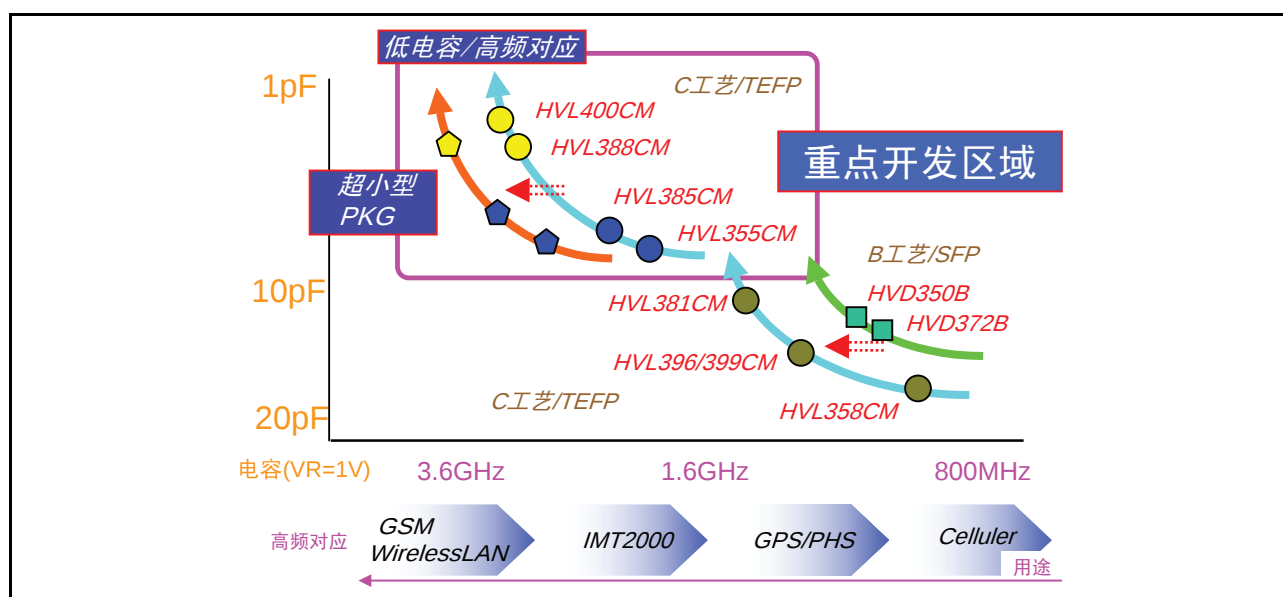


图 2.2 不同频率的新产品开发路线图 (VCO)

3. 变容二极管的结构

3.1 芯片截面结构

如图3.1所示，变容二极管使用了高品质的硅单晶体，为了确保高可靠性，还使用了硅外延平面型芯片。

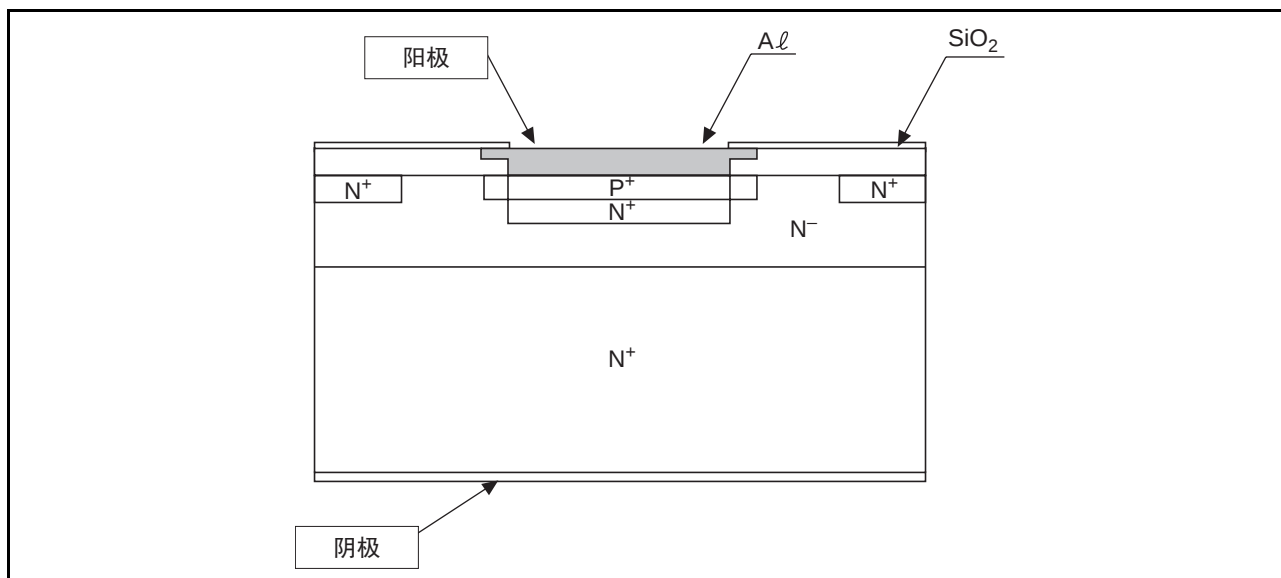


图3.1 芯片截面图例子

3.2 组装结构

变容二极管采用了SRP、URP、UFP、SFP、EFP、MPAK、CMPAK和CMPAK-4的各种封装。（参照图3.2～图3.5）

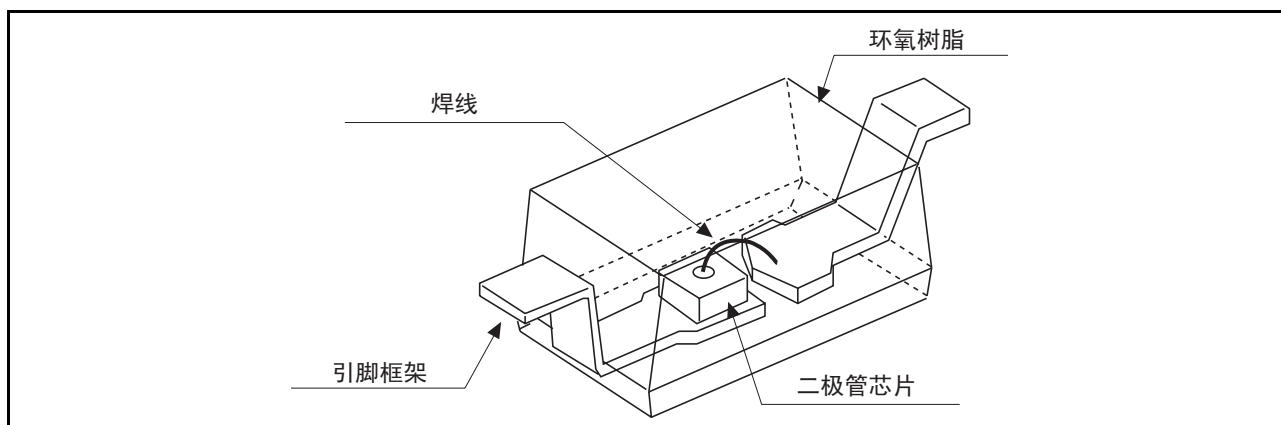


图3.2 SRP、URP结构图

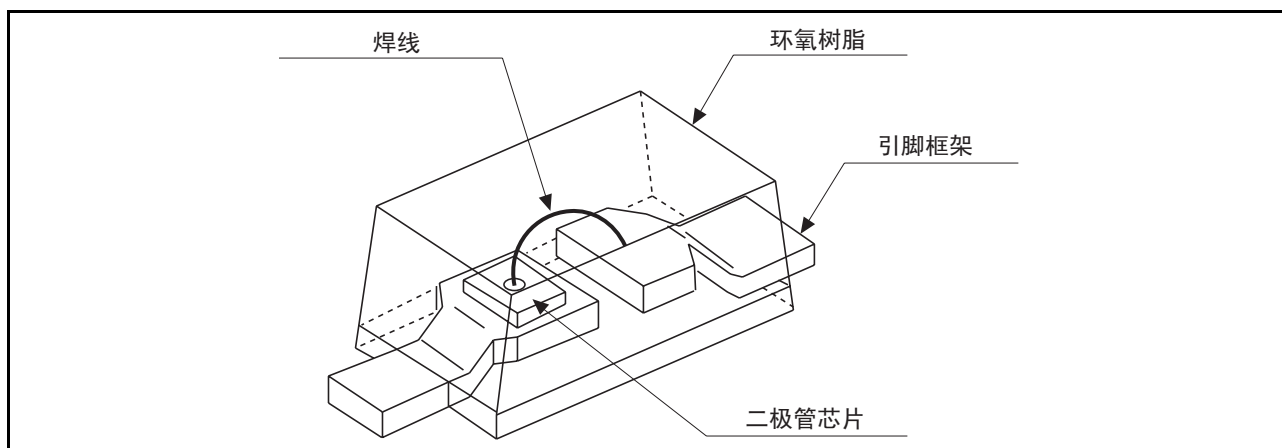


图 3.3 UFP、SFP、EFP 结构图

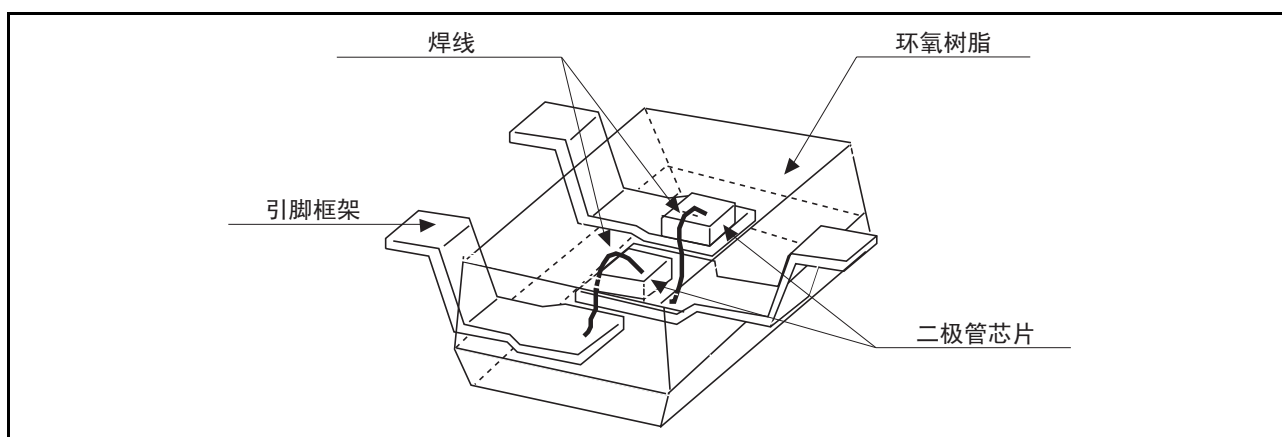


图 3.4 MPAK、CMPAK 结构图

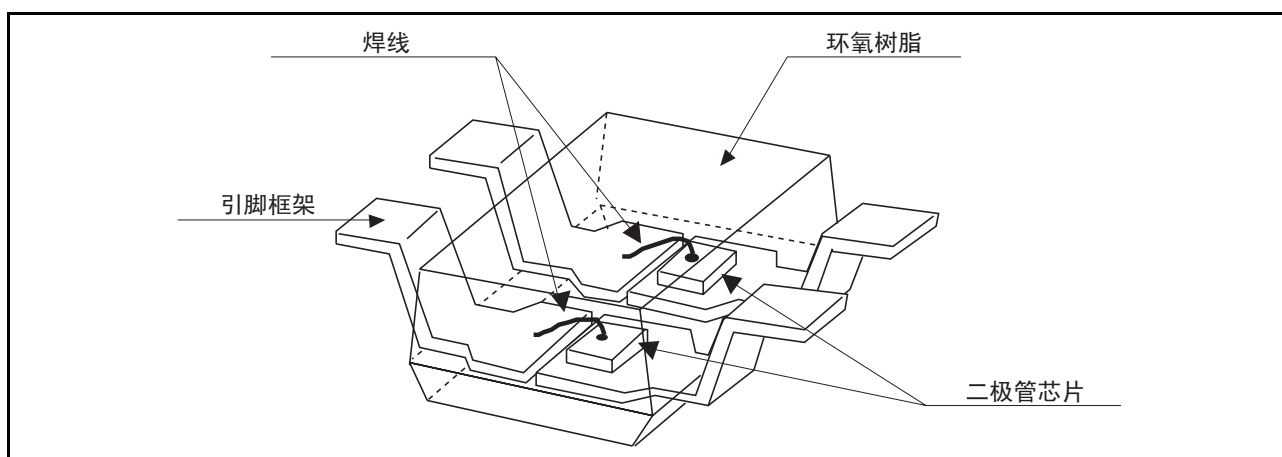


图 3.5 CMPAK-4 结构图

3.3 封装趋势

以手机为代表的便携式机器，在追求设备的薄型化和多功能化的同时，对于面向安装了VCO和天线开关等各种模块的电子器件，更加大了对薄型化的需求。

瑞萨变容二极管批量生产了1006型（本体尺寸 $0.8 \times 0.6 \times 0.5 \text{ max(mm)}$ ）EFP（Extremely small Flat Package/瑞萨封装代码）封装的二极管，1006型是引脚型中尺寸最小的型号。另外，为了进一步对应超薄型化，研发了1006型（本体尺寸 $0.8 \times 0.6 \times 0.4 \text{ max(mm)}$ ）的超小型/薄型“TEFP（Thin Extremely small Flat Package/瑞萨封装代码）”封装。

该封装方式可将封装厚度减少到相同面积产品的80%左右。并且，因为是引脚型变容二极管，所以更容易使用，其 0.4 max(mm) 的厚度有效地实现了安装设备的薄型化。

综上所述,瑞萨在器件性能的提高和封装的小型化方面都作出了不懈的努力。

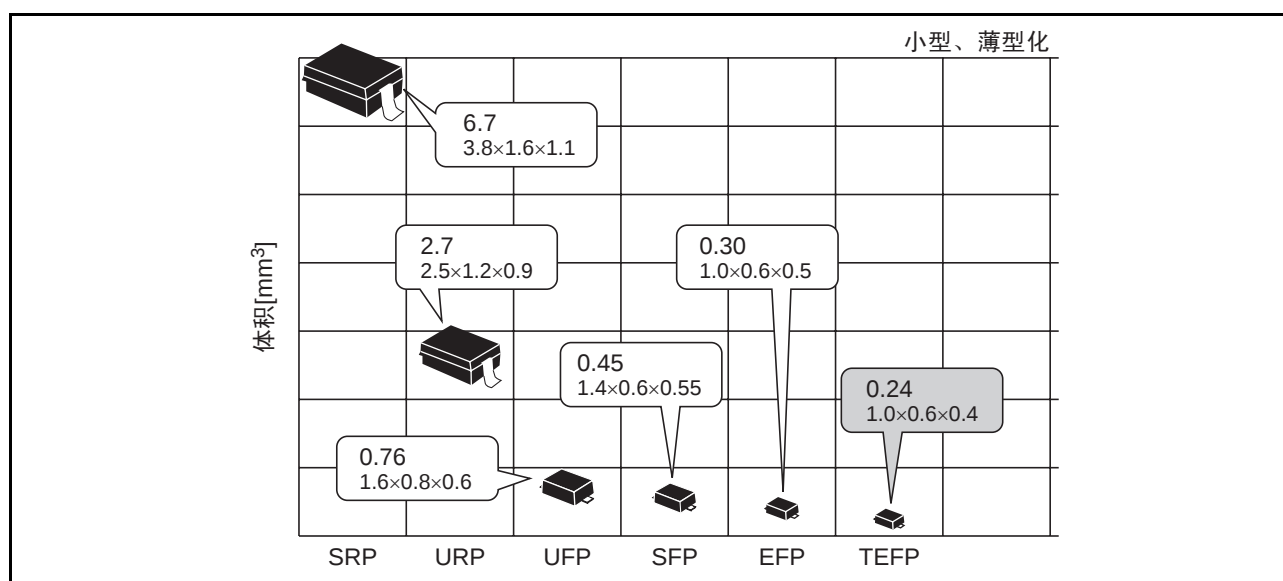
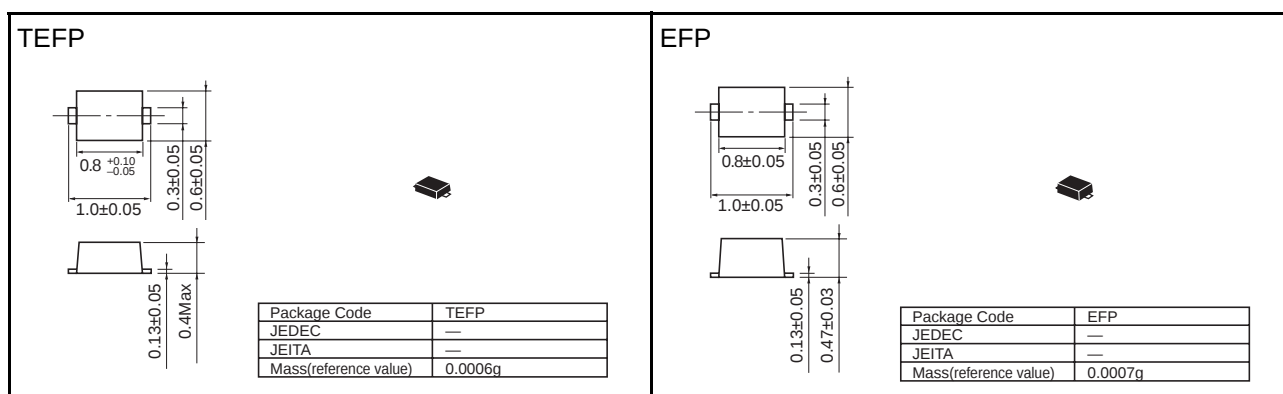


图3.6 封装趋势

3.4 各封装的封装图

Unit: mm



（接下页）

Unit: mm

SFP <table border="1"> <tr><td>Package Code</td><td>SFP</td></tr> <tr><td>JEDEC</td><td>—</td></tr> <tr><td>JEITA</td><td>—</td></tr> <tr><td>Mass(reference value)</td><td>0.0010g</td></tr> </table>	Package Code	SFP	JEDEC	—	JEITA	—	Mass(reference value)	0.0010g	UFP <table border="1"> <tr><td>Package Code</td><td>UFP</td></tr> <tr><td>JEDEC</td><td>—</td></tr> <tr><td>JEITA</td><td>Conforms</td></tr> <tr><td>Mass(reference value)</td><td>0.0016g</td></tr> </table>	Package Code	UFP	JEDEC	—	JEITA	Conforms	Mass(reference value)	0.0016g
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Package Code	MPAK																
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JEITA	Conforms																
Mass(reference value)	0.011g																

4. 关于焊接

4.1 温度分布图例子

4.1.1 回流焊接法的使用条件

表 4.1 二极管封装的焊接条件

引脚镀层	Sn-Pb		Sn-Bi、Sn-Cu	
安装焊膏	Sn-Pb 共晶	Sn-Ag 系列	Sn-Pb 共晶	Sn-Ag 系列
封装表面温度 (最大值)	峰值温度: 260°C 不低于 220°C、60 秒以内		峰值温度: 260°C 不低于 220°C、60 秒以内	
温度分布图				

4.1.2 射流焊接法的使用条件

使用射流焊接法的焊接条件如下所示:

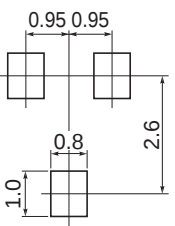
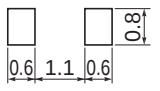
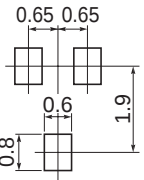
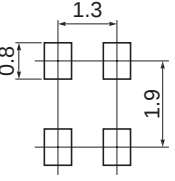
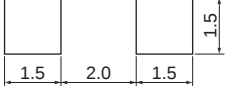
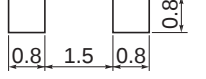
表 4.2 使用射流焊接法的焊接条件

项目		条件	最大值	条件规定
预热	温度	80 ~ 150°C	—	电路板表面
	时间	1 ~ 3 分		
浸焊	温度	230 ~ 250°C	260°C	焊料层温度
	时间	2 ~ 4 秒	10 秒	经过焊料层的时间

4.2 关于表面贴装型二极管的焊盘面积

表面贴装型二极管的焊接条件例子如表4.3所示：

表4.3 表面贴装型二极管的焊接条件例子

项目 封装	焊盘面积 (焊垫) 尺寸	焊膏厚度	项目 封装	焊盘面积 (焊垫) 尺寸	焊膏厚度
MPAK		0.15 ~ 0.30mm	UFP		0.15 ~ 0.30mm
CMPAK		0.15 ~ 0.30mm	SFP		0.15 ~ 0.30mm
CMPAK-4		0.15 ~ 0.30mm	EFP TEFP		0.15 ~ 0.30mm
SRP		0.15 ~ 0.30mm			
URP		0.15 ~ 0.30mm			

- 【注】 1. 焊盘面积（焊垫）的单位是mm。
2. 回流安装时焊膏厚度的例子。

5. 变容二极管的连续卷带方式(C.C方式)

5.1 瑞萨的C.C.方式

用于电子调谐器/前端等的可变电容二极管，为了避免频带内的追踪错误，使用电压—电容特性（C-V曲线）分组后的二极管。分组后的二极管因调谐器等的特性要求，必须在规定的偏压范围内将电容偏差($\Delta C/C$)控制在百分之几以内。

作为进行分组的方法，本公司导入C.C.方式(Continuous Connected Taping System)。特此介绍。

5.2 瑞萨的C.C.方式分组方法

半导体的特性偏差是由部材以及制造工艺的偏差引起的。但是，晶片内相邻的产品（芯片）大体上显示为相同特性。因此，通过将相邻的芯片依次组装，并进行带包装，可连续分组。该系统称为C.C.方式。

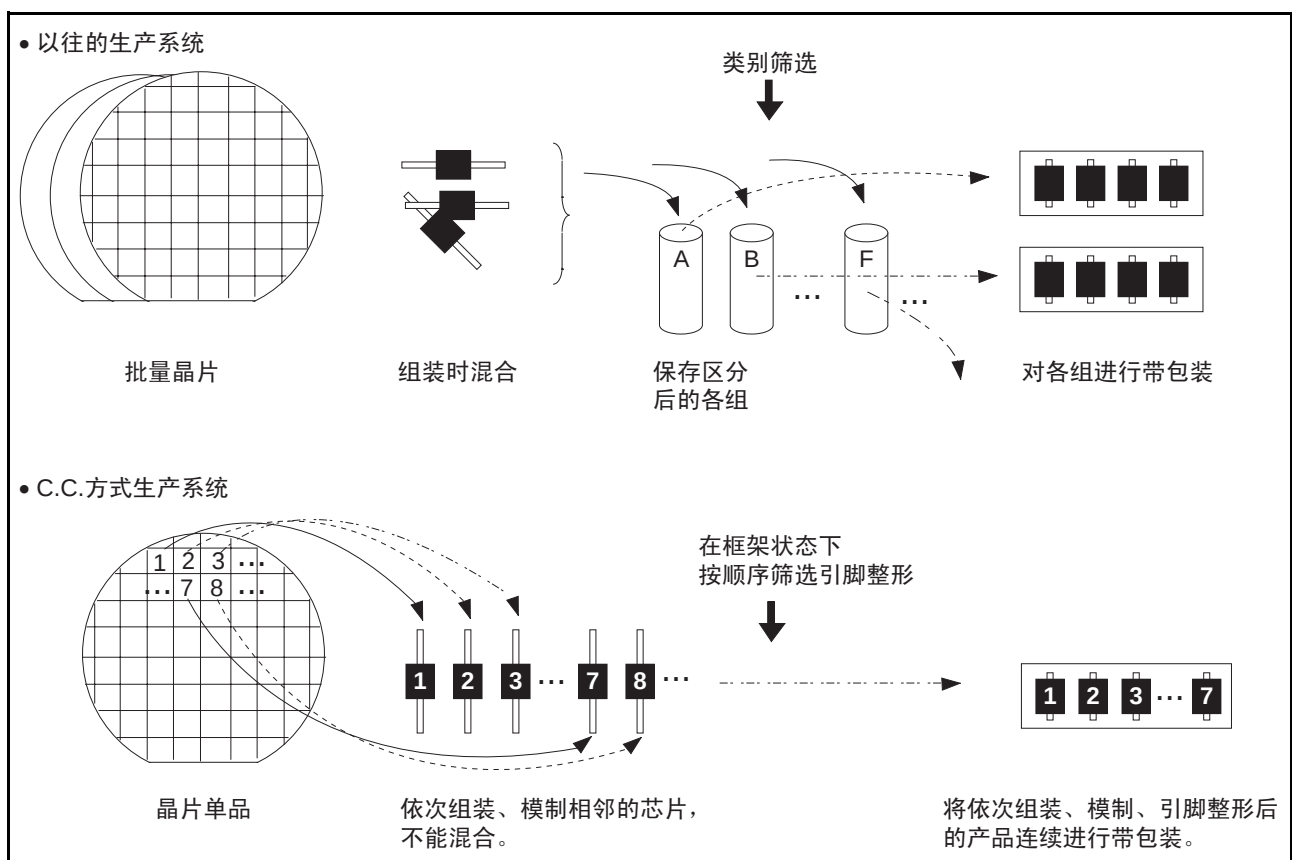
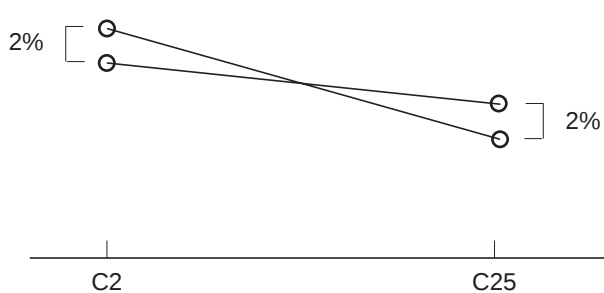
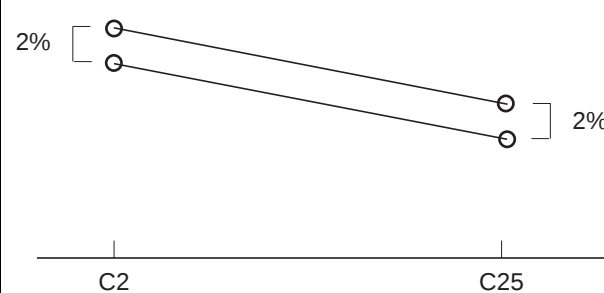


图5.1 以往方式和C.C.方式的系统差异

表5.1 以往方式和C.C.方式的特性差异

以往方式	C.C.方式
C-V曲线的平行性少  例如: $\Delta C/C=2\%$时, 有可能存在如上图的交叉曲线型。	有C-V曲线的平行性  例如: $\Delta C/C=2\%$时, 也有可能存在如上图的平行性。因此, 调谐器的追踪特性良好。
<u>$\Delta C/C$值大</u> 鉴于筛选方式, 分布在筛选设定值内。	<u>$\Delta C/C$值小</u> 连续的将相邻的芯片进行带包装, 偏差变小。
<u>卷盘内组数 (间断) 多</u> 鉴于类别筛选, 分组后的数量变少。因此, 卷盘内组数增加。	<u>卷盘内组数 (间断) 少</u> 为了保持系统连续性, 可减少卷盘内的间断, 能够改善使用时的安装效率。(安装机器的停止次数减少)

5.3 瑞萨C.C.方式的卷带规格

主要规格如下所示。

- (1) $\Delta C/C$ 方式可保证任意连续的10个二极管。(但是, 根据产品不同连续数量也会发生变化。)
- (2) 卷带型号 (准备了以下2种类型。)

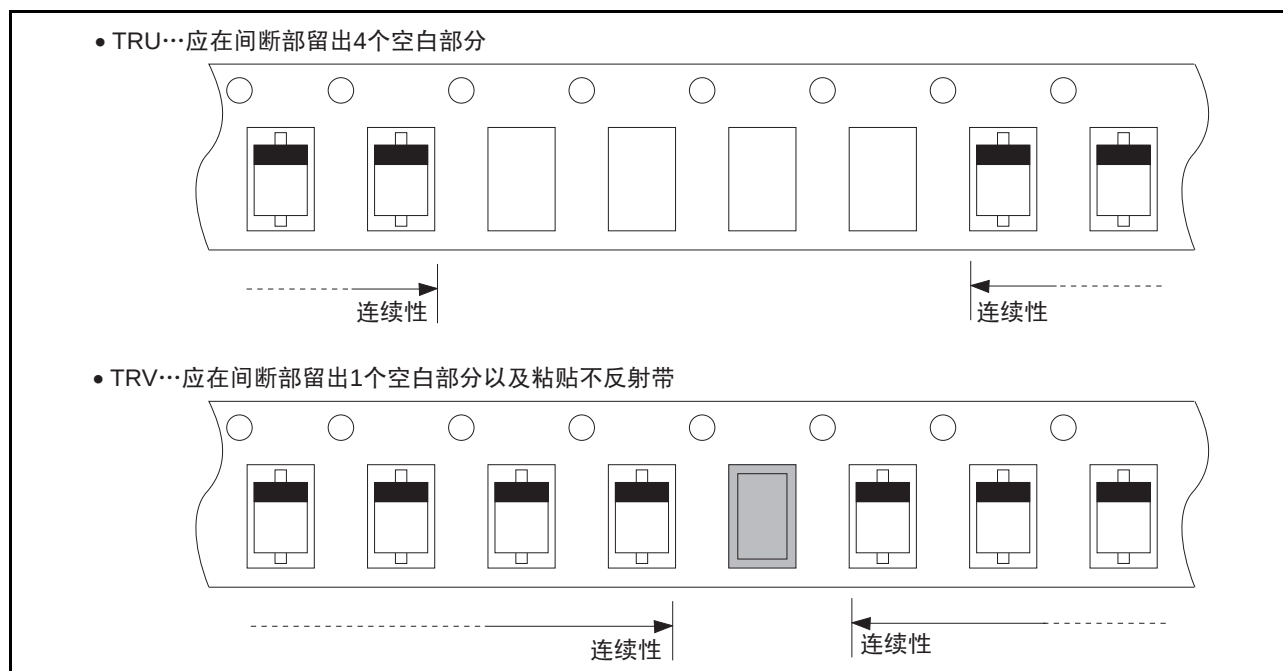


图5.2 C.C.方式的卷带规格

6. 标准特性

6.1 VCO用变容二极管(1)

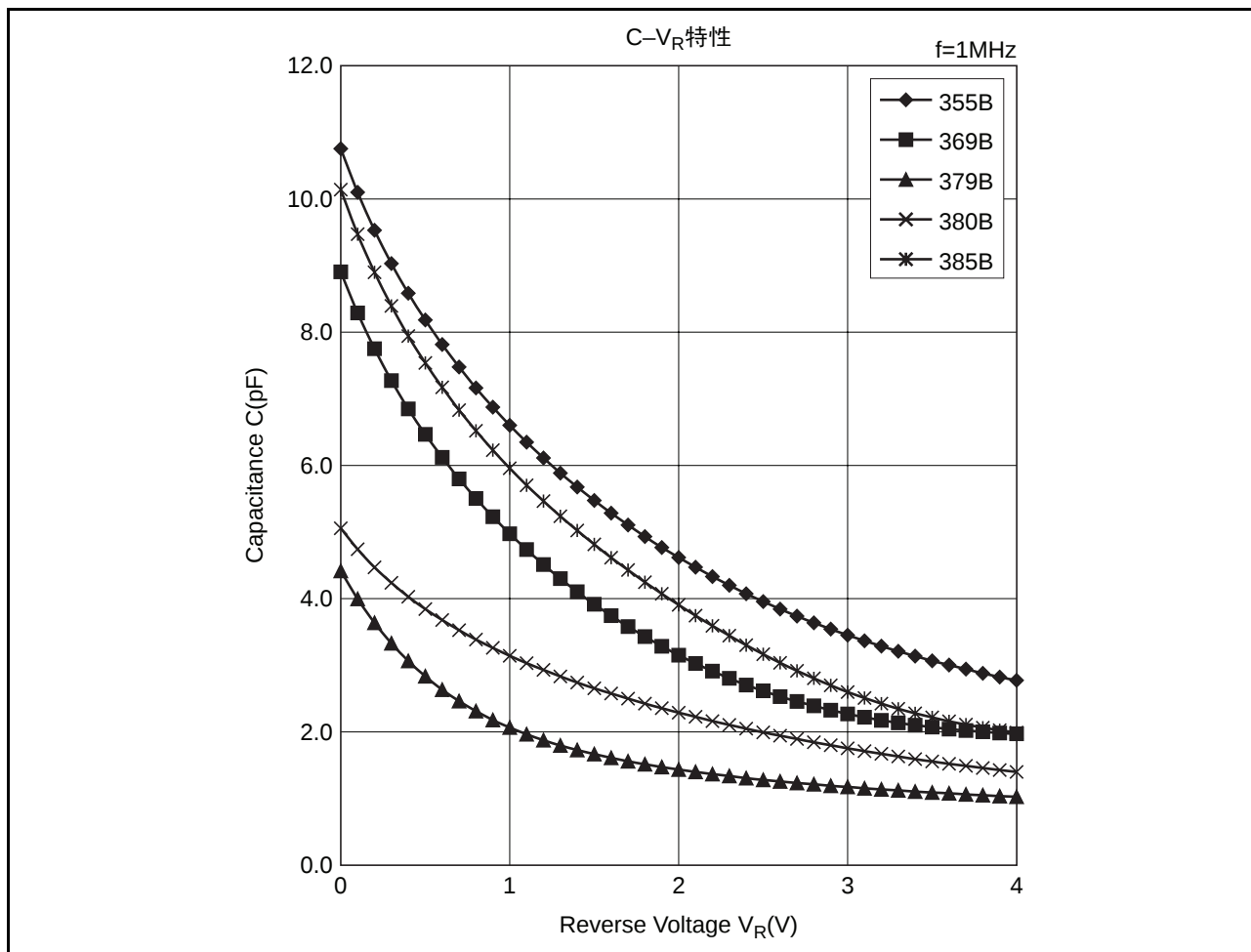


图6.1 VCO用变容二极管(1)

6.2 VCO用变容二极管(2)

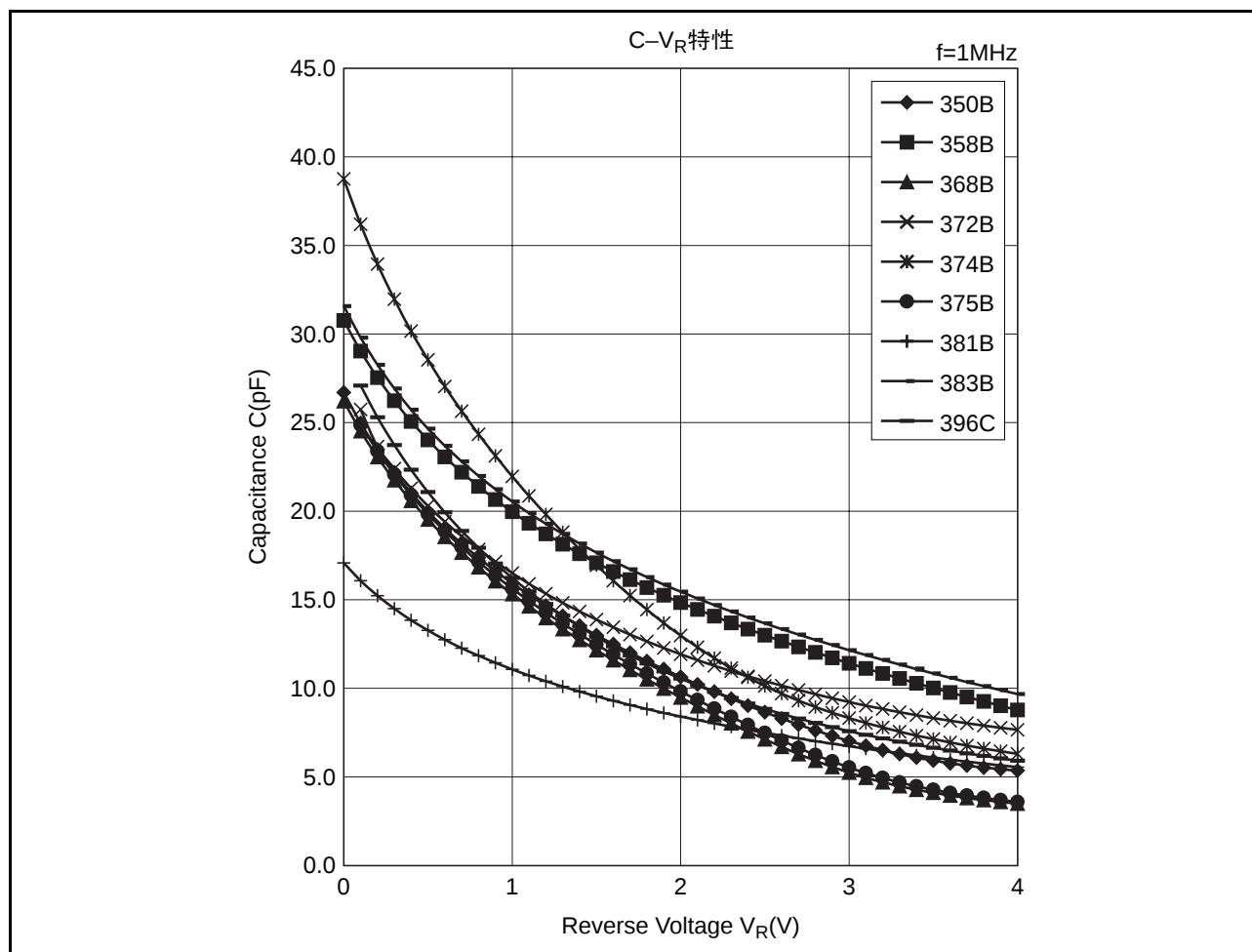


图6.2 VCO用变容二极管(2)

6.3 VCO用变容二极管(3)

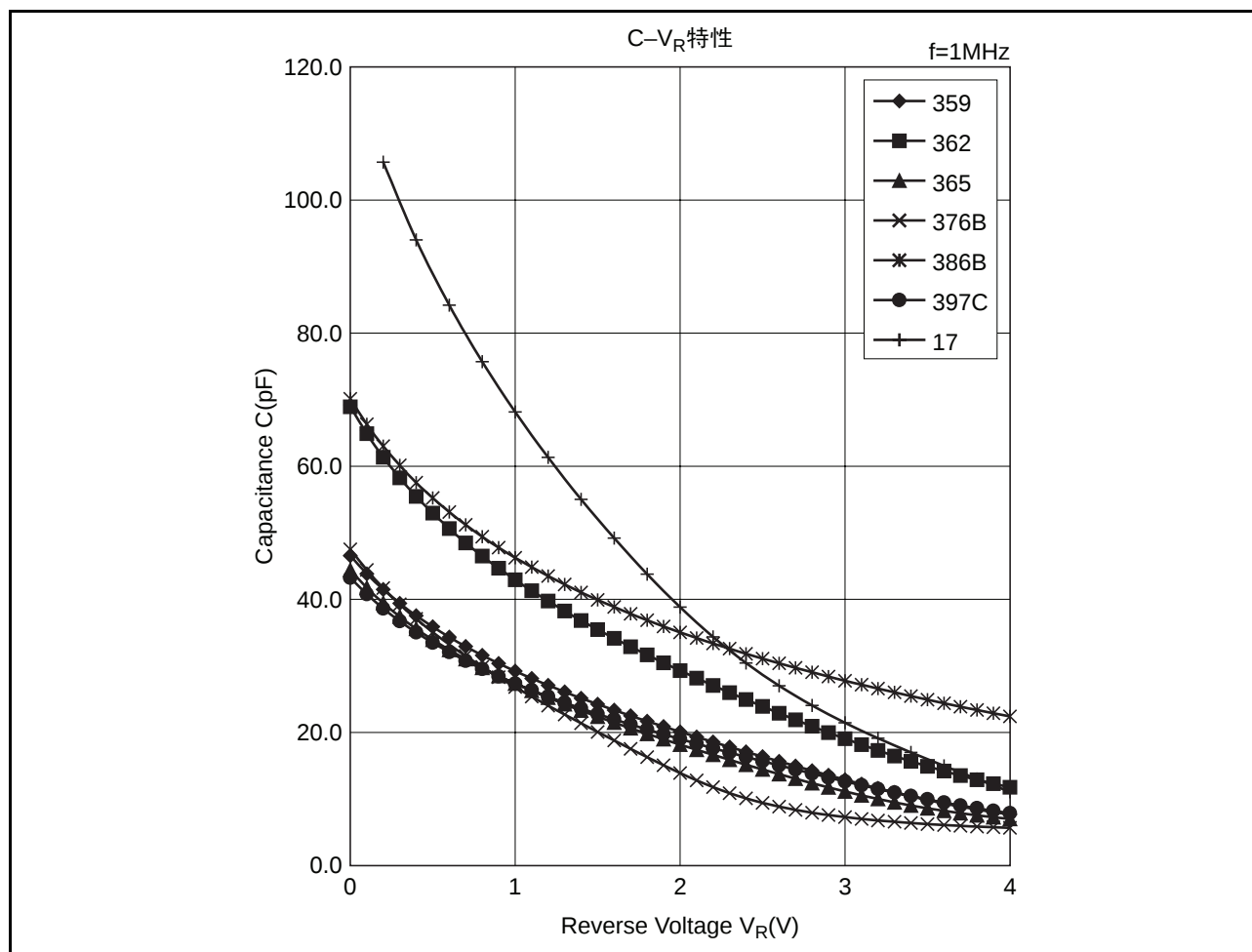


图6.3 VCO用变容二极管(3)

6.4 调谐器用变容二极管(1)

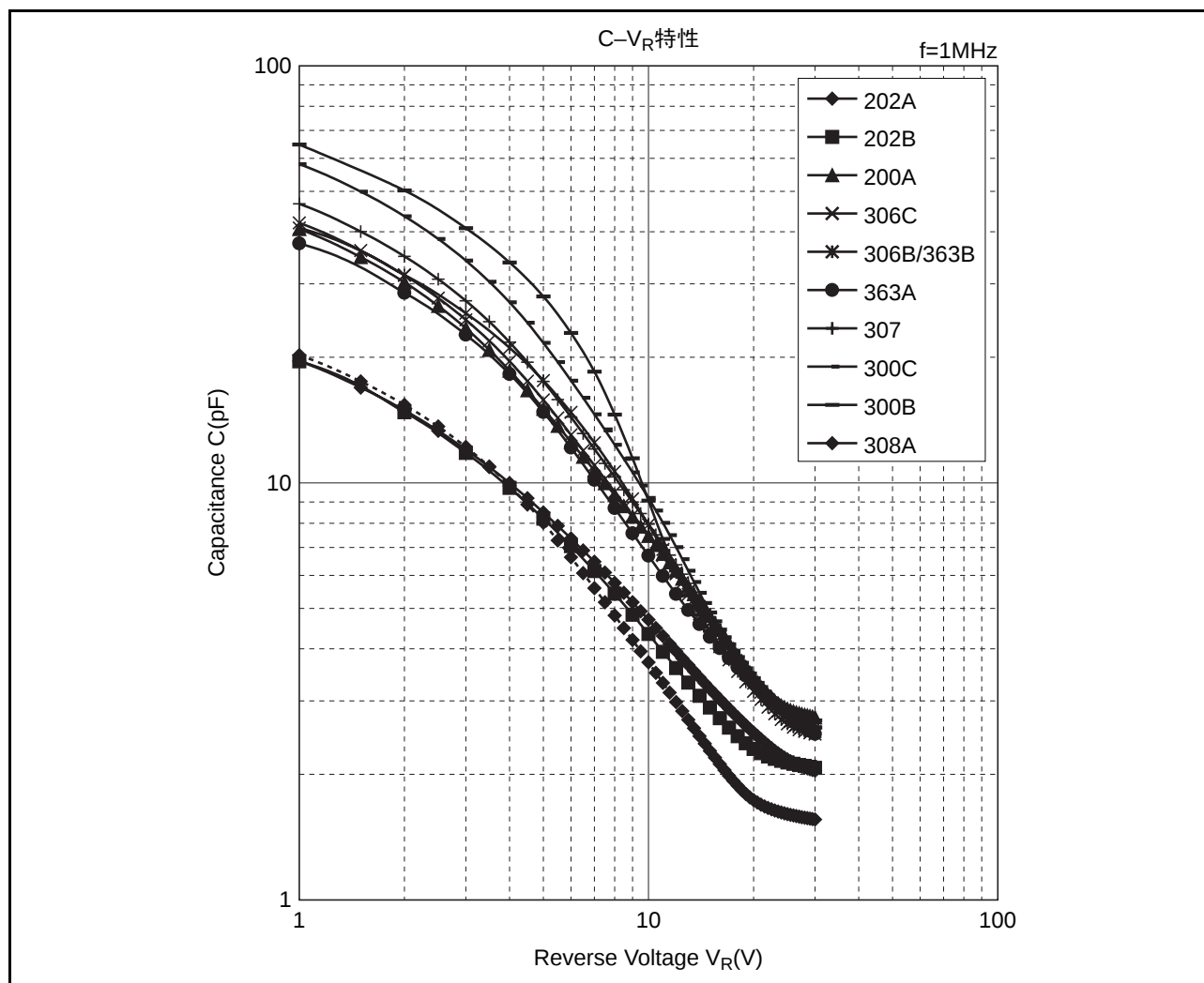


图 6.4 调谐器用变容二极管(1)

6.5 调谐器用变容二极管(2)

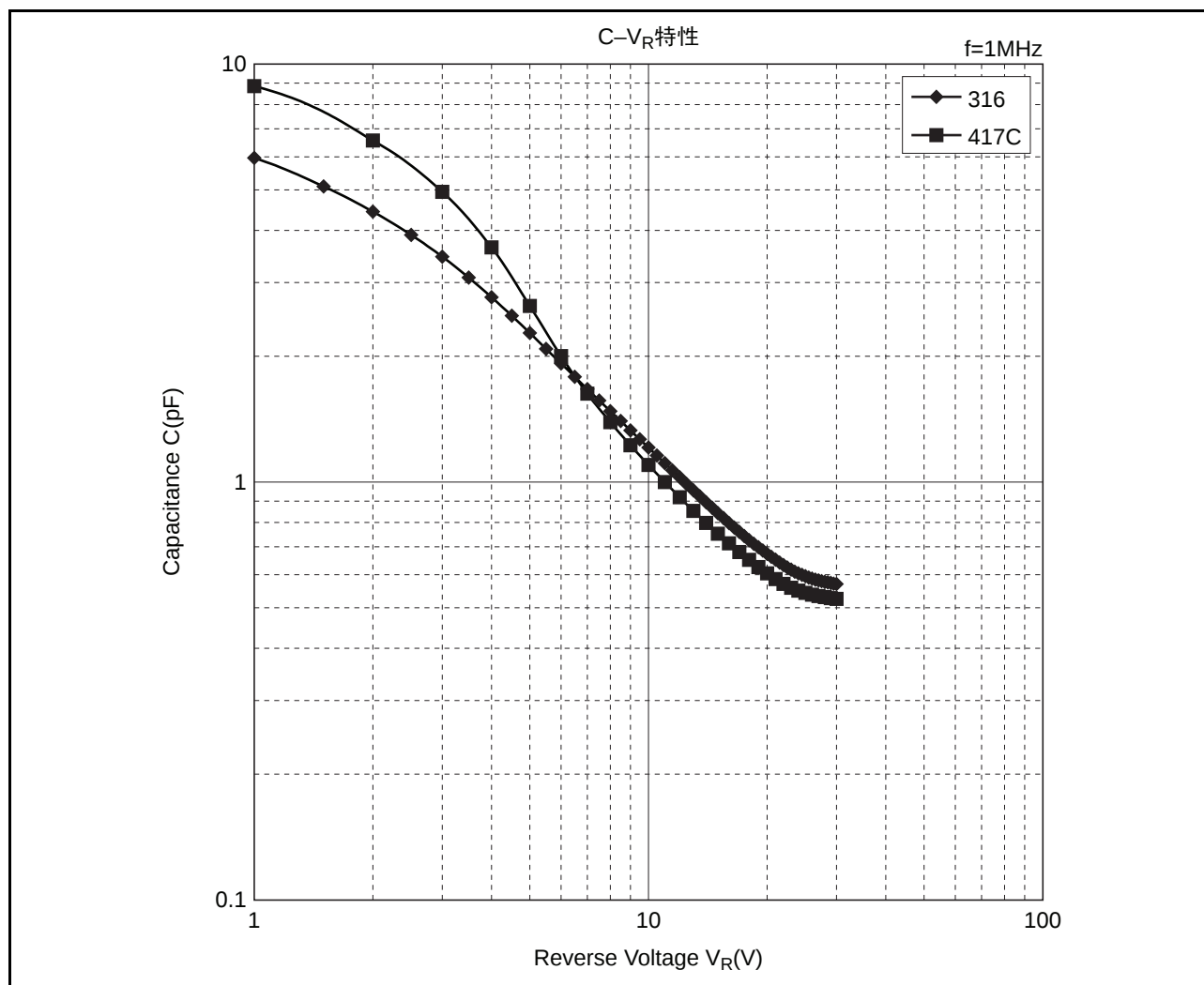


图 6.5 调谐器用变容二极管(2)

6.6 调谐器用变容二极管(3)

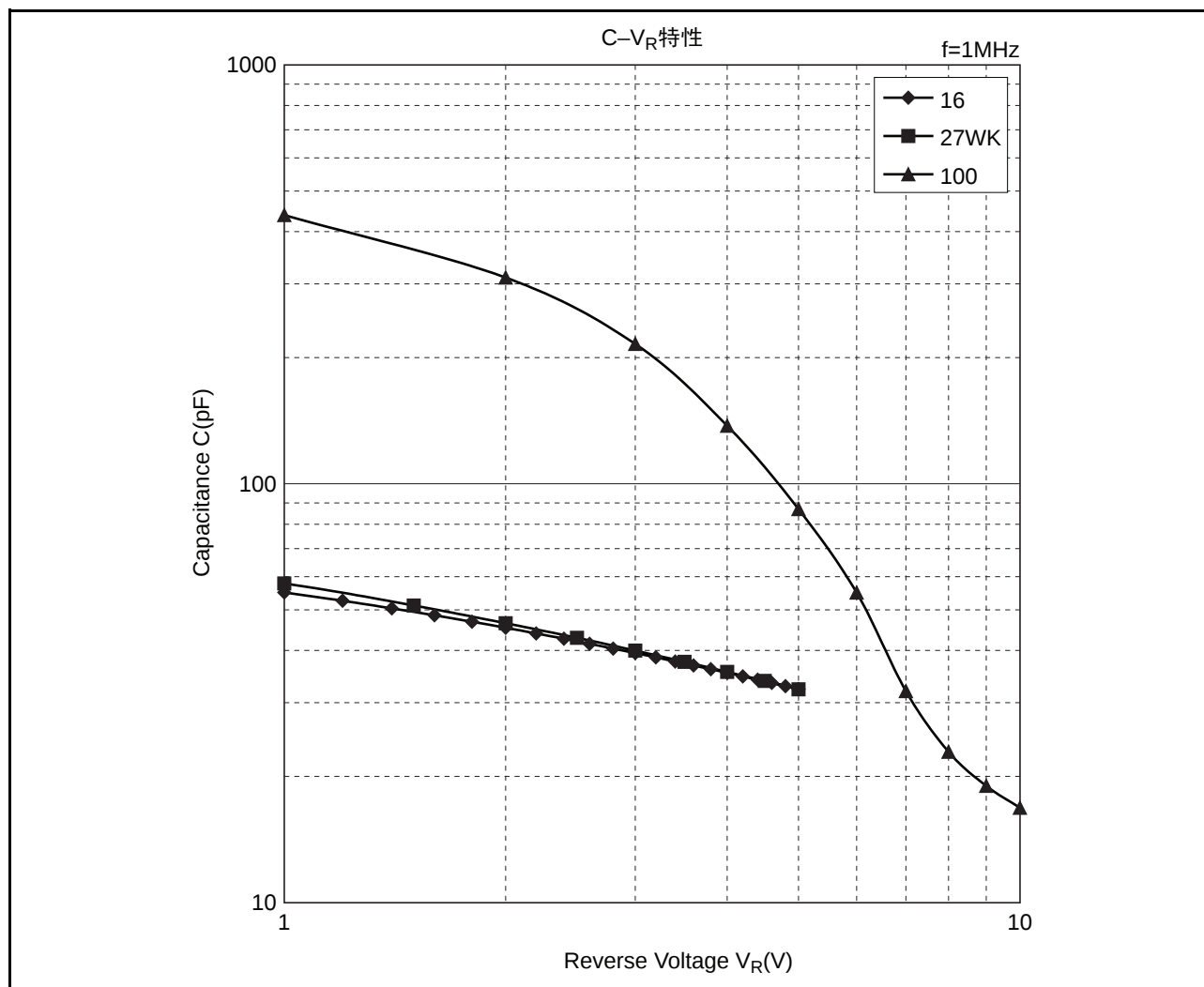


图6.6 调谐器用变容二极管(3)

修订记录

Rev.	发行日	修订内容	
		页	修订处
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