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2010年4月1日  
瑞萨电子公司

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## Bi-CMOS 逻辑 HD74BC 系列

### 概要

HD74BC 系列既有和高速双极逻辑 IC 同等的高速性和大电流驱动能力，又有 CMOS 的低功耗优点。

在信息产业设备中，存储器总线的缓冲器和系统总线的 I/O 缓冲器等一般使用 8 位结构的高速双极标准逻辑 IC，但是最近的 OA 设备除了小型化和轻量化以外，还需要通过信息的高速处理和系统的低功耗化来延长电池的寿命。因此，也要求标准逻辑 IC 具有：

- (1) 低功耗
- (2) 大电流驱动能力
- (3) 能发展为 16 位的产品
- (4) 能进行表面贴装

为了满足这样的市场需求，利用 Bi-CMOS 加工技术（结合了双极晶体管的大电流驱动能力和 CMOS 的低功耗能力）开发了 Bi-CMOS 总线接口系列。

### 1. 特点

对于大容量存储器的地址缓冲电路以及连接主板和扩展电路板的系统总线 I/O 的多位化，HD74BC 系列的开关速度为 4.5ns(typ)、驱动电流为 64mA，具有和高速双极逻辑同等的特性，并且在 10MHz 工作频率时 HD74BC 系列的功耗大约为高速双极逻辑的 1/5，所以如果使用 HD74BC 系列，就能通过和从前一样的系统设计，力求低功耗，并通过采用贴面封装，实现设备的高密度安装。

HD74BC 系列的输出信号全部被缓冲，输出电压和输出电流的规格在整个族中是共同的。因为在全部的输入/输出引脚和 GND 之间由各肖特基势垒二极管进行钳位，所以抑制了大噪声系统中的阻抗失配引起的负尖峰。除此以外还有以下 2 个特点：

- (1) 当切断设备的电源时，因为输入引脚为高阻抗，所以电流就不从输入引脚流入电源，能防止电池的损耗；当接通电源时，还和以前 CMOS 结构的输入不同，即使外加电源电压以上的输入电压，电流也不会流入，所以不必担心会发生闩锁等情况。
- (2) 因为通过电阻和二极管的组合电路将全部的输入引脚上拉到和输出“H”电平同等的电压，所以能进行和高速双极逻辑同样的引脚处理，而不必在意输入部是由 CMOS 电路构成的。

### 2. 基本电路结构

Bi-CMOS 总线接口系列的基本电路结构如图 1 所示。允许控制电路和输入部由 CMOS 构成，双极晶体管只在输出缓冲器部。因此，当输出引脚不为“L”电平时，就会大幅度地降低功耗。

为了将 HD74BC 系列的全部输入引脚上拉到  $V_{OH}$  电平，连接了电阻和二极管的电路。因此，在输入引脚为“L”电平时大约有 120 $\mu$ A 的电流流过，虽然是 CMOS 结构的输入引脚，但是和双极结构的输入引脚一样不需要处理未使用的引脚。

如果只用电阻进行上拉，因为输出上升到电源电压，所以在输出下降时，输出电压的振幅就会变大，导致噪声变大。但是，因为 HD74BC 系列的上拉电压设定为  $V_{OH}$  电平，所以在输出发生变化时能将对静态输出的影响控制到最小。

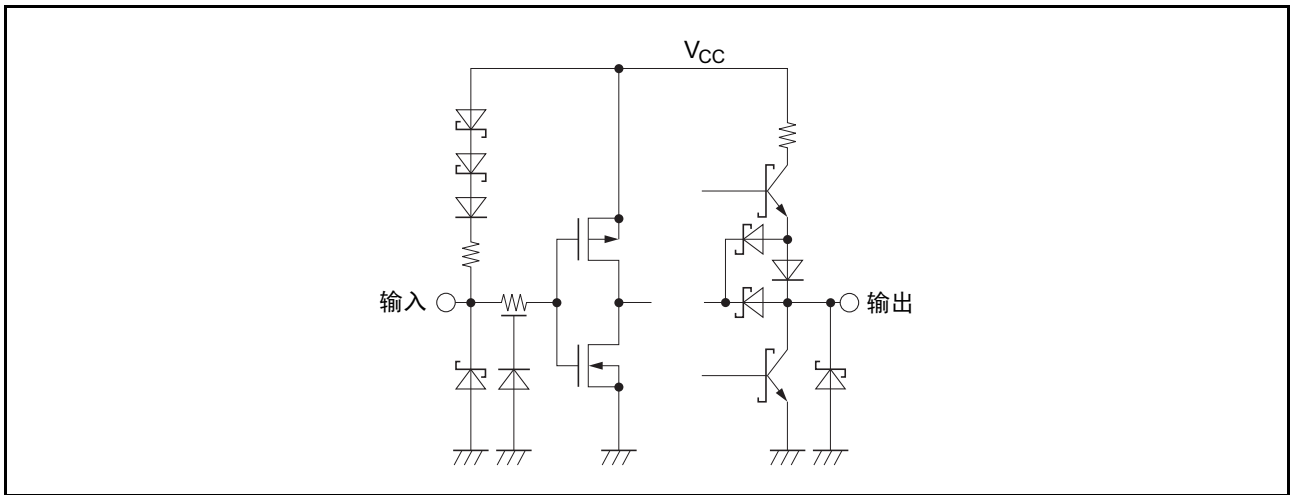


图1 HD74BC系列的电路结构

修订记录

Rev.	发行日	修订内容	
		页	修订处
1.00	2008.03.25	一	初版发行

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