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CMOS 逻辑 HD74AC 系列 (FACT)

电路特性

* FACT 是美国国家半导体公司的注册商标。

1. 功耗

使用 CMOS 逻辑的优点在于超低功耗。在静止状态下，FACT 的功耗比其他双极型产品小了几个数量级。但是在实际使用中，CMOS 结构和双极型结构不仅会产生 DC 功耗，而且还产生 AC 功耗。

通常，功耗为

$$P_D = [(C_L + C_{PD}) \cdot V_{CC} \cdot V_S \cdot f] + [I_Q \cdot V_{CC}]$$

P_D : 功耗

C_L : 负载电容

C_{PD} : 器件的内部等效电容

V_{CC} : 电源电压

V_S : 输出电压振幅

f : 工作频率

I_Q : 静态消耗电流

FACT 的功耗取决于电源电压、工作频率、内部等效电容和负载， V_S 和 V_{CC} 基本相同，在 CMOS 的情况下能忽略 I_Q 。

因此在 CMOS 的情况下，能将上式简化为：

$$P_D = (C_L + C_{PD}) \cdot V_{CC}^2 \cdot f$$

通过用 2 个不同的工作频率测量器件的功耗来计算 CMOS 器件的 C_{PD} 值。 C_{PD} 的计算方法如下：

- (1) 将电源电压 V_{CC} 设定为 5.0V。
- (2) 为了尽可能使更多的输出进行开关动作而设定输入信号条件，并使此条件为 JEDEC 规定的条件中最坏的情况（参照下一章节）。
- (3) 分别用 200kHz 和 1MHz 的输入频率测量电源消耗电流。
- (4) 通过解以下联立方程式，求内部等效电容。

$$P_1 = (C_{PD} \cdot V_{CC}^2 \cdot f_1) + (I_{CC} \cdot V_{CC})$$

$$P_2 = (C_{PD} \cdot V_{CC}^2 \cdot f_2) + (I_{CC} \cdot V_{CC})$$

$$C_{PD} = (P_1 - P_2) / V_{CC}^2 (f_1 - f_2)$$

或者

$$C_{PD} = (I_1 - I_2) / V_{CC} (f_1 - f_2)$$

在此，

I_1 : $f_1=200\text{kHz}$ 时的电源消耗电流

I_2 : $f_2=1\text{MHz}$ 时的电源消耗电流

在 FACT 的数据表中，此 C_{PD} 值表示 1 个封装或者封装内 1 个门的典型值。

FACT 和 FALS 的功耗比较电路如图 1 所示，这是表示 FACT 低功耗性的例子。

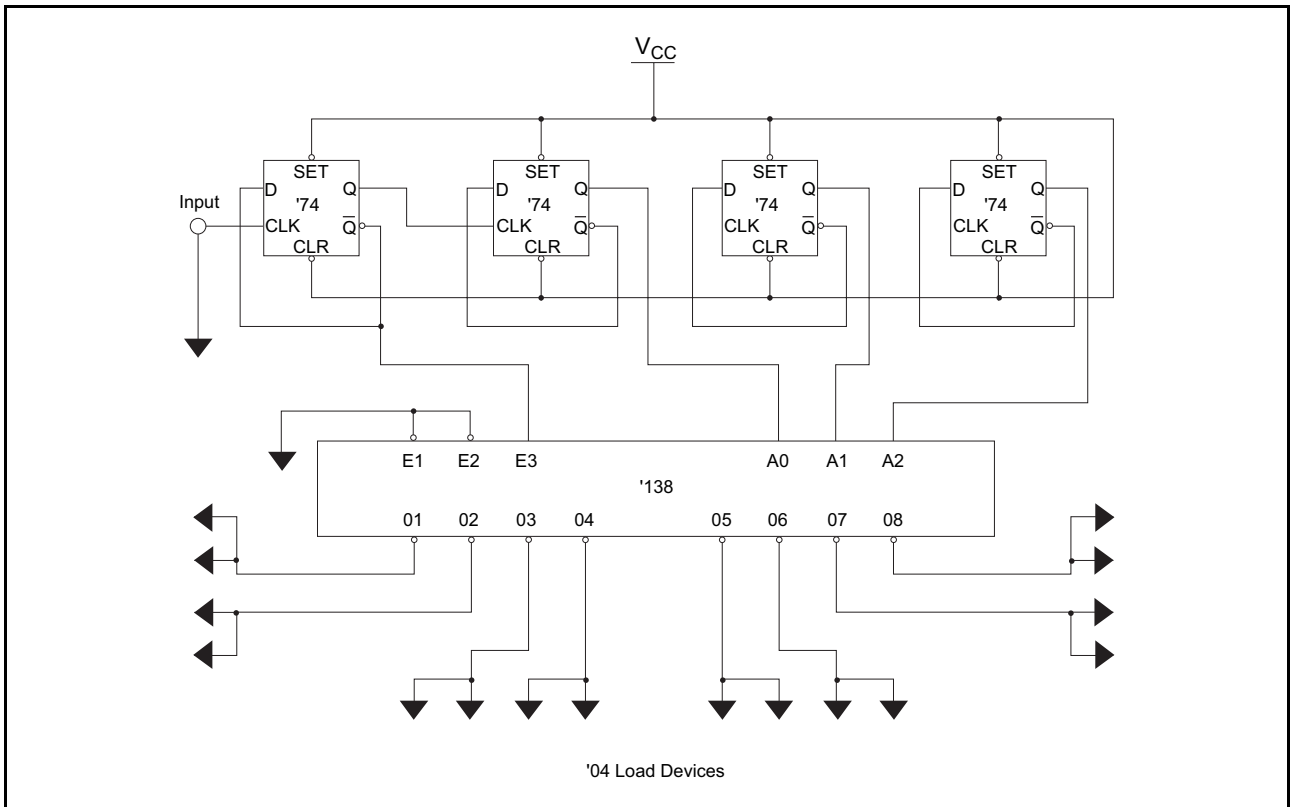


图1 功耗比较电路

在同一电路板上安装了由FACT和FAST构成的2种相同形式的电路，并用同一个输入信号进行驱动。在电路中，将输入信号输入到用作 divide-by-2 频率计数器的4个D触发器，触发器的输出引脚连接到'138解码器的输入引脚，因此'138的输出引脚产生8个互不重叠的时钟脉冲。将'138的输出引脚连接到'04反相器。在不同输入频率下测量的电源功耗如图2所示。

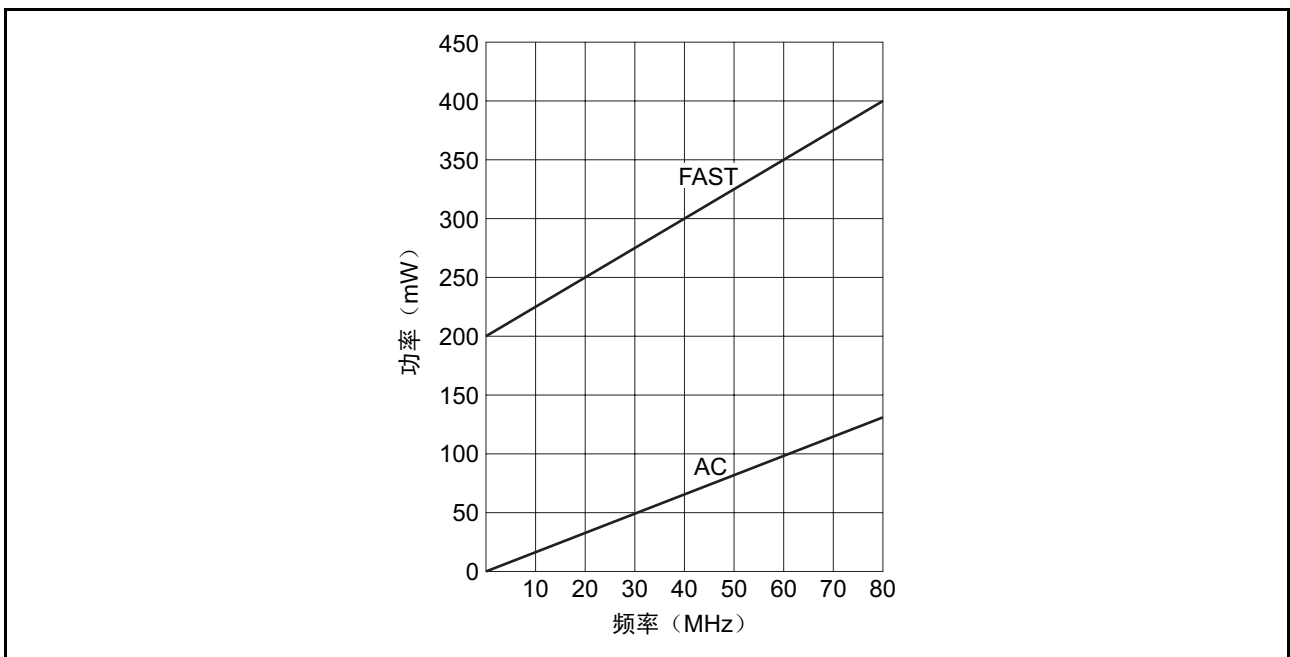


图2 FACT-FAST电路的功耗

因此，使用FACT电路的功耗比使用FAST电路的功耗小得多。尤其在频率为0的静止状态下，使用FACT电路的功耗为0，而使用FALS电路的功耗约为200mW。

2. 负载电容的特性

在FACT的情况下，当负载电容大于50pF时，必须考虑负载电容对传播延迟时间的影响。能通过下表求出传播延迟时间，传播延迟时间是在输出波形50%的位置被测定的。

表1 负载电容的特性

项目		V _{CC} (V)			单位
		3.0	4.5	5.5	
trise	FACT	31	22	19	ps/pF
tfall	FACT	18	13	12.5	ps/pF

在不同的负载电容C_L和电源电压V_{CC}时测定的传播延迟时间分别如图3和图4所示，负载电容C_L对输出上升时间和下降时间的影响分别如图5和图6所示。

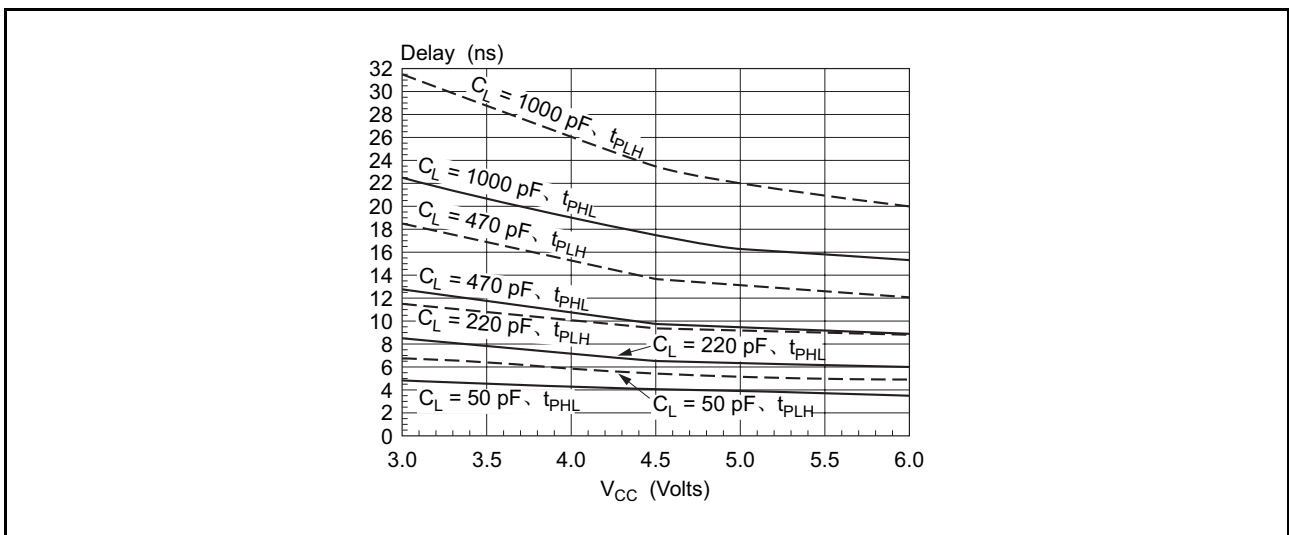


图3 传播延迟时间-V_{CC} (AC)

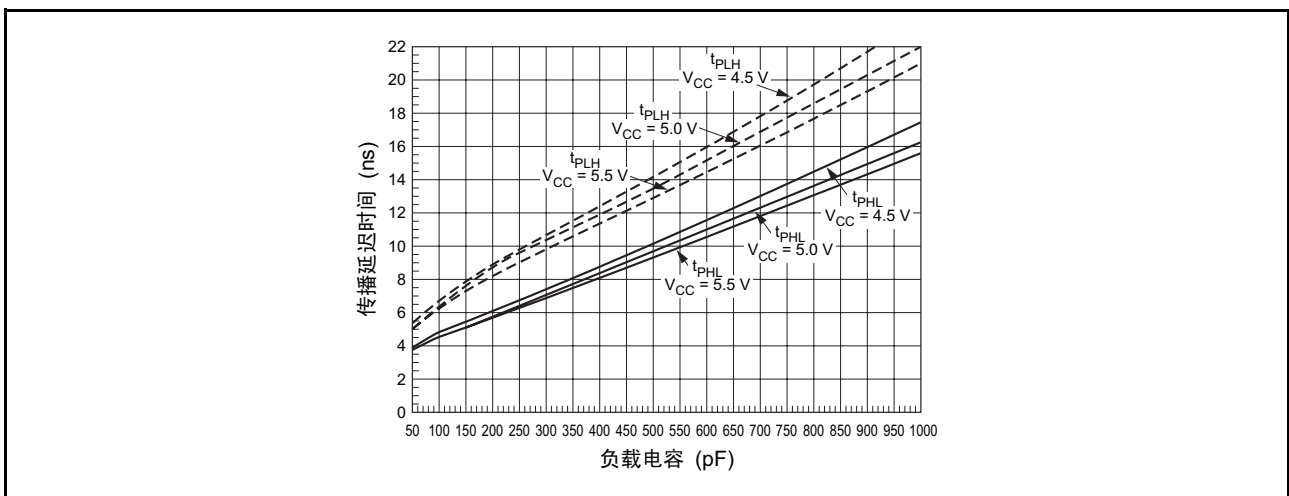


图4 传播延迟时间-负载电容 (AC)

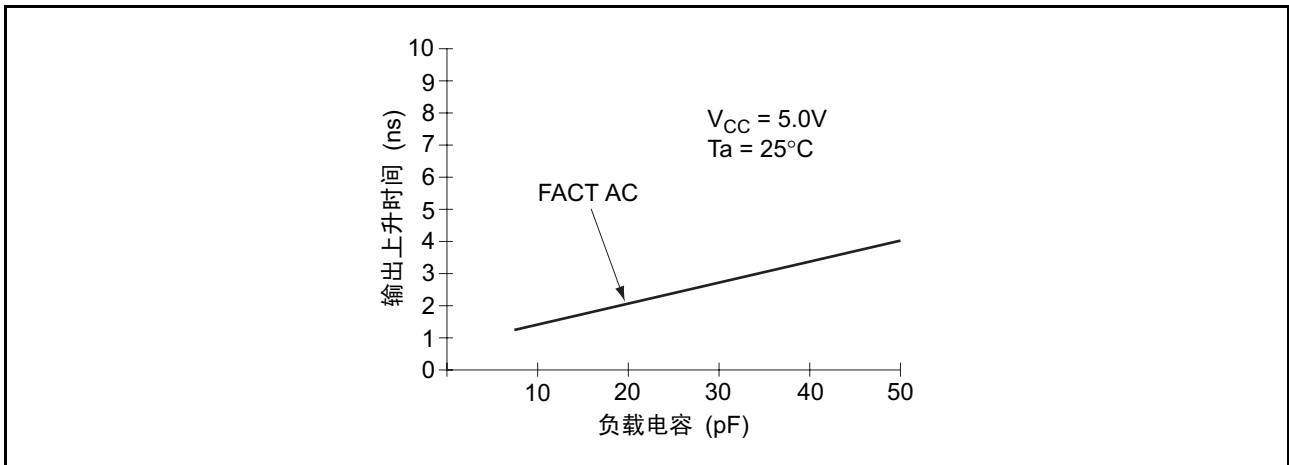


图5 输出上升时间-负载电容

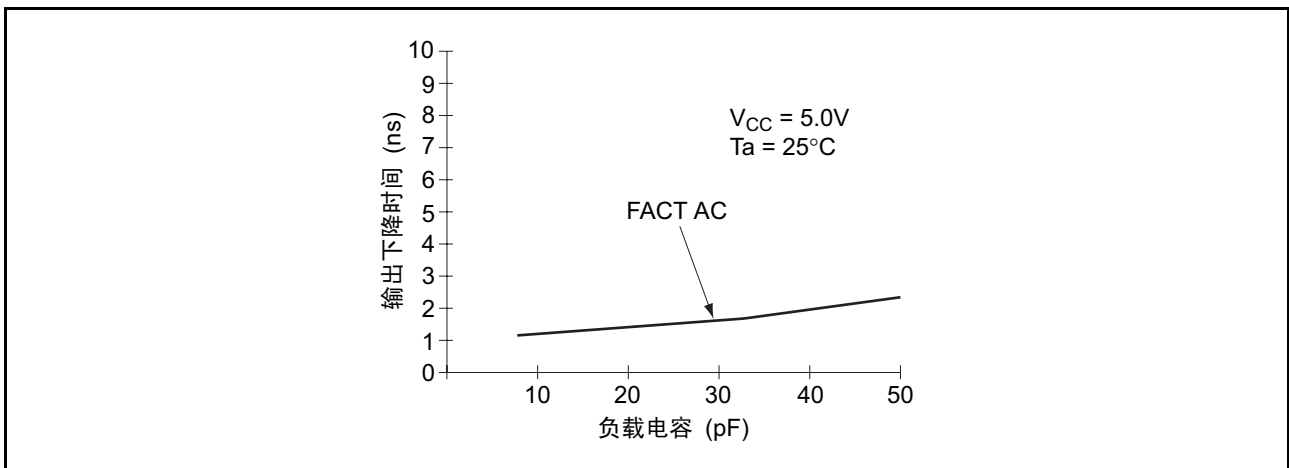


图6 输出下降时间-负载电容

3. 闩锁

对闩锁现象的灵敏度是CMOS的重要问题之一，这是由CMOS高输入阻抗和寄生晶体管的增益引起的。

即使在最坏条件 ($T_a=85^{\circ}\text{C}$ 、 $V_{CC}=5.5\text{V}$) 下给输入/输出引脚外加100mA的动态电流，FACT也不会产生闩锁现象，而且在室温下，即使外加不小于450mA的动态电流，通常也不会产生闩锁现象。

在实际使用中，一般不会出现闩锁问题，但是必须了解此现象的产生原因和防止对策。

在设计FACT时，特别注意到尽量降低闩锁现象产生的可能性。

FACT降低了寄生晶体管的增益、降低了N阱和P阱的电阻以及增加了导通寄生晶体管时所需的外部驱动电流。另外，通过版图设计设法防止了衬底注入电流和其他元件的耦合，进一步提高了闩锁耐量。

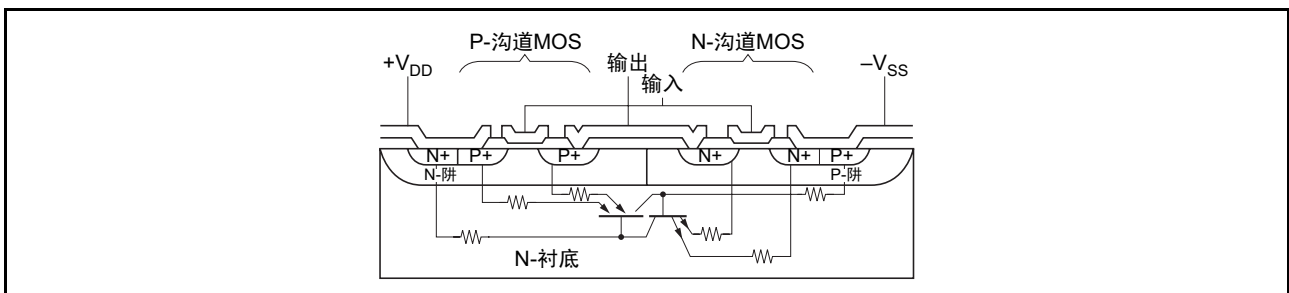


图7 CMOS反相器结构中的寄生晶闸管结构

4. 抗静电击穿能力

FACT 具有非常好的抗静电击穿能力。

FACT 符合 MIL-STD Test Method 3015 的 B 类。

在使用 FACT 时不需要特别注意，但是必须注意和一般 IC 相同的注意事项。

静电试验电路以及用于试验的放电脉冲波形分别如图 8 和图 9 所示。

试验方法：以 5 秒间隔给被测量的引脚外加 5 次 2000V 的脉冲。然后，调换极性，按照同样的方法进行试验。在对全部引脚进行试验后，如果符合 DC 项目和 AC 项目的全部规格，该器件就符合 MIL-STD TM3015 的 B 类。

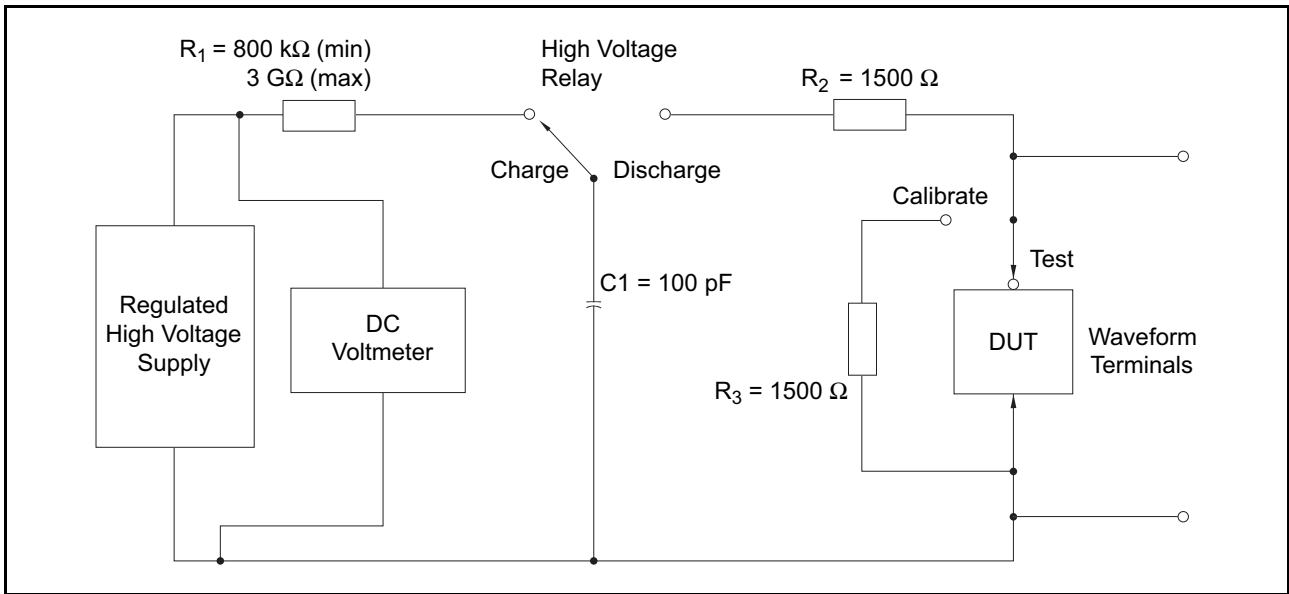


图 8 静电试验电路

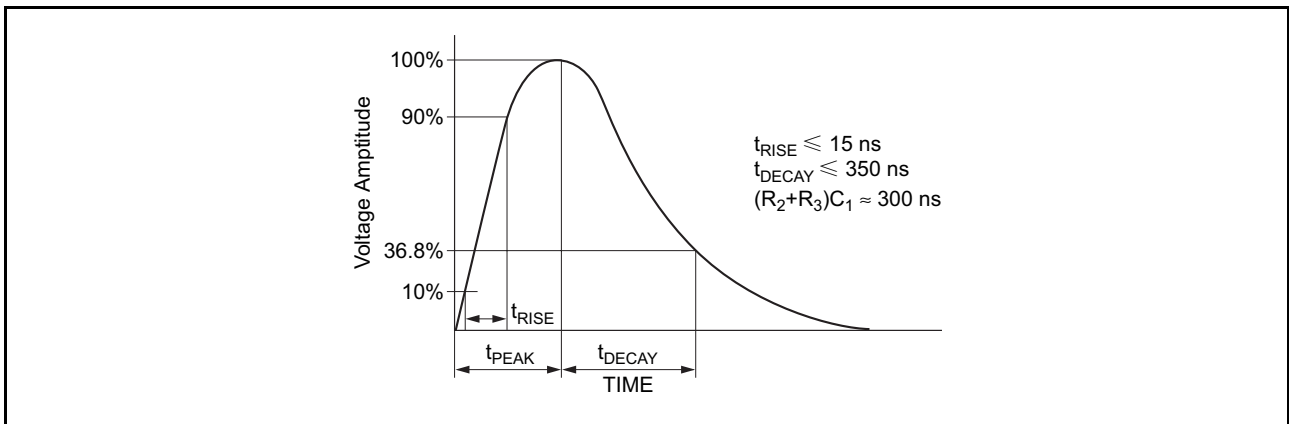


图 9 脉冲波形

修订记录

Rev.	发行日	修订内容	
		页	修订处
1.00	2008.03.25	一	初版发行

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