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瑞萨电子公司网址：http://www.renesas.com

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【发行】瑞萨电子公司（http://www.renesas.com）

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低电压CMOS逻辑IC HD74LV_A/LVC系列

术语和符号

1. 电特性和推荐工作条件

(1) DC特性

符号	术语	说明
V_{IH}	“H”电平输入电压	保证逻辑元件在某规格内正常工作的“H”电平输入电压。
V_{IL}	“L”电平输入电压	保证逻辑元件在某规格内正常工作的“L”电平输入电压。
V_{OL}	“L”电平输出电压	在使输出引脚为“L”电平的输入条件下，规定的输出电流I_{OL}（例如，假定最大扇出时的最大流入电流）流入输出引脚时的输出电压。
V_{OH}	“H”电平输出电压	在使输出引脚为“H”电平的输入条件下，规定的输出电流I_{OH}（例如，假定最大扇出时的最大流入电流）从输出引脚流出时的输出电压。
I_{IH}	“H”电平输入电流	给输入引脚外加规定的“H”电平电压时，流入的输入电流。
I_{IL}	“L”电平输入电流	给输入引脚外加规定的“L”电平电压时，流出的输入电流。
I_{OH}	“H”电平输出电流	在输出引脚为规定的“H”电平输出电压V_{OH}时，流出的输出电流。
I_{OL}	“L”电平输出电流	在输出引脚为规定的“L”电平输出电压V_{OL}时，流入的输出电流。
I_{OZ}	OFF状态的输出电流（高阻抗）	为了使三态输出元件的输出引脚进入高阻抗状态而设定了输入条件时，流入输出引脚的电流。
I_I	输入电流	给输入引脚外加规定的最大输入电压时，流入的输入电流。
I_{CC}	电源电流	流入电源引脚（V_{CC}）的电流。
ΔI_{CC}	当输入规定的电平时，电源电流的变化	在外加规定的输入电压时，每个输入引脚的电源电流的变化量。

(2) 开关特性

符号	术语	说明
f_{max}	最高时钟频率	要通过时钟脉冲使输出状态发生变化而设定了输入/输出条件时，按照规定的顺序，能维持稳定的输出逻辑电平变化的最高时钟重复频率。
t_{PLH}	输出上升沿的传播延迟时间	当输出引脚从 “L” 电平变为 “H” 电平时，在规定的负载条件下，输入和输出电压波形在规定的电压电平之间的延迟时间。
t_{PHL}	输出下降沿的传播延迟时间	当输出引脚从 “H” 电平变为 “L” 电平时，在规定的负载条件下，输入和输出电压波形在规定的电压电平之间的延迟时间。
t_{HZ}	三态输出的禁止时间 （“H” 电平）	当三态输出引脚从 “H” 电平变为高阻抗状态时，在规定的负载条件下，输入和输出电压波形在规定的电压电平之间的延迟时间。
t_{LZ}	三态输出的禁止时间 （“L” 电平）	当三态输出引脚从 “L” 电平变为高阻抗状态时，在规定的负载条件下，输入和输出电压波形在规定的电压电平之间的延迟时间。
t_{ZH}	三态输出的允许时间 （“H” 电平）	当三态输出引脚从高阻抗状态变为 “H” 电平时，在规定的负载条件下，输入和输出电压波形在规定的电压电平之间的延迟时间。
t_{ZL}	三态输出的允许时间 （“L” 电平）	当三态输出引脚从高阻抗状态变为 “L” 电平时，在规定的负载条件下，输入和输出电压波形在规定的电压电平之间的延迟时间。
t_w	脉宽	脉宽波形前后端在规定的电平之间的时间。
t_h	保持时间	在其他相关的输入引脚 （例如，时钟输入）发生变化后，必须对规定的输入引脚保持信号的时间。
t_s	准备时间	在其他相关的输入引脚 （例如，时钟输入）发生变化前，必须对规定的输入引脚数据外加并维持信号的时间。
t_{rec}	恢复时间	从规定的输入引脚解除信号后，到能改变其他相关的输入引脚 （例如，时钟输入）的时间。

2. 功能表

符号	说明
H	High （高）电平 （稳定）（在文章中记为 “H” 或者H电平）
L	Low （低）电平 （稳定）（在文章中记为 “L” 或者L电平）
↑	从L电平变为H电平
↓	从H电平变为L电平
X	H或者L均可
Z	三态输出引脚处于OFF状态 （高阻抗）
a.....h	A～H各输入引脚的稳定状态的输入电平
Qo	确立输入条件前的Q电平
$\overline{Qo}$	Qo的补码
Qn	在发生最新有效变化 （↓或者↑）前的Q电平
	1个H电平的脉冲
	1个L电平的脉冲
TOGGLE	各输出引脚随着输入引脚的有效变化 （↓或者↑）而变为前一个状态的补码

修订记录

Rev.	发行日	修订内容	
		页	修订处
1.00	2008.03.25	—	初版发行

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