RA FAMILY
HARDWARE MANUAL GUIDE
(ELECTRICAL CHARACTERISTICS)

APRIL, 2026

GP EMBEDDED PROCESSOR AND CONTROLLER PRODUCT
MARKETING DEPARTMENT
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EMBEDDED PROCESSING PRODUCT GROUP
RENESAS ELECTRONICS

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DC CHARACTERISTICS

TIMING CONDITIONS

53. Electrical Characteristics

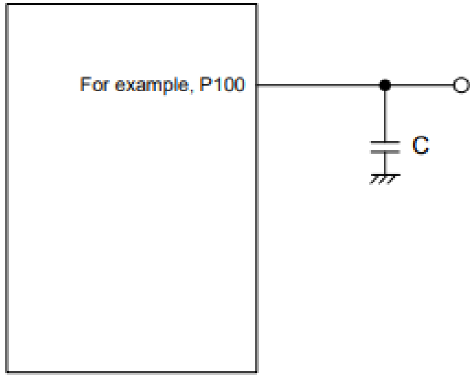
Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
- 2.7 ≤ VREFH0/VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL0/VREFL = VSS_USB = VSS1_USBHS = VSS2_USBHS = AVSS_USBHS = PVSS_USBHS = 0 V
- $T_a = T_{opr}$

Figure 53.1 shows the timing conditions.

The AC characteristics described in this manual are guaranteed only under the following conditions.
If these conditions are not met, the AC characteristics cannot be guaranteed.



V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
Load capacitance C = 30 pF

Figure 53.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

ABSOLUTE MAXIMUM RATINGS

53.1 Absolute Maximum Ratings

Table 53.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC, VCC_USB[*2]	–0.3 to +4.0	V
VBATT power supply voltage	VBATT	–0.3 to +4.0	V
Input voltage (except for 5 V-tolerant ports[*1])	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (5 V-tolerant ports[*1])	V_{in}	–0.3 to + VCC + 4.0 (max. 5.8)	V
Reference power supply voltage	VREFH/VREFH0	–0.3 to VCC + 0.3	V
USBHS power supply voltage	VCC_USBHS	–0.3 to +4.0	V
USBHS analog power supply voltage	AVCC_USBHS	–0.3 to +4.0	V
Analog power supply voltage	AVCC0[*2]	–0.3 to +4.0	V
Analog input voltage	V_{AN}	–0.3 to AVCC0 + 0.3	V
Operating temperature[*3 *4]	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note 1. Ports P205, P206, P400, P401, P407 to P415, P511, P512, and P708 to P713 are 5 V tolerant.
Note 2. Connect AVCC0 and VCC_USB to VCC.
Note 3. See section 53.2.1. Tj/Ta Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

Operation outside this voltage range could cause permanent damage to the LSI.
This does not mean that normal operation is guaranteed

The voltage ranges of power supply that don't cause permanent damage.

The input voltage ranges that don't cause permanent damage to pins.
Application of a voltage outside of this range could cause permanent damage to the LSI pins.
The value in the brackets is applied when VCC or AVCC is equal or greater than the minimum voltage described in the recommended operating voltage

. Operation outside this temperature range if not guaranteed and may cause permanent damage to the LSI.
Derating pf the operation may be required at temperatures above 85 oC

Storage of the device outside this temperature range may cause permanent damage to the LSI

The notes provide supplementary information regarding the electrical characteristics.
Necessary conditions for use.

RECOMMENDED OPERATING CONDITIONS

Table 53.2 Recommended operating conditions

Conditions required to guarantee AC specifications and normal operation.

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC	When USB/USBHS is not used	2.7	—	3.6	V
		When USB/USBHS is used	3.0	—	3.6	V
	VSS		—	0	—	V
USB power supply voltages	VCC_USB, VCC_USBHS		—	VCC	—	V
	VSS_USB, AVSS_USBHS, PVSS_USBHS, VSS1_USBHS, VSS2_USBHS		—	0	—	V
VBATT power supply voltage	VBATT		1.65*2	—	3.6	V
Analog power supply voltages	AVCC0*1		—	VCC	—	V
	AVSS0		—	0	—	V

Note 1. Connect AVCC0 to VCC. When the A/D converter and the D/A converter are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

Note 2. Low CL crystal cannot be used below VBATT = 1.8V.

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Table 53.4 I/O V_{IH}, V_{IL} (2 of 2)

Parameter					Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	IIC (except for SMBus)			V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	V
					V_{IL}	—	—	VCC × 0.3	
					ΔV_T	VCC × 0.05	—	—	
		CEC			V_{IH}	2.0	—	—	
					V_{IL}	—	—	0.8	
					ΔV_T	—	0.4	—	
		5 V-tolerant ports[*1 *5]			V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
					V_{IL}	—	—	VCC × 0.2	
					ΔV_T	VCC × 0.05	—	—	
		RTCIC0, RTCIC1, RTCIC2	When using the Battery Backup Function	When VBATT power supply is selected	V_{IH}	V_{BATT} × 0.8	—	V_{BATT} + 0.3	
					V_{IL}	—	—	V_{BATT} × 0.2	
					ΔV_T	V_{BATT} × 0.05	—	—	
				When VCC power supply is selected	V_{IH}	VCC × 0.8	—	Higher voltage either VCC + 0.3 V or V_{BATT} + 0.3 V	
					V_{IL}	—	—	VCC × 0.2	
					ΔV_T	VCC × 0.05	—	—	
			When not using the Battery Backup Function		V_{IH}	VCC × 0.8	—	VCC + 0.3	
					V_{IL}	—	—	VCC × 0.2	
					ΔV_T	VCC × 0.05	—	—	
		Other input pins[*2]			V_{IH}	VCC × 0.8	—	—	
					V_{IL}	—	—	VCC × 0.2	
					ΔV_T	VCC × 0.05	—	—	
	Ports	5 V-tolerant ports[*3 *5]			V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	V
					V_{IL}	—	—	VCC × 0.2	
		Other input pins[*4]			V_{IH}	VCC × 0.8	—	—	
					V_{IL}	—	—	VCC × 0.2	

Terminals for which ΔVt is not specified are not guaranteed to have hysteresis width. It is only guaranteed to be recognized as High if it is above VIHmin and Low if it is below VILmax.

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53.2.3 I/O I_{OH}, I_{OL}

The current flowing out of the MCU to the external circuitry.

The current flowing into the MCU from the external circuitry

Table 53.5 I/O I_{OH}, I_{OL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P000 to P010, P014, P015, P201	—	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
	Ports P205, P206, P407 to P415, P708 to P713, PB01 (total 18 pins)	Low drive[*1]	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive[*2]	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive[*3]	I_{OH}	—	—	–20	mA
			I_{OL}	—	—	20	mA
	Ports P100 to P107, P208 to P211, P214, P600, P601 (total 15 pins)	Low drive[*1]	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive[*2]	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive[*3]	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
		High speed high drive[*4]	I_{OH}	—	—	–20	mA
			I_{OL}	—	—	20	mA
	Other output pins[*5]	Low drive[*1]	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive[*2]	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive[*3]	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA

This is the average current over the MCU's operating cycle.

(Example) If the values are 1mA, 2mA and 3mA, the average value is 6mA/3 = Average 2mA

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The maximum allowable current value that can flow in per pin. If this value is exceeded, operation cannot be guaranteed and the LSI may be permanently damaged

Total current value of all MCU output pins.

Table 53.5 I/O I_{OH}, I_{OL} (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (max value per pin)	Ports P000 to P010, P014, P015, P201	—	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
	Ports P205, P206, P407 to P415, P708 to P713, PB01 (total 18 pins)	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–40	mA
			I_{OL}	—	—	40	mA
	Ports P100 to P107, P208 to P211, P214, P600, P601 (total 15 pins)	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA
		High speed high drive*4	I_{OH}	—	—	–40	mA
			I_{OL}	—	—	40	mA
	Other output pins*5	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA
Permissible output current (max value of total of all pins)	Maximum of all output pins		$\Sigma I_{OH\ (max)}$	—	—	–80	mA
			$\Sigma I_{OL\ (max)}$	—	—	80	mA

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. This is the value when high speed high driving ability is selected in the Port Drive Capability in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 5. Except for P200, which is an input port.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 μs.

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53.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 53.6 I/O V_{OH}, V_{OL}, and other characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
		V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
	IIC[*1]	V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1)
		V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC	V_{OH}	VCC – 0.5	—	—		I_{OH} = –1.0 mA
		V_{OL}	—	—	0.4		I_{OL} = 1.0 mA
	CEC	V_{OL}	—	—	0.6		I_{OL} = 2.1 mA
	Ports P205, P206, P407 to P415, P708 to P713, PB01 (total of 18 pins)[*2]	V_{OH}	VCC – 1.0	—	—		I_{OH} = –20 mA VCC = 3.3 V
		V_{OL}	—	—	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins	V_{OH}	VCC – 0.5	—	—		I_{OH} = –1.0 mA
		V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
Input leakage current	RES	$\lvert I_{in} \rvert$	—	—	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Port P200		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5 V-tolerant ports	$\lvert I_{TSI} \rvert$	—	—	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for port P200)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up MOS current	Ports P0 to PB	I_p	–300	—	–10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input capacitance	Ports P014, P015	C_{in}	—	—	16	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz Ta = 25°C
	USB_DP and USB_DM		—	—	12		
	USBHS_DP, USBHS_DM, and ports P400, P401, P511, P512		—	—	10		
	Other input pins		—	—	8		

Note 1. SCL0_A, SDA0_A, SCL1_A, SDA1_A (total 4 pins).
Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

For information under the test conditions which are not listed here, refer to the IBIS model.

Leakage current of terminals other than those described in the "Input Leakage Current" item.
The off state refer to the high impedance state.

Built-in pull-up resistor value can be calculated by using this value.

Pull-up resistor = voltage in use ÷ Ip

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Current consumption when all functions except BGO are in operation.

Current consumption value when BGO is not working and the clock to modules described in Module Stop Control Registers is supplied/stopped.

Current consumption value of each low power consumption mode. Refer to Low Power Consumption chapter for the peripheral state of each modes.
(Below is an example of RA6M5)

Table 10.2 Operating conditions of each low power mode (1 of 2)

Item	Sleep mode	Software Standby mode	Snooze mode	Deep Software Standby mode
Transition condition	WFI instruction while SBYCR.SSBY = 0	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 0	Snooze request trigger in Software Standby mode. SNZCR.SNZE=1.	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 1
Canceling method	All interrupts. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.
State after cancellation by an interrupt	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Reset state
State after cancellation by a reset	Reset state	Reset state	Reset state	Reset state
Main clock oscillator	Selectable	Stop	Selectable[*6]	Stop
Sub-clock oscillator	Selectable	Selectable	Selectable	Selectable
High-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Middle-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Low-speed on-chip oscillator	Selectable	Selectable	Selectable	Selectable[*9]
IWDT-dedicated on-chip oscillator	Selectable[*1]	Selectable[*1]	Selectable[*1]	Stop

53.2.5 Operating and Standby Current

Table 53.7 Operating and standby current (1 of 2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current[*1]	High-speed mode	Maximum[*2]		I_{CC}[*3]	—	—	143	mA	ICLK = 200 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 50 MHz PCLKD = 100 MHz FCLK = 50 MHz BCLK = 100 MHz
		Maximum (without USBHS)			—	—	130		
		CoreMark®[*5 *6]			—	22	—		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash[*4]		—	32	—		
			All peripheral clocks disabled, while (1) code executing from flash[*5 *6]		—	18	—		
		Sleep mode[*5 *6]			—	11	55		
		Increase during BGO operation	Data flash P/E		—	6	—		
			Code flash P/E		—	8	—		
	Low-speed mode[*5 *9]				—	1.9	—		ICLK = 1 MHz
	Subosc-speed mode[*5 *10]				—	1.7	—		ICLK = 32.768 kHz
	Software Standby mode		SNZCR.RXDREQEN = 1		—	—	40		—
			SNZCR.RXDREQEN = 0		—	2.1	—		—
	Deep Software Standby mode	Power supplied to Standby SRAM and USB resume detecting unit			—	16.9	131	μA	—
		Power not supplied to SRAM or USB resume detecting unit	Power-on reset circuit low power function disabled		—	11.8	33.7		—
			Power-on reset circuit low power function enabled		—	4.8	23.8		—
		Increase when the RTC and AGT are operating	When the low-speed on-chip oscillator (LOCO) is in use		—	4.5	—		—
			When a crystal oscillator for low clock loads is in use		—	1.2	—		—
			When a crystal oscillator for standard clock loads is in use		—	1.5	—		—
	RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)		When a crystal oscillator for low clock loads is in use		—	0.9	—		V_{BATT} = 1.8 V, VCC = 0 V
					—	1.3	—		V_{BATT} = 3.3 V, VCC = 0 V
			When a crystal oscillator for standard clock loads is in use		—	1.1	—		V_{BATT} = 1.8 V, VCC = 0 V
					—	1.8	—		V_{BATT} = 3.3 V, VCC = 0 V
	Inrush current on returning from Deep Software Standby mode		Inrush current[*7]	I_{RUSH}	—	160	—	mA	
			Energy of inrush current[*7]	E_{RUSH}	—	1.0	—	μC	

Required conditions to guarantee the specification.

Current consumption value for the low power modes

Differences in Typ/max are due to temperature, manufacturing variations, etc. (in particular due to temperature)

This is current consumption value in the RTC operation.
To calculate the current consumption during RTC operation in each mode, add this value.

This is the transient current observed upon recovery from Deep Software Standby mode. A temporary inrush current occurs, during which the current exceeds the steady-state level.

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Analog power supply current	During 12-bit A/D conversion		AI_{CC}	—	0.8	1.1	mA	—
	Temperature sensor			—	0.1	0.2	mA	—
	During D/A conversion (per unit)	Without AMP output		—	0.1	0.2	mA	—
		With AMP output		—	0.6	1.1	mA	—
	Waiting for A/D, D/A conversion (all units)			—	0.9	1.6	mA	—
	ADC12, DAC12 in standby modes (all units)*8			—	2	8	μA	—

Current consumption of an analog power supply.
The current is consumed to operate ADC12, DAC12, and Temperature sensor.

Current consumption during conversion by ADC12.
It is applied at the timing shown in the figure below.

Current consumption during conversion waiting by ADC12 and DAC12.
It is applied at the timing shown in the figure below.

Current consumption during conversion by DAC12.
It is applied at the timing shown in the figure below.

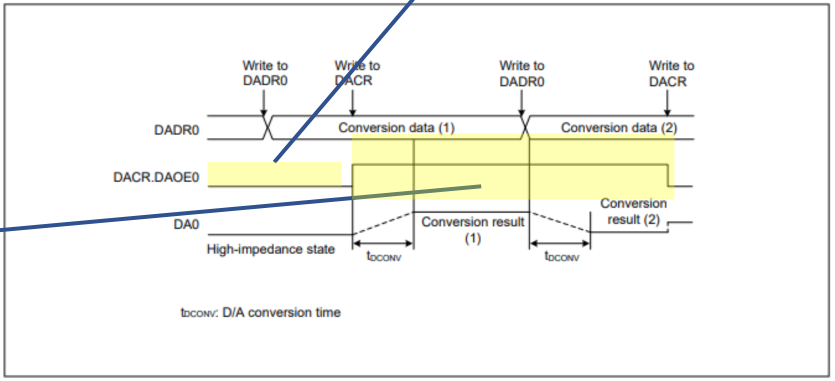

Figure 44.2 Example of DAC12 operation

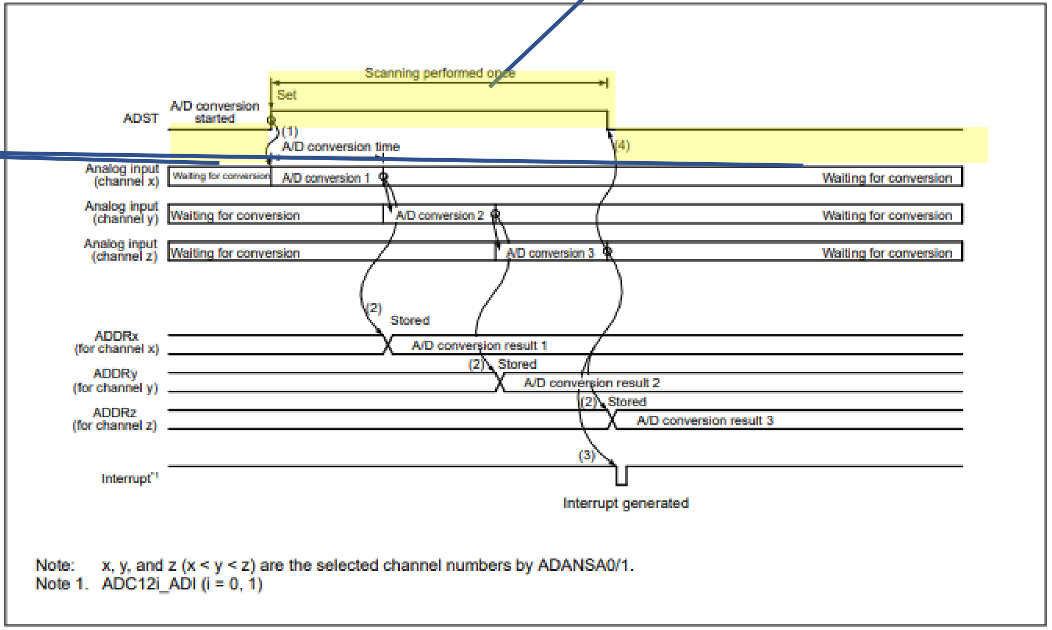

Figure 43.8 Example basic operation in single scan mode when the analog inputs (channel x to z) are selected

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Table 53.8 Coremark and normal mode current

Parameter			Symbol	Typ	Unit	Test conditions
Supply Current[*1]	Coremark		I_{CC}	107	µA/MHz	ICLK = 200MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = BCLK = 3.125MHz
	Normal mode	All peripheral clocks disabled, cache on, while (1) code executing from flash[*2]		104		
		All peripheral clocks disabled, cache off, while (1) code executing from flash[*2]		87		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

This is the current-consumption value measured during execution of the EEMBC-specified CoreMark program.
The current is primarily consumed by CPU operation.

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If the VCC rise time at power-on is faster than this, it is out of the guaranteed operating range. (0.0084ms/V)

if VCC rise time at power-on is slower than this, it is out of the guaranteed operating range. (20ms/V)

If VCC fall time when changing to VBATT is faster than this, it is out of the guaranteed operating range. (0.0084ms/V)
Sudden voltage drops when using VBATT can cause malfunction on return.

53.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 53.9 Rise and fall gradient characteristics

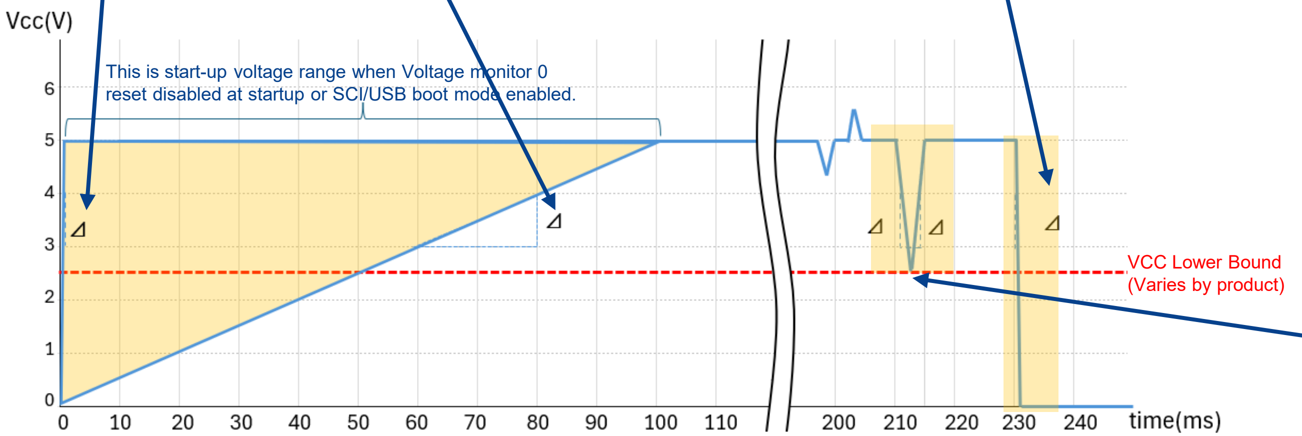
Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	—	20	ms/V	—
	Voltage monitor 0 reset enabled at startup		0.0084	—	—		—
	SCI/USB boot mode[*1]		0.0084	—	20		—
VCC falling gradient[*2]		SfVCC	0.0084	—	—	ms/V	—

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.
Note 2. This applies when VBATT is used.

Table 53.10 Rising and falling gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	—	—	10	kHz	Figure 53.6 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 53.6 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 53.6 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%



Example for VCC=5V

Allowable rising/falling slope of a voltage change (greater than ±10%).
If a voltage change is faster than this, it is out of the guaranteed operating range. (1ms/V)

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Table 53.11 Thermal Resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal Resistance	100-pin LQFP (PLQP0100KB-B)	θja	35.0	°C/W	JESD 51-2 and 51-7 compliant
	144-pin LQFP (PLQP0144KA-B)		33.0		
	176-pin LQFP (PLQP0176KB-C)		32.3		
	100-pin BGA (PLBG0100KB-A)		36.3		JESD 51-2 and 51-9 compliant
	144-pin BGA (PLBG0144KB-A)		36.3		
	176-pin BGA (PLBG0176GF-A)		35.4		
	100-pin LQFP (PLQP0100KB-B)	Ψjt	0.76	°C/W	JESD 51-2 and 51-7 compliant
	144-pin LQFP (PLQP0144KA-B)		0.63		
	176-pin LQFP (PLQP0176KB-C)		0.48		
	100-pin BGA (PLBG0100KB-A)		0.60		JESD 51-2 and 51-9 compliant
	144-pin BGA (PLBG0144KB-A)		0.60		
	176-pin BGA (PLBG0176GF-A)		0.52		

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

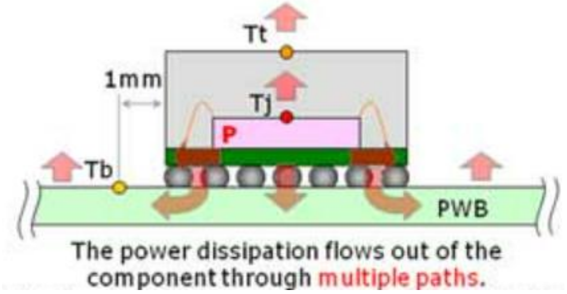
Thermal resistance according to JEDEC standard.
Please refer to below for details.

<Heat-dissipation Mechanism | Renesas>

Θja=(Tj-Ta)/P

Ψjt=(Tj-Tt)/P

Please refer to next pages for Tj calculation.



Ta: Temperature of a place not affected by a heat source

DC CHARACTERISTICS

53.2.7.2 Example of T_j calculation

Assumption :

- Package 176-pin LQFP : θja = 32.3 °C/W
- Ta = 100 °C
- I_{CC}max = 70 mA
- VCC = 3.5 V (VCC = AVCC0 = AVCC_USBHS = VCC_USB = VCC_USBHS)
- I_{OH} = 1 mA, V_{OH} = VCC – 0.5 V, 12 Outputs
- I_{OL} = 20 mA, V_{OL} = 1.0 V, 8 Outputs
- I_{OL} = 1 mA, V_{OL} = 0.5 V, 12 Outputs
- C_{in} = 8 pF, 32 pins, Input frequency = 10 MHz
- C_{load} = 30 pF, 32 pins, Output frequency = 10 MHz

Leakage current of IO = Σ (V_{OL} × I_{OL}) / Voltage + Σ ((VCC - V_{OH}) × I_{OH}) / Voltage
= (20 mA × 1 V) × 8 / 3.5 V + (1 mA × 0.5 V) × 12 / 3.5 V + ((VCC - (VCC - 0.5 V)) × 1 mA) × 12 / 3.5 V
= 45.7 mA + 1.71 mA + 1.71 mA
= 49.1 mA

Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
= ((8 pF × 32) × 10 MHz + (30 pF × 32) × 10 MHz) × 3.5 V
= 42.6 mA

Total power consumption = Voltage × (Leakage current + Dynamic current)
= (70 mA × 3.5 V) + (49.1 mA + 42.6 mA) × 3.5 V
= 566 mW (0.566 W)

Tj = Ta + θja × Total power consumption
= 100 °C + 32.3 °C/W × 0.566W
= 118.7 °C

AC CHARACTERISTICS AND OTHERS

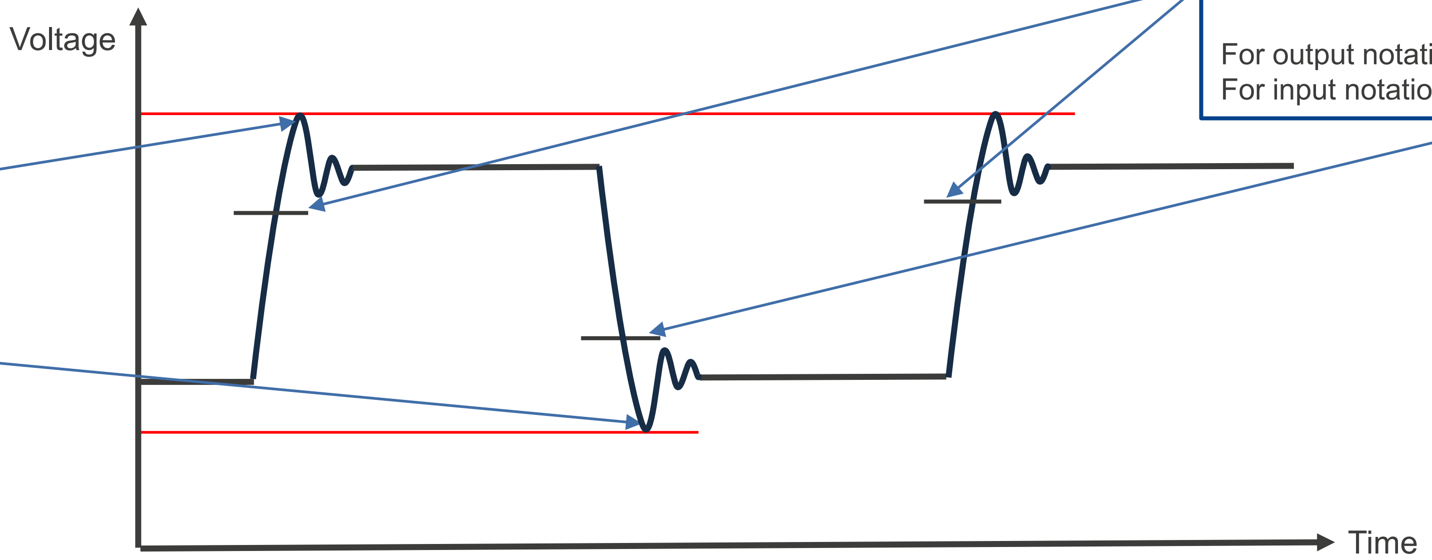
PREREQUISITES:

1. About Indication in Figures in AC Characteristics section

The base point of the horizontal line in the notation is basically as follows.
*If the expressions are different, they will be described separately.

For output notation: VOH or VOL
For input notation: VIH or VIL

Overshoot and undershoot should be kept within the absolute maximum rating.



Typical example in AC Characteristics

2. Notation of clocks in AC Specification section

Depending on the product, there are places where the clock notation is omitted.
For the exact clock name, refer to the Clock section of the hardware manual.

Example : Notation in AC Characteristics section : PCLK, notation in Clock section : PCLKB
Notation in AC Characteristics section : ADCLK, notation in Clock section : PCLKD

AC CHARACTERISTICS: CLOCK TIMING

This is the time until the oscillation of the resonator stabilizes. This value follows the matching evaluation by the resonator manufacturer.

It takes time to stabilize the oscillation after LOCO is oscillated (LOCOCR.LCSTP=0). Max. 60.4us is applied under the conditions in this table.

HOCO oscillator frequency can be selected from several options. For this device, the oscillator frequency of 16/18/20MHz can be selected. This table also shows the errors at each oscillation frequency.
In addition, note that the measurement conditions have temperature characteristics.
The accuracy according to this value is as follows.

Oscillation frequency (MHz)	Error (Ta = -20~105℃)	Error (Ta = -40~-20℃)
16	±2.4375%	±3%
18	±2.44%	±3%
20	±2.4 %	±3%

Period jitter indicates the temporal variation of the clock period.

Table 53.17 Clock timing except for sub-clock oscillator

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EBCLK pin output cycle time		t_{Bcyc}	20	—	—	ns	Figure 53.7
EBCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
EBCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
EBCLK pin output rise time		t_{Cr}	—	—	5.0	ns	
EBCLK pin output fall time		t_{Cf}	—	—	5.0	ns	
EXTAL external clock input cycle time		t_{EXcyc}	41.66	—	—	ns	Figure 53.8
EXTAL external clock input high pulse width		t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	15.83	—	—	ns	
EXTAL external clock rise time		t_{EXr}	—	—	5.0	ns	
EXTAL external clock fall time		t_{EXf}	—	—	5.0	ns	
Main clock oscillator frequency		f_{MAIN}	8	—	24	MHz	—
Main clock oscillation stabilization wait time (crystal)*1		$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 53.9
LOCO clock oscillation frequency		f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	60.4	μs	Figure 53.10
ILOCO clock oscillation frequency		f_{ILOCO}	13.5	15	16.5	kHz	—
MOCO clock oscillation frequency		f_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization wait time		t_{MOCOWT}	—	—	15.0	μs	—
HOCO clock oscillator oscillation frequency	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.960	16	16.040		–40 ≤ Ta ≤ 105°C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.955	18	18.045		
		f_{HOCO20}	19.950	20	20.050		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	—	—	64.7	μs	—
HOCO period jitter		—	—	±85	—	ps	—

AC CHARACTERISTICS: CLOCK TIMING

This is the time between enabling FLL (Frequency Correction) and stabilizing.
The frequency accuracy of the FLL is guaranteed only after the FLL is stabilized.

The output clock frequency range of the PLL frequency synthesizer.
Note that this is not the operation clock. In addition, please note that the input frequency range of the PLL frequency synthesizer is determined by the productNOTE.

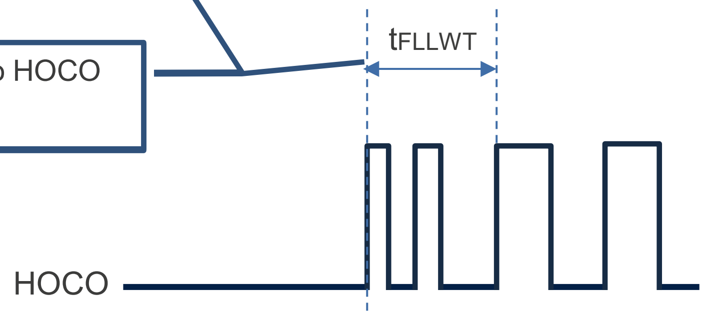
NOTE : Refer to the Clock Generation Circuit section in the User's Manual Hardware.

FLL stabilization wait time	t_{FLLWT}	—	—	1.8	ms	—
PLL clock frequency	f_{PLL}	120	—	200	MHz	—
PLL2 clock frequency	f_{PLL2}	120	—	240	MHz	—
PLL/PLL2 clock oscillation stabilization wait time	t_{PLLWT}	—	—	174.9	μs	Figure 53.11
PLL/PLL2 period jitter	—	—	±100	—	ps	—
PLL/PLL2 long term jitter	—	—	±300	—	ps	Term: 1μs, 10μs

It takes time to stabilize the oscillation (OSCSF. PLLSF=1) after PLL is oscillated (PLLCR. PLLSTP=0).Max. 174.9us is applied under the conditions in this table.

This is an indication of the timing variability of the clock period.
Period jitter takes the difference from the previous period for each cycle and statistically expresses the variation.
Long term jitter expresses the variation from the difference between the ideal and actual clock cycles.

Time from FLL Activation to HOCO Clock Stabilization



POWER-ON RESET CIRCUIT AND VOLTAGE DETECTION CIRCUIT CHARACTERISTICS

This is the voltage that cancels the internal reset when the power supply is started **(when VCC rises)**.
If the VCC exceeds the **V_{POR}**, it cancels the internal reset after the t_{POR} + t_{det} elapses. *1
Turn up VCC to working voltage before release.

This is the voltage that causes an internal reset when the **VCC is lowered**. (You can choose to enable/disable)
When enabled, the voltage can be selected from the n-level (in this case, two levels).
If VCC drops below **V_{det0}**, it will cancel the internal reset after t_{LVD0} + t_{det} has elapsed. *1
Turn up VCC to working voltage before release.

This voltage causes an interrupt or internal reset when **VCC rises or falls**. (You can choose to enable/disable)
If VCC falls below or above **V_{detn}**, it cancels the internal reset after t_{LVDn} + t_{det} elapses. (The timing changes depending on the value of LVDnCR0.RN)*1
Turn up VCC to working voltage before release.

Table 53.51 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b.	V_{POR}	2.5	2.6	2.7	V	Figure 53.88
		DPSBYCR.DEEPCUT[1:0] = 11b.		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 53.89
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 53.90
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 53.91
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	—	4.5	—	ms	Figure 53.88
	LVD0 reset time		t_{LVD0}	—	0.51	—		Figure 53.89
	LVD1 reset time		t_{LVD1}	—	0.38	—		Figure 53.90
	LVD2 reset time		t_{LVD2}	—	0.38	—		Figure 53.91
Minimum VCC down time*1			t_{VOFF}	200	—	—	μs	Figure 53.88, Figure 53.89
Response delay			t_{det}	—	—	200	μs	Figure 53.89 to Figure 53.91
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	—	—	10	μs	Figure 53.90, Figure 53.91
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	70	—	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for POR and LVD.

The internal reset hold time of the POR.
If the VCC exceeds V_{POR}, an internal unreset signal is issued after the **t_{POR}** + t_{det} elapses.

LVDn (n=0~2) internal reset retention time.
If the VCC exceeds V_{detn}, an internal unreset signal is issued after **t_{LVDn}** + t_{det} has elapsed.

This is the minimum amount of time that needs to be secured when the VCC falls below the detection voltage.
If the VCC exceeds the detected voltage after the VCC drops for less than **t_{VOFF}**, the voltage cannot be detected correctly when the VCC rises, and the power-on reset will not occur.

Voltage detection response delay time (the delay time until it reacts after voltage detection).
There is delay by **t_{det}** from when the voltage crosses the threshold to when the internal reset signal switching occurs.

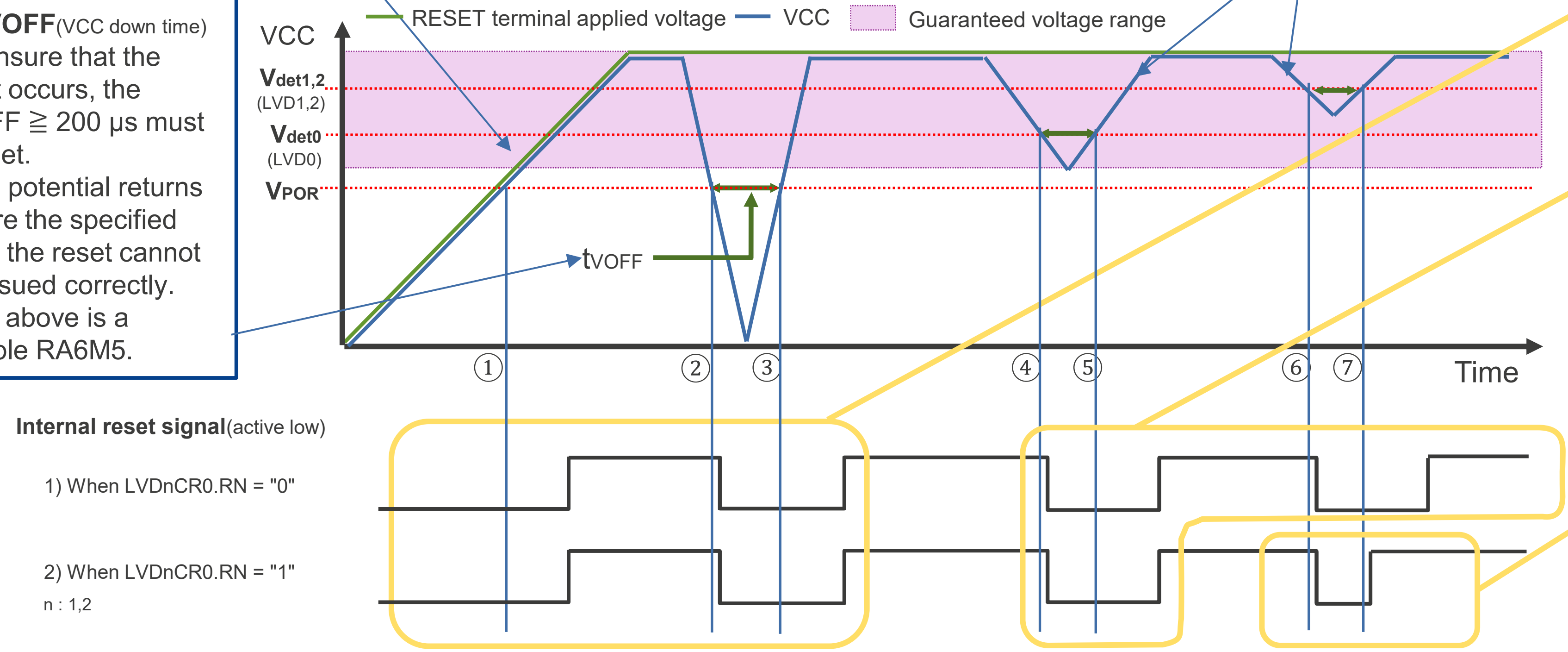
*1 See here for information on when a reset occurs/cancels.

SUPPLEMENTARY INFORMATION : POWER-ON RESET CIRCUIT AND VOLTAGE DETECTION CIRCUIT CHARACTERISTICS

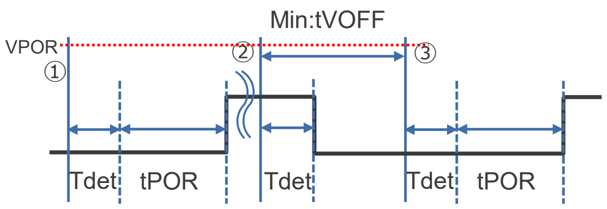
- To enable POR, apply more than VCC*1 to RESET pin.
  Note that if a capacitor is inserted to RESET pin to protect against noises, RESET pin rising potential will be slower than VCC rising potential, which means that the pin is judged to be a RESET pin reset, not a power-on reset.
  *1 : VCC must comply with the following rising slope (SrVCC).
  Example of RA6M5 case :
  Power supply startup with LVD0 : (0.0084ms/V) ≦ SrVCC ≦ (20ms/V)
  NOTE :The above is true when Voltage monitor 0 reset disabled at startup or SCI/USB boot mode enabled.

- Dt/dVCC
  Allowable rise/fall gradient for power supply fluctuation (fluctuation exceeding ±10%).
  If the power supply suddenly **fluctuates more than 1ms/V**, it will not be covered by the warranty.
  *The above is a sample RA6M5. There are some products that have no default.

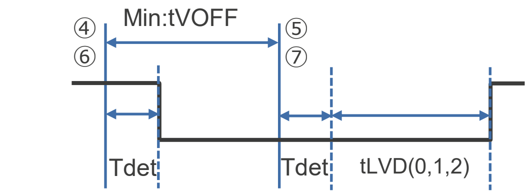
- **tVOFF**(VCC down time)
  To ensure that the reset occurs, the tVOFF ≧ 200 μs must be met.
  If the potential returns before the specified time, the reset cannot be issued correctly.
  *The above is a sample RA6M5.



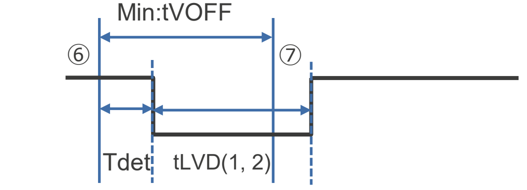
- Internal-reset operation when POR is applied



- Internal-reset operation by LVD0, 1, 2
  (LVD1,2 is when LVDnCR0.RN = "0")



- Internal-reset operation by LVD1, 2
  (When LVDnCR0.RN = "1")



* LVD1 and 2 can be reset by setting LVDnCR0.RN = "1".

NOTE :Various values in the statements and tables vary depending on the product. Refer to the electrical characteristics in the hardware manual of each product.
NOTE :For more information on the symbol symbols in the diagram, see here.

AC CHARACTERISTICS: RESET TIMING

This is the reset time required for internal initialization.
Be sure to input a reset signal that is greater than or equal to the value described in this manual. If the reset time is short, the MCU may not be initialized correctly, and operation may not be possible.

After the reset pin goes High, the reset process is required internally. After this time has elapsed, the reset is cancelled and the user program is executed.

53.3.3 Reset Timing

Table 53.19 Reset timing (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	0.7	—	—	ms	Figure 53.13
	Deep Software Standby mode	t_{RESWD}	0.6	—	—	ms	Figure 53.14
	Software Standby mode, Subosc-speed mode	t_{RESWS}	0.3	—	—	ms	
	All other	t_{RESW}	200	—	—	μs	
Wait time after RES cancellation		t_{RESWT}	—	37.3	41.2	μs	Figure 53.13

Table 53.19 Reset timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, TrustZone error reset, Cache parity error reset)	t_{RESW2}	—	324	397.7	μs	—

This is the waiting time that occurs after an internal reset due to the above factors.
After this time, the internal reset is cancelled, and the CPU starts handling the reset exception.

AC CHARACTERISTICS: LOW POWER MODE

Example)
If the system clock source is the main clock oscillator and the LOCO is in operation.

Total return time =
$t_{SBYMC} + t_{SBYOSCWT} - t_{SBYOSCWT} + 2n / f_{LOCO}$
Longest clock   Main clock

n: Number of weeks
f_{LOCO}: LOCO frequency

Please refer to the contents of Note 13 and the table below to find the return time.
Below is an example of the RA6M5.

Wakeup time	TYP		MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYMC	(MSTS[7:0]*32 + 3) / 0.262	35 + 18 / fICLK + 4n / fMAIN	(MSTS[7:0]*32 + 14 / 0.236	62 + 18 / fICLK + 4n / fMAIN	μs
tSBYPC	(MSTS[7:0]*32 + 34) / 0.262	35 + 18 / fICLK + 4n / fPLL	(MSTS[7:0]*32 + 45) / 0.236	62 + 18 / fICLK + 4n / fPLL	μs
tSBYEX	10	35 + 18 / fICLK + 4n / fEXMAIN	62	62 + 18 / fICLK + 4n / fEXMAIN	μs
tSBYPE	135	35 + 18 / fICLK + 4n / fPLL	192	62 + 18 / fICLK + 4n / fPLL	μs
tSBYSC	0	35 + 18 / fICLK + 4n / fSUB	0	62 + 18 / fICLK + 4n / fSUB	μs
tSBYLO	0	35 + 18 / fICLK + 4n / fLOCO	0	62 + 18 / fICLK + 4n / fLOCO	μs
tSBYHO	20	35 + 18 / fICLK + 4n / fHOCO	67	62 + 18 / fICLK + 4n / fHOCO	μs
tSBYPH	140	35 + 18 / fICLK + 4n / fPLL	202	62 + 18 / fICLK + 4n / fPLL	μs
tSBYMO	0	35 + 18 / fICLK + 4n / fMOCO	0	62 + 18 / fICLK + 4n / fMOCO	μs

53.3.4 Wakeup Timing

Table 53.20 Timing of recovery from low power modes (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}*13	—	2.1	2.4	ms	Figure 53.15 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}*13	—	2.2	2.6	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}*13	—	45	125	μs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}*13	—	170	255	μs	
	System clock source is sub-clock oscillator*6 *11		t_{SBYSC}*13	—	0.7	0.8	ms	
	System clock source is LOCO*7 *11		t_{SBYLO}*13	—	0.7	0.9	ms	
	System clock source is HOCO clock oscillator*8		t_{SBYHO}*13	—	55	130	μs	
	System clock source is PLL with HOCO*9		t_{SBYPH}*13	—	175	265	μs	
	System clock source is MOCO clock oscillator*10		t_{SBYMO}*13	—	35	65	μs	

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest tSBYOSCWT in the active oscillators - tSBYOSCWT for the system clock + 2 LOCO cycles (when LOCO is operating) + Subosc is oscillating and MSTPC0 = 0 (CAC module stop))

Note 13. The recovery time can be calculated with the equation of tSBYOSCWT + tSBYSEQ. And they can be determined with the following value and equation. For n, the greatest value is selected from among the internal clock division settings.

AC CHARACTERISTICS: NOISE FILTER

The pulse widths shown in this table are for normal mode operation.
In software standby mode, a pulse width of Min = 200us is required.

If you switch the clock source to something other than PCLKB and use a filter, the 4 clocks of the switched clock source will be added to the pulse width shown in the table.

53.3.5 NMI and IRQ Noise Filter

Table 53.21 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \le 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \le 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

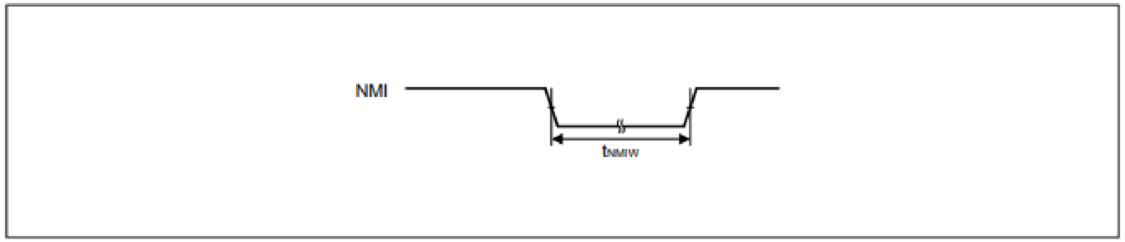


Figure 53.18 NMI interrupt input timing

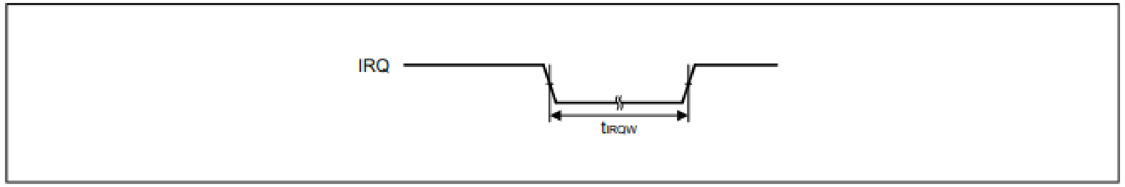


Figure 53.19 IRQ interrupt input timing

AC CHARACTERISTICS: BUS TIMING

Required conditions to guarantee the following specifications.
Pay special attention when selecting the output load conditions and drive capability. If the normal drive output is selected for bus driving, the timing may not be long enough and access may not be performed correctly.

53.3.6 Bus Timing

Table 53.22 Bus timing

Condition:
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF.
EBCLK: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
Others: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	—	12.5	ns	Figure 53.22 to Figure 53.25
Byte control delay	t_{BCD}	—	12.5	ns	
CS delay	t_{CSD}	—	12.5	ns	
ALE delay time	t_{ALED}	—	12.5	ns	
RD delay	t_{RSD}	—	12.5	ns	
Read data setup time	t_{RDS}	12.5	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR/WRn delay	t_{WRD}	—	12.5	ns	
Write data delay	t_{WDD}	—	12.5	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT setup time	t_{WTS}	12.5	—	ns	Figure 53.26
WAIT hold time	t_{WTH}	0	—	ns	

As for this value, it does not become 0 or less.

AC CHARACTERISTICS: BUS TIMING

A0~A15 is output from the address bus/data bus (A0/D0~A15/D15). After A16, it is output from the address bus of Axx.

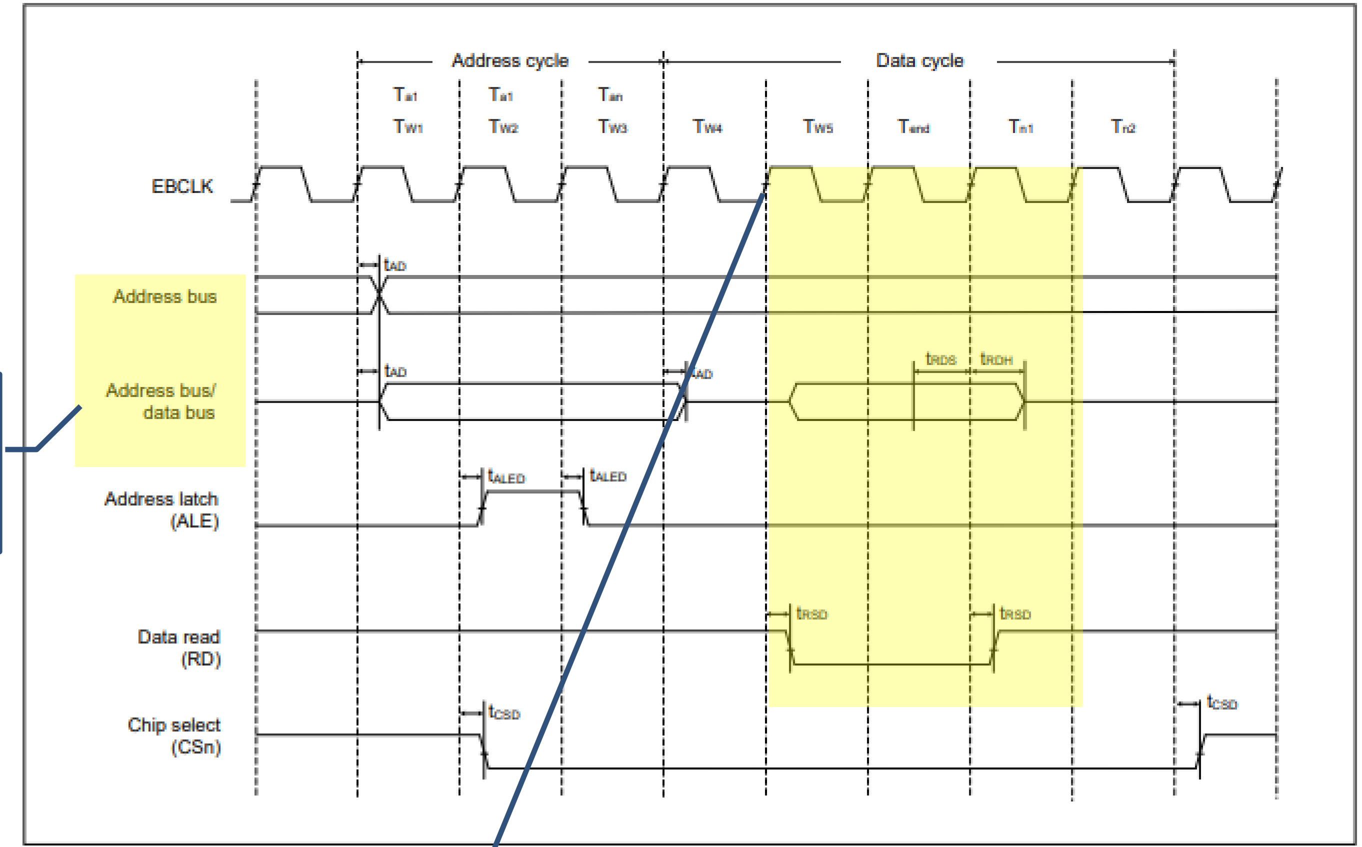


Figure 53.20 **Address/data multiplexed bus read access timing**

Read timing is the rising edge of EBCLK's Tend.

AC CHARACTERISTICS: BUS TIMING

WAIT cycling is inserted synchronously with the inner EBCLK. When EBCLK pin output is set to 1/2 of the internal BCLK clock, note that the assertion/negation timing of the control signals may change not only at the rising timing but also at the falling timing of the EBCLK pin depending on the number of WAITs set.

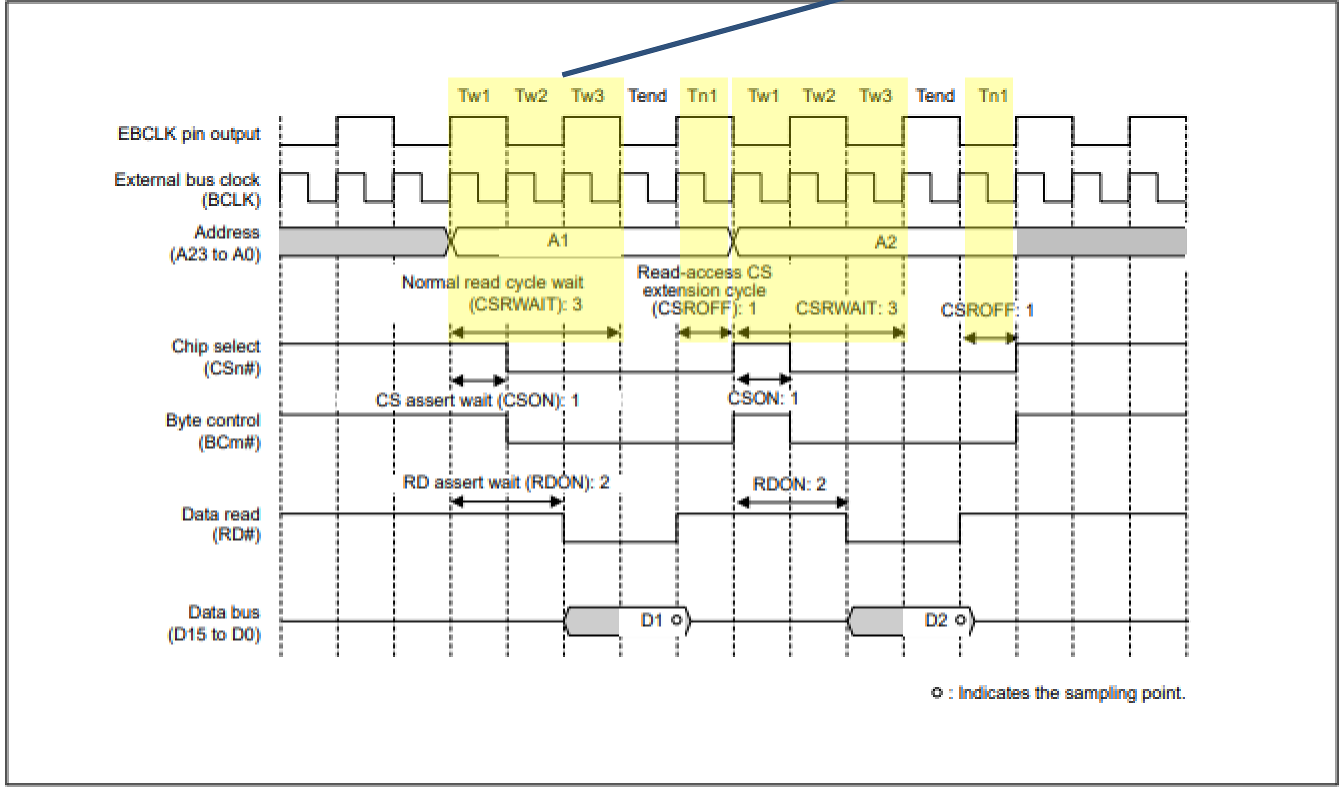


Figure 14.15 Example of normal read operation when BCLK/2 is selected in the EBCLK Pin Output Select Bit and two rounds of bus access are generated in response to a single transfer request (n = 0 to 7, m = 0 to 1)

AC CHARACTERISTICS: I/O PORTS TIMING

53.3.7 I/O Ports, POEG, GPT, AGT, and ADC12 Trigger Timing

Table 53.23 I/O ports, POEG, GPT, AGT, and ADC12 trigger timing (1 of 2)

GPT32 Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 53.27
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 53.28
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 53.29
		Dual edge		2.5	—		
	GTIOCxY output skew (x = 0 to 3, Y = A or B)	Middle drive buffer	t_{GTISK} [*1]	—	4	ns	Figure 53.30
		High drive buffer		—	4		
	GTIOCxY output skew (x = 4 to 9, Y = A or B)	Middle drive buffer		—	4		
		High drive buffer		—	4		
	GTIOCxY output skew (x = 0 to 9, Y = A or B)	Middle drive buffer		—	6		
		High drive buffer		—	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	—	5	ns	Figure 53.31

The time varies depending on the frequency of the peripheral module clock (PCLK), so please check it together with the set PCLK period.
In the example shown, t_{PBcyc} x 1.5 is the input data pulse width.

Skew represents the time difference between signals when transmitting multiple signals simultaneously.

AC CHARACTERISTICS: I/O PORTS TIMING

Table 53.23 I/O ports, POEG, GPT, AGT, and ADC12 trigger timing (2 of 2)

GPT32 Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
AGT	AGTIO, AGTEE input cycle	t_{ACYC}*2	100	—	ns	Figure 53.32
	AGTIO, AGTEE input high width, low width	t_{ACKWH}, t_{ACKWL}	40	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle	t_{ACYC2}	62.5	—	ns	
ADC12	ADC12 trigger input pulse width	t_{TRGW}	1.5	—	t_{Pcyc}	Figure 53.33

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

The reference clock is the peripheral module clock supplied to I/O port. Check in the Clock Generation Circuit chapter.
The RA6M5 example uses the following clocks as a reference:
ADC12 : PCLKA
AGT : PCLKB

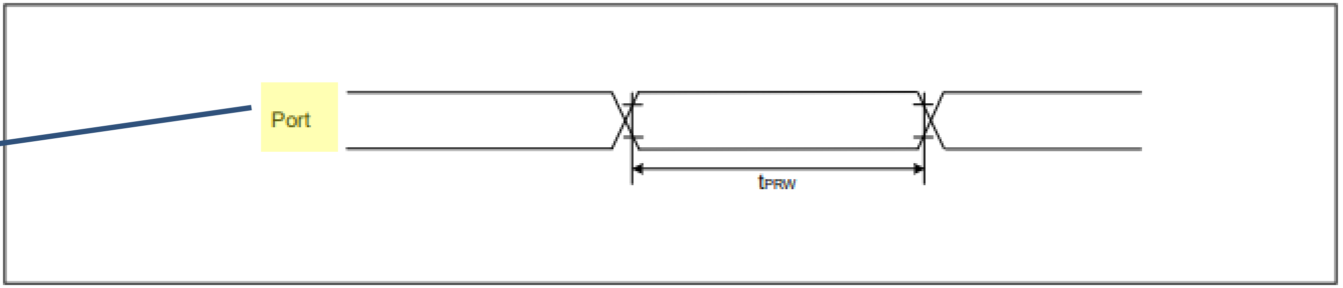


Figure 53.27 I/O ports input timing

AC CHARACTERISTICS: SPI TIMING

To achieve the maximum bit rate Please considering carefully the specifications of the bus driver / bus interface LSI , such as settup and hold time , and the bus configuration (bus loading) to make sure the maimum bit rate can be achieved reliably.

53.3.10 SPI Timing

Table 53.28 SPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 53.42
		Slave		4	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})$ / 2 – 3	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})$ / 2 – 3	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Slave		—	1	μs	
	Data input setup time	Master	t_{SU}	4	—	ns	Figure 53.43 to Figure 53.48
		Slave		5	—		
	Data input hold time	Master (PCLKA division ratio set to 1/2)	t_{HF}	0	—	ns	
		Master (PCLKA division ratio set to a value other than 1/2)	t_H	t_{Pcyc}	—		
		Slave	t_H	20	—		
	SSL setup time	Master	t_{LEAD}	$N \times t_{SPcyc} - 10^{*1}$	$N \times t_{SPcyc} + 100^{*1}$	ns	
		Slave		$4 \times t_{Pcyc}$	—	ns	
	SSL hold time	Master	t_{LAG}	$N \times t_{SPcyc} - 10^{*2}$	$N \times t_{SPcyc} + 100^{*2}$	ns	
		Slave		$4 \times t_{Pcyc}$	—	ns	
	Data output delay	Master	t_{OD1}	—	6.3	ns	
			t_{OD2}		6.3		
		Slave	t_{OD}	—	20		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	—	5	ns	
		Input		—	1	μs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	—	5	ns	
		Input		—	1	μs	
	Slave access time		t_{SA}	—	25	ns	Figure 53.47 and Figure 53.48
	Slave output release time		t_{REL}	—	25		

Note: t_{Pcyc}: PCLKA cycle.

AC CHARACTERISTICS: QSPI TIMING

53.3.11 QSPI Timing

Table 53.29 QSPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
QSPI	QSPCK clock cycle	t_{QScyc}	2	48	t_{Pcyc}	Figure 53.49
	QSPCK clock high pulse width	t_{QSWH}	$t_{QScyc} \times 0.4$	—	ns	
	QSPCK clock low pulse width	t_{QSWL}	$t_{QScyc} \times 0.4$	—	ns	
	Data input setup time	t_{Su}	10	—	ns	Figure 53.50
	Data input hold time	t_{IH}	0	—	ns	
	QSSL setup time	t_{LEAD}	$(N + 0.5) \times t_{Qscyc} - 5^{*1}$	$(N + 0.5) \times t_{Qscyc} + 100^{*1}$	ns	
	QSSL hold time	t_{LAG}	$(N + 0.5) \times t_{Qscyc} - 5^{*2}$	$(N + 0.5) \times t_{Qscyc} + 100^{*2}$	ns	
	Data output delay	t_{OD}	—	4	ns	
	Data output hold time	t_{OH}	–3.3	—	ns	
	Successive transmission delay	t_{TD}	1	16	t_{QScyc}	

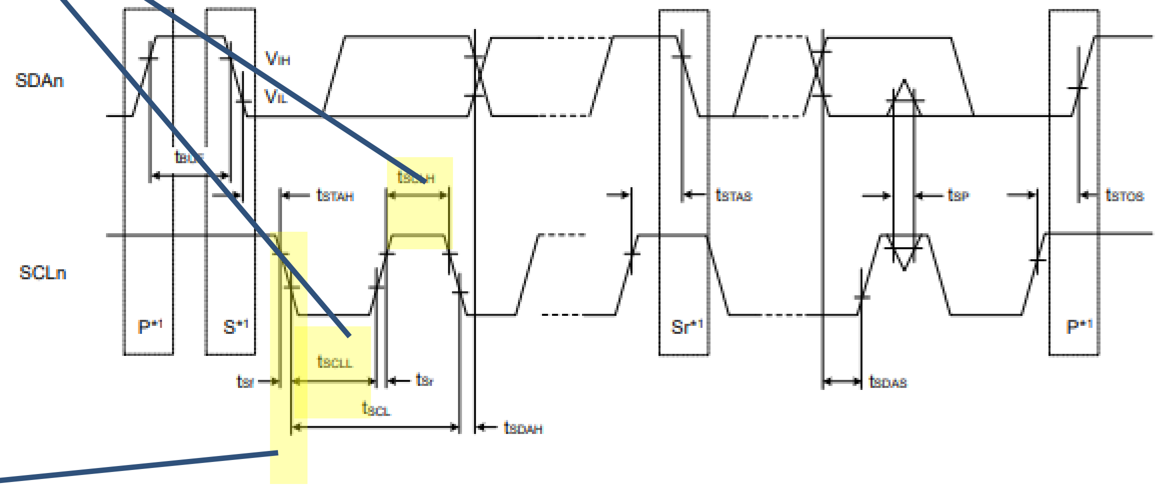
Note: t_{Pcyc}: PCLKA cycle.
Note 1. N is set to 0 or 1 in SFMSLD.
Note 2. N is set to 0 or 1 in SFMSHD.

In the case of continuous transfer, this is the free time from the end of the transfer to the start of the next transfer.

AC CHARACTERISTICS: IIC TIMING

The upper/lower limit of tSCLH,tSCLL differs depending on the communication speed of IIC. For more information, please refer to the "IIC Bus Specifications" proposed by NXP.

As the rise time varies depending on the load conditions, observe the actual output waveform after mounting the board and check.



Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 53.57 **I²C bus interface input/output timing**

A/D CONVERSION CHARACTERISTICS

Refer to the next page for the terms of A/D conversion.

Please also refer to the Hardware Manual "Analog input sampling time and scan conversion time (comparison time)".

53.5 ADC12 Characteristics

Table 53.44 A/D conversion characteristics for unit 0

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	—	50	MHz	—
Analog input capacitance			—	—	30	pF	—
Quantization error			—	±0.5	—	LSB	—
Resolution			—	—	12	Bits	—
High-precision high-speed channels (AN000 to AN005)	Conversion time*1 (operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.52 (0.26)*2	—	—	μs	Sampling in 13 states
		Max. = 400 Ω	0.40 (0.14)*2	—	—	μs	Sampling in 7 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
High-precision normal-speed channels (AN006 to AN010, AN012, AN013)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.92 (0.66)*2	—	—	μs	Sampling in 33 states
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of pins AN000 to AN010, AN012, AN013 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0/VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note: When both unit0 and unit1 are used, do not select the following analog input combinations at the same time except the interleave function. If selected, values might not fall within the indicated ranges.

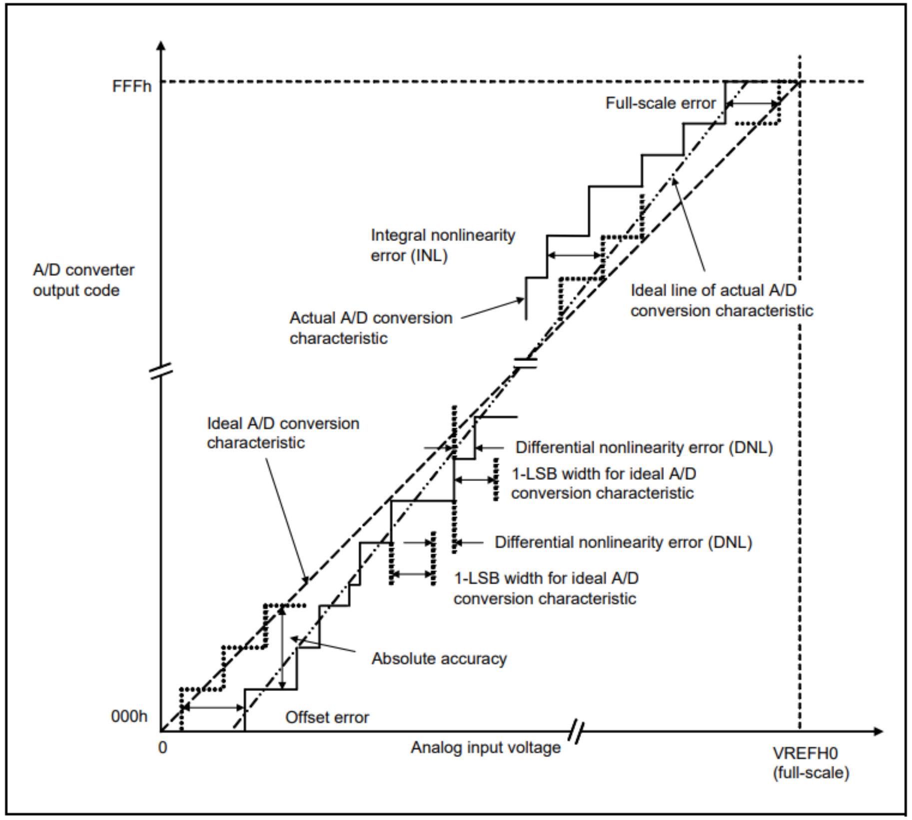
- AN100 and AN000 or AN001 or AN002
- AN101 and AN000 or AN001 or AN002 or AN003
- AN102 and AN000 or AN001 or AN002 or AN003 or AN004

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

EXPLANATION OF A/D CONVERTER-CHARACTERISTIC TERMINOLOGY

- **Absolute accuracy**
  Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.
  If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.
- **Integral nonlinearity error (INL)**
  Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.
- **Differential nonlinearity error (DNL)**
  Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.
- **Offset error**
  Offset error is the difference between a transition point of the ideal first output code and the actual first output code.
- **Full-scale error**
  Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.



D/A CONVERSION CHARACTERISTICS

0V~0.2V and AVCC1-0.2~AVCC are not guaranteed, although the voltage is output.

This is the buffer characteristic when the low-capacitance impedance buffer is enabled.

Some products have no buffer.

In the case of buffered output, DNL and INL characteristics are guaranteed rather than absolute accuracy.

Output resistor (RO) in D/A converters.
When external buffers are connected, a voltage-drop occurs due to the output-resistance inside D/A converter.
The actual Vr are as follows.
Vr = Output voltage*R/ (R + RO)

Therefore, in order to bring Vr closer to the output voltage,
The external resistance (R) must be greater than RO (e.g., 100 times or more).

53.6 DAC12 Characteristics

Table 53.48 D/A conversion characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bits	—
Without output amplifier					
Absolute accuracy	—	—	±24	LSB	Resistive load 2 MΩ
INL	—	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	—	±1.0	±2.0	LSB	—
Output impedance	—	8.5	—	kΩ	—
Conversion time	—	—	3	μs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	—	VREFH	V	—
With output amplifier					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
Conversion time	—	—	4.0	μs	—
Resistive load	5	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
Output voltage range	0.2	—	VREFH – 0.2	V	—

TSN CHARACTERISTICS

The temperature can be calculated using this value. However, this value is only an average value across all LSI , and there are individual differences between each device.

If you wish to perform more accurate temperature measurement, we recommend that you perform two-point calibration for each chip and calculate the slope individually.

Average value of temperature sensor output potential when ambient temperature is 25°C. The temperature can be calculated using this value. However, this value is only an average value across all LSI, and there are individual differences between each device..

If you want to make more accurate temperature measurements, we recommend that you make actual measurements for each chip and use that value.

This temperature sensor can measure the temperature inside the chip.
Since there is a variation between individual values of this temperature sensor, the temperature slope and output potential of this temperature sensor characteristics are average (typical).
If you want to measure the temperature with higher accuracy, perform trial measurements of 1 and 2 points of temperature for each individual, and calculate the temperature slope and output potential.
For the calculation method, please refer to the How to use the temperature sensor in the Temperature Sensors chapter.

53.7 TSN Characteristics

Table 53.49 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.0	—	°C	—
Temperature slope	—	—	4.0	—	mV/°C	—
Output voltage (at 25 °C)	—	—	1.24	—	V	—
Temperature sensor start time	t_{START}	—	—	30	µs	—
Sampling time	—	4.15	—	—	µs	—

This is the stable waiting time of the output (reference voltage) of the temperature sensor.
After starting up the temperature sensor, wait for the temperature sensor startup time before starting the A/D conversion.
The temperature sensor activation signal differs for each microcomputer. Check the temperature sensor chapter.

BATTERY BACKUP FUNCTION CHARACTERISTICS

53.10 VBATT Characteristics

Table 53.52 Battery backup function characteristics

Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VBATT = 1.65 to 3.6 V*1

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 53.92
Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop	V_{BATTSW}	2.70	—	—	V	
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	—	—	μs	
VBATT low voltage detection level	$V_{battldet}$	1.8	1.9	2.0	V	Figure 53.93
Minimum VBATT down time	$t_{BATTOFF}$	200	—	—	μs	
Response delay	$t_{BATTdet}$	—	—	200	μs	
VBATT monitor operation stabilization time (after VBATTMNSELR.VBATTMNSEL is changed to 1)	$t_{d(E-A)}$	—	—	20	μs	
VBATT current increase (when VBATTMNSELR.VBATTMNSEL is 1 compared to the case that VBATTMNSELR.VBATTMNSEL is 0)	$I_{VBATTSEL}$	—	140	350	nA	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

Note 1. Low CL crystal cannot be used below VBATT = 1.8 V.

This is the voltage applied to the VBATT terminal when switching the power supply from VCC to Vbatt. If the condition **Vbatt < 2.7V** is met during the time that VCC ia falling, it will not transition to the battery backup.

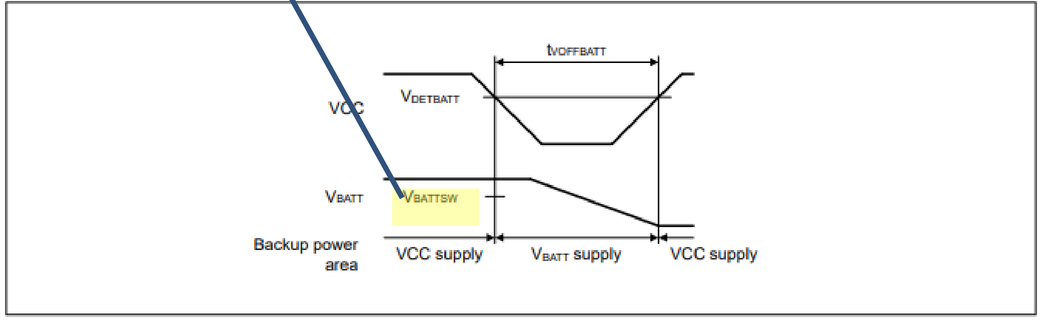


Figure 53.92 Battery backup function characteristics

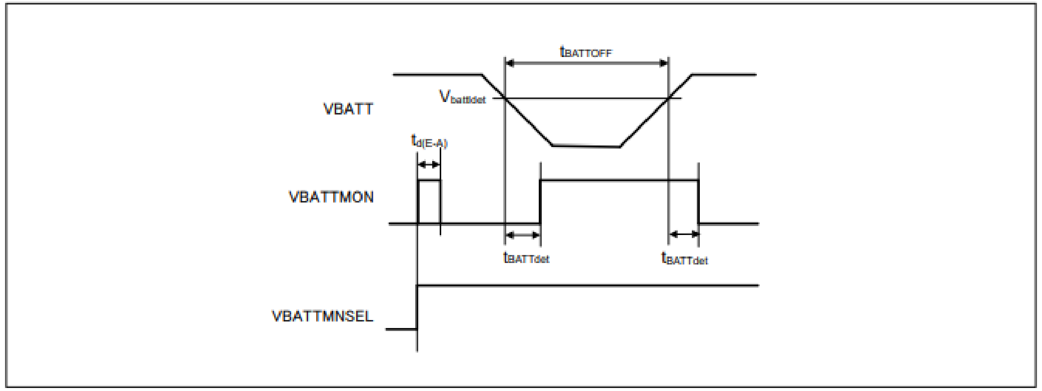


Figure 53.93 Battery backup function characteristics

FLASH MEMORY CHARACTERISTICS

Required conditions to guarantee the following specifications.

The range of typ/max values depends on individual differences in the product, temperature, number of writes, etc.

The target area of the program/erase count is for each area of the program unit.
For example, if the program unit is 4B for a 32 KB area, it is possible to achieve more writes than described as a whole by staggering the areas instead of writing to the same area continuously.

53.12 Flash Memory Characteristics

53.12.1 Code Flash Memory Characteristics

Table 53.54 Code flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ[*6]	Max	Min	Typ[*6]	Max		
Programming time N_{PEC} ≤ 100 times	128-byte	t_{P128}	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t_{P8K}	—	49	176	—	22	80	ms	
	32-KB	t_{P32K}	—	194	704	—	88	320	ms	

Table 53.54 Code flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ[*6]	Max	Min	Typ[*6]	Max		
Programming time N_{PEC} > 100 times	128-byte	t_{P128}	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t_{P8K}	—	60	212	—	27	96	ms	
	32-KB	t_{P32K}	—	234	848	—	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	—	78	216	—	43	120	ms	
	32-KB	t_{E32K}	—	283	864	—	157	480	ms	
Erasure time N_{PEC} > 100 times	8-KB	t_{E8K}	—	94	260	—	52	144	ms	
	32-KB	t_{E32K}	—	341	1040	—	189	576	ms	
Reprogramming/erasure cycle[*4]		N_{PEC}	10000[*1]	—	—	10000[*1]	—	—	Times	
Suspend delay during programming		t_{SPD}	—	—	264	—	—	120	μs	
Programming resume time		t_{PRT}	—	—	110	—	—	50	μs	
First suspend delay during erasure in suspend priority mode		t_{SESD1}	—	—	216	—	—	120	μs	
Second suspend delay during erasure in suspend priority mode		t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Suspend delay during erasure in erasure priority mode		t_{SEED}	—	—	1.7	—	—	1.7	ms	
First erasing resume time during erasure in suspend priority mode[*5]		t_{REST1}	—	—	1.7	—	—	1.7	ms	
Second erasing resume time during erasure in suspend priority mode		t_{REST2}	—	—	144	—	—	80	μs	
Erasing resume time during erasure in erasure priority mode		t_{REET}	—	—	144	—	—	80	μs	
Forced stop command		t_{FD}	—	—	32	—	—	20	μs	
Data hold time[*2]		t_{DRP}	10[*2 *3]	—	—	10[*2 *3]	—	—	Years	
			30[*2 *3]	—	—	30[*2 *3]	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3V and room temperature.

DATA FLASH CHARACTERISTICS

53.12.2 Data Flash Memory Characteristics

Table 53.55 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Required conditions to guarantee the following specifications.

The range of typ/max values depends on individual differences in the product, temperature, number of writes, etc.

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ[*6]	Max	Min	Typ[*6]	Max		
Programming time	4-byte	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
	8-byte	t_{DP8}	—	0.38	4.0	—	0.17	1.8		
	16-byte	t_{DP16}	—	0.42	4.5	—	0.19	2.0		
Erasure time	64-byte	t_{DE64}	—	3.1	18	—	1.7	10	ms	
	128-byte	t_{DE128}	—	4.7	27	—	2.6	15		
	256-byte	t_{DE256}	—	8.9	50	—	4.9	28		
Blank check time	4-byte	t_{DBC4}	—	—	84	—	—	30	μs	
Reprogramming/erasure cycle[*1]		N_{DPEC}	125000[*2]	—	—	125000[*2]	—	—	—	
Suspend delay during programming	4-byte	t_{DSPD}	—	—	264	—	—	120	μs	
	8-byte		—	—	264	—	—	120		
	16-byte		—	—	264	—	—	120		
Programming resume time		t_{DPRT}	—	—	110	—	—	50	μs	
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	—	—	216	—	—	120	μs	
	128-byte		—	—	216	—	—	120		
	256-byte		—	—	216	—	—	120		

The target area of the program/erase count is for each area of the program unit.
For example, if the program unit is 4B for a 32 KB area, it is possible to achieve more writes than described as a whole by staggering the areas instead of writing to the same area continuously.

DATA FLASH CHARACTERISTICS

Table 53.55 Data flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	—	—	300	—	—	300	μs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	—	—	300	—	—	300	μs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
First erasing resume time during erasure in suspend priority mode*5		t_{DREST1}	—	—	300	—	—	300	μs	
Second erasing resume time during erasure in suspend priority mode		t_{DREST2}	—	—	126	—	—	70	μs	
Erasing resume time during erasure in erasure priority mode		t_{DREET}	—	—	126	—	—	70	μs	
Forced stop command		t_{FD}	—	—	32	—	—	20	μs	
Data hold time*3		t_{DRP}	10*3 *4	—	—	10*3 *4	—	—	Year	
			30*3 *4	—	—	30*3 *4	—	—		Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3 V and room temperature.

The target area of the program/erase count is for each area of the program unit.
For example, if the program unit is 4B for a 32 KB area, it is possible to achieve more writes than described as a whole by staggering the areas instead of writing to the same area continuously.

If the specified number of programs/erases is exceeded, the write/erase time will be longer and read errors will be more likely to occur.

REVISION HISTORY

Revision	Date	Page	Contents
1.00	April, 2026	-	1st version issued.