RA FAMILY
HARDWARE MANUAL GUIDE (PERIPHERAL FUNCTIONS)

APRIL, 2026

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PURPOSE OF THIS DOCUMENT

- This manual is an easy-to-understand summary of each peripheral functional chapter of the hardware manual, using the RA4L1 and RA6M5 as examples.
- The purpose of this document is to provide a much deeper understanding of the functions by using it with the hardware manual.
- For more detailed usage instructions, please refer to the application notes provided on each page.
- This document does not cover all the information described in the manual. For detailed information such as precautions for each function, please check the hardware manual for the product you want to use.

LIST OF PERIPHERAL FUNCTIONS

This document explains the following peripheral functions. The abbreviations in parentheses indicate function names.
The peripheral functions described in this material will continue to be added.

Please also refer to the Hardware Manual Guide: Electrical Characteristics (R01TU0457EJ0100)

LOW POWER CONSUMPTION

“LOW POWER CONSUMPTION” FUNCTION BY PRODUCT GROUP

- The “Low Power Consumption” functions for each product are shown in the table below.

Product	Sleep	Software Standby	Deep Software Standby	Snooze	High-speed	Middle-speed	Low-speed	Subosc-speed
RA4L1 groups	✓	✓	—	✓	✓	✓	✓	✓
RA6M5 groups	✓	✓	✓	✓	✓	—	✓	✓

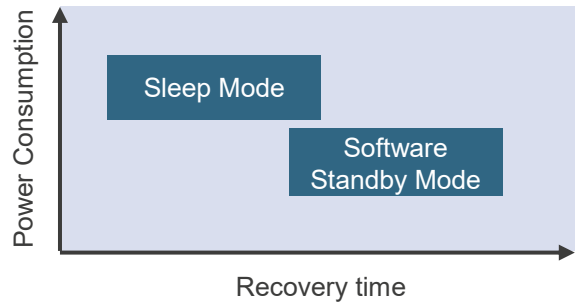
* Some products may not support certain modes, so please refer to the hardware section of the user's manual for each product for details.

OVERVIEW
“LOW POWER CONSUMPTION” FUNCTION OF RA4L1 GROUP

“Stopped (Retained)” means that internal register values are retained and internal operations are suspended.
“Stopped (Undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

Low power consumption mode	CPU	Oscillator / Power management				Peripheral modules						Memory		I/O Port
		Main clock	HOCO MOCO PLL	LOCO Sub-clock RTC LVD	POR	IWDT I3C AGT UARTA ACMPLP SLCDC IRQ NMI	WDT	USBFS	IIC0	ADC12 DAC12 CTSU DTC SCI0 DOC ELC	Other	SRAM	Flash memory	
Sleep	Stop (retained)	Selectable	Selectable	Selectable	Operating	Selectable	Selectable	Selectable	Selectable	Selectable	Selectable	Selectable	Operating	Operating
Software Standby	Stop (retained)	Stop	Stop	Selectable	Operating	Selectable	Stop (retained)	Stop (retained) *2	Selectable	Stop (retained)	Stop (retained)	Stop (retained)	Stop (retained)	Stop (retained)
Snooze*1	Stop (retained)	Selectable	Selectable	Selectable	Operating	Selectable	Stop (retained)	Operation prohibited *2	Selectable *3	Selectable	Operation prohibited	Selectable	Stop (retained)	Operating

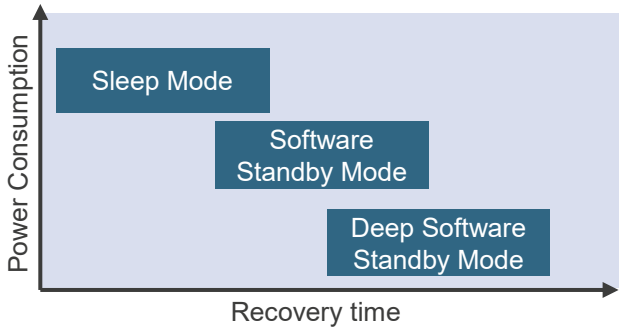
*1 : For details of snooze mode, see this page.
*2 : USB resumption detection is possible.
*3 : Wake-up interrupt operation only.



OVERVIEW
“LOW POWER CONSUMPTION” FUNCTION OF RA6M5 GROUP

“Stopped (Retained)” means that internal register values are retained and internal operations are suspended.
“Stopped (Undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

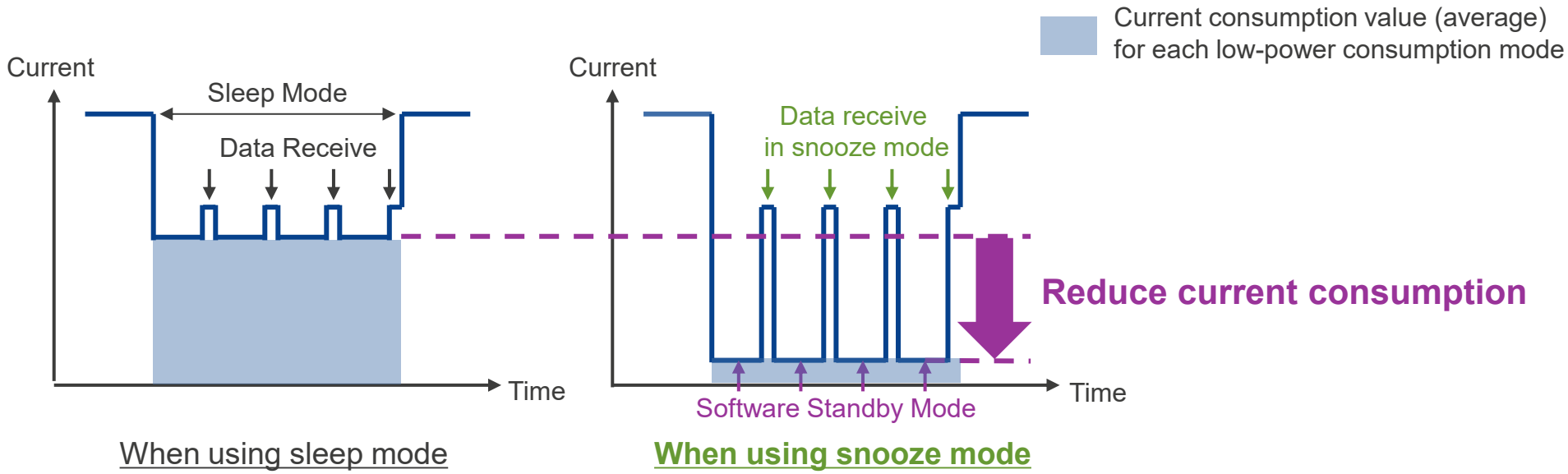
Low power consumption mode	CPU	Oscillator / Power management				Peripheral modules						Memory			I/O Port
		Main-clock HOCO MOCO PLL PLL2	LOCO Sub-clock RTC LVD AGT	POR	EBCLK	IWDT IIC0 IRQ	NMI IRQ-DS	WDT	ADC12 DAC12 CTSU SCI0 DTC DOC ELC	USBFS USBHS	Other	SRAM	Standby RAM	Flash memory	
Sleep	Stop (retained)	Selectable	Selectable	Operating	Selectable	Selectable	Selectable	Selectable	Selectable	Selectable	Selectable	Selectable	Selectable	Operating	Operating
Software Standby	Stop (retained)	Stop	Selectable	Operating	Stop (retained)	Selectable	Selectable	Stop (retained)	Stop (retained)	Stop (retained)	Stop (retained)	Stop (retained)	Stop (retained)	Stop (retained)	Stop (retained)
Snooze *1	Stop (retained)	Selectable	Selectable	Operating	Operation prohibited	Selectable *2	Selectable	Stop (retained)	Selectable	Operation prohibited	Operation prohibited	Selectable	Selectable	Stop (retained)	Operating *3
Deep Software Standby	Stop (Undefined)	Stop	Selectable *4	Operating	Stop (retained)	Stop (Undefined)	Selectable	Stop (Undefined)	Stop (Undefined)	Stop (retained/ Undefined)	Stop (Undefined)	Stop (retained)	Stop (retained/ Undefined)	Stop (retained)	Stop (retained)



*1 : For details of snooze mode, see this page.
*2 : For the IIC0,Wake-up interrupt operation only possible.
*3 : Stop Only EBCLK pin:(retained)
*4 : Stop Only AGT4~5:(Undefined)

SNOOZE MODE

- During software standby mode, some peripheral functions can operate without wakening the CPU (intermittent operation).
- By performing intermittent operation in software standby and snooze mode, the total current consumption can be reduced from mA to uA level compared to sleep mode operation.



HIGH-SPEED MODE

- By selecting the appropriate operating power control mode according to the operating frequency, power consumption can be reduced in normal, sleep, and snooze modes.
- In High-Speed mode, it will operate within the following operating voltages and operating frequency ranges:

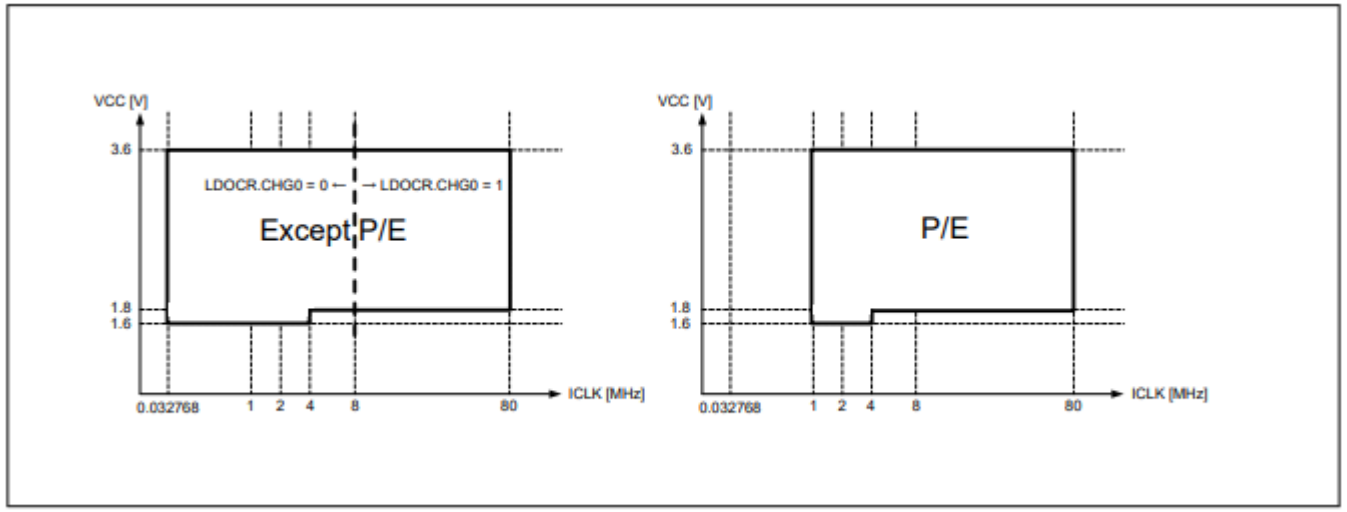


Figure 10.2 Operating voltages and frequencies in High-speed mode

For details on the mode, please refer to the User's Manual: Hardware of each product.

MIDDLE-SPEED MODE

- By selecting the appropriate operating power control mode according to the operating frequency, power consumption can be reduced in normal, sleep, and snooze modes.
- In Middle-speed mode, it will operate within the following operating voltages and operating frequency ranges:

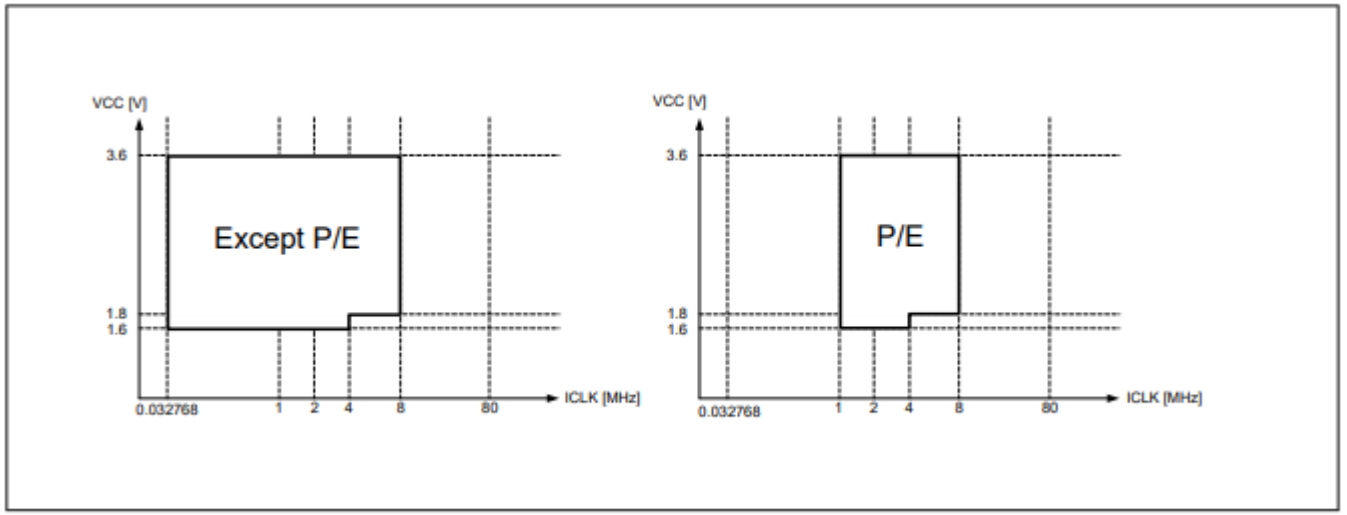


Figure 10.3 Operating voltages and frequencies in Middle-speed mode

For details on the mode, please refer to the User's Manual: Hardware of each product.

LOW-SPEED MODE

- By selecting the appropriate operating power control mode according to the operating frequency, power consumption can be reduced in normal, sleep, and snooze modes.
- In Low-speed mode, it will operate within the following operating voltages and operating frequency ranges:

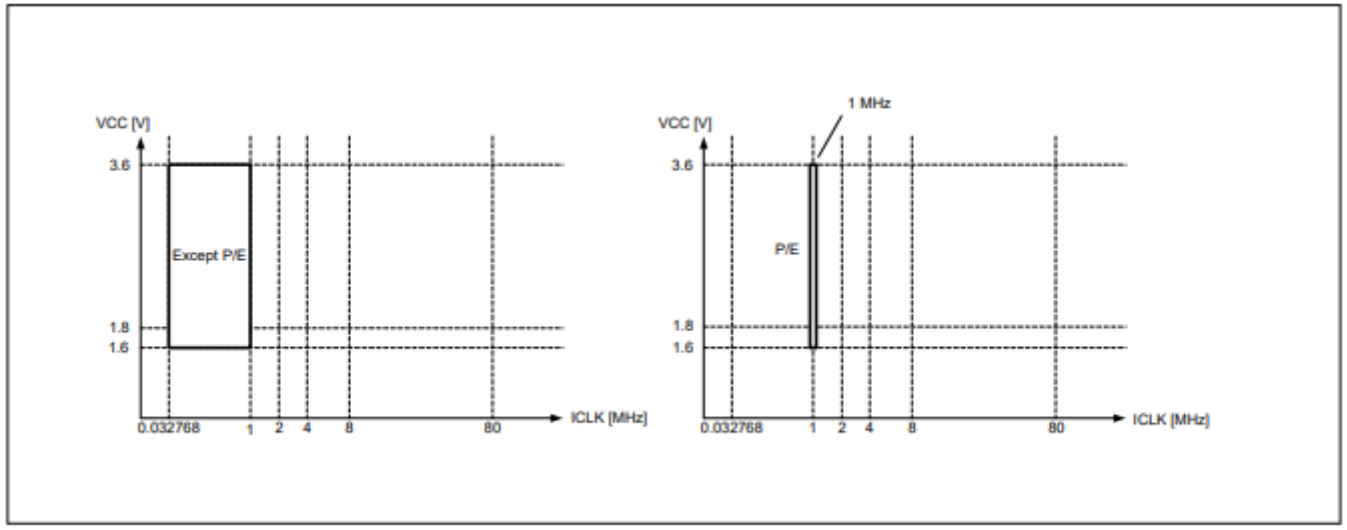


Figure 10.4 Operating voltages and frequencies in Low-speed mode

For details on the mode, please refer to the User's Manual: Hardware of each product.

SUBOSC-SPEED MODE

- By selecting the appropriate operating power control mode according to the operating frequency, power consumption can be reduced in normal, sleep, and snooze modes.
- In Subosc-speed mode, it will operate within the following operating voltages and operating frequency ranges:

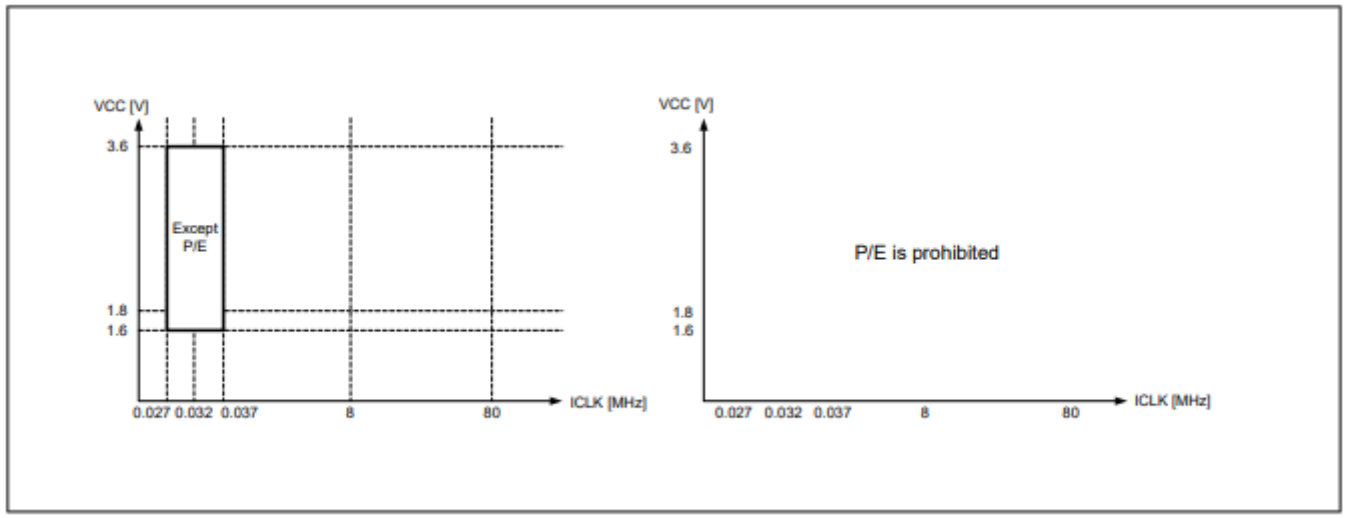


Figure 10.5 Operating voltages and frequencies in Subosc-speed mode

For details on the mode, please refer to the User's Manual: Hardware of each product.

TIPS FOR REDUCING POWER CONSUMPTION

Introduce tips for reducing power consumption using the RA4L1 as an example.

The following information depends on the product you are using. For details, please refer to the User's Manual: Hardware of each product.

① Utilize High-speed / Middle-speed / Low-speed / Subosc-speed operation mode as appropriate
Power consumption can be further reduced by lowering the operating frequency of the system when entering sleep or deep sleep mode.

② Stop unused peripheral modules
There is a large difference in current consumption when "all modules are operated" or "all modules are stopped". Therefore, power consumption can be reduced by stopping unused peripheral modules.

③ I/O Port
The current consumption of the I/O port for which the output is selected can be reduced by the following process.
- If it is connected to a pull-up resistor, set the output level to High, and if it is connected to a pull-down resistor, set the output level to Low.

Example) Comparison of current consumption in sleep mode and operation of all peripheral modules (typical)

	High-speed	Middle-speed	Low-speed	Subosc-speed
Current Consumption	22.8 mA	3.4 mA	0.94 mA	15 **uA**

Example) Comparison of current consumption of peripheral module operation/stop in High-speed sleep mode (typical)

	All peripheral operation	Stop all peripherals
Current Consumption	22.8 mA	5.63 mA

TIPS FOR REDUCING POWER CONSUMPTION

④ Clock Generation Circuit

When using low power mode, observe the following clock frequency settings: Here are some examples of the highest operating frequency and the circumferential ratio. For more information, refer to the chapter on Clock Generation Circuit in the user manual.

Table 8.2 Clock generation circuit specifications for the internal clocks (1 of 3)

Item	Clock source	Clock supply	Specification
System clock (ICLK)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	CPU, DTC, DMAC, Flash, RAM, I/O ports	Up to 80 MHz Division ratio: 1/2/4/8/16/32/64
Peripheral module clock A (PCLKA)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	Peripheral modules (QSPI, SCI, SPI, CRC, DOC, ADC12, DAC12, GPT bus clock, CNECC, IrDA, I3C)	Up to 80 MHz Division ratio: 1/2/4/8/16/32/64

Note: Restrictions on setting clock frequency: ICLK ≥ PCLKA ≥ PCLKB, PCLKD ≥ PCLKA ≥ PCLKB
ICLK ≥ FCLK
Restrictions on clock frequency ratio: (N: integer, and up to 64)
ICLK : FCLK = 1:1 when ICLK ≤ 48 MHz, ICLK : FCLK = 2:1 when 48 MHz < ICLK ≤ 80 MHz
ICLK : PCLKA = N:1, ICLK : PCLKB = N:1, ICLK : PCLKC = N:1 or 1:N , ICLK : PCLKD = N:1 or 1:N
If the A/D converter is enabled, the clock frequency ratio is constrained as follows:
PCLKA : PCLKC = 1:1 or 2:1 or 4:1 or 8:1 or 1:2 or 1:4

⑤ Changing the Regulator (LDO) Operating Mode

The LDO has normal operating mode and high-performance mode. Power consumption can be minimized by operating in the normal mode.

TIPS FOR REDUCING POWER CONSUMPTION

⑥ Sub-clock oscillator drive capability switching function
This function is implemented in some products of the RA4L1 Group.
The current consumption decreases in the following order: Normal mode> Low power mode 1, >Low power mode 2, > Low power mode 3.
In addition, in order to achieve low-power consumption modes 1, 2, and 3, the external crystal must be a low-CL product. so please inform each oscillator manufacturer for above-mentioned contents when requesting a matching evaluation or refer to the application note below to take a matching.

■ Application Note

Renesas RX and RA families Design Guide for Main Clock Circuits and Sub Clock Circuits R01AN7202EJ0102

APPLICATION NOTE FOR “LOW POWER CONSUMPTION” FUNCTION

- Please refer to the following APN for details on how to use the “Low Power Consumption” function.
  - RA2L1 Group Capacitive Touch Low Power Guide R01AN6266EJ0110
  - RA6M2 Group Capacitive Touch Low Power Guide R11AN6473EJ0100
  - RA2E3 Group RA2E3 HS4001 Low Power Sensor System Example R01AN7744EJ0101
  - Renesas RA0 Family Low Power Consumption Guide R01AN7893EJ0100

I/O PORT

LIST OF PORT FUNCTIONS

Table 18.2 I/O port functions

Port	Port name	Input pull-up	Input mode switching	Open-drain output	5V tolerant	I/O
Port0	P000 to P004, P010, P011	✓	—	—	—	Input / Output
Port1	P100, P101	✓	✓	✓	—	Input / Output
	P102 to P115	✓	—	✓	—	Input / Output
Port2	P200, P214, P215	—	—	—	—	Input
	P201, P204 to P213	✓	—	✓	—	Input / Output
Port3	P300, P303 to P307	✓	—	✓	—	Input / Output
	P301, P302	✓	✓	✓	✓	Input / Output
Port4	P400, P401	✓	✓	✓	✓	Input / Output
	P402 to P406, P408 to P415	✓	—	✓	—	Input / Output
	P407	✓	—	✓	✓	Input / Output
Port5	P500 to P513	✓	—	✓	—	Input / Output
Port6	P600 to P602, P608 to P610	✓	—	✓	—	Input / Output
Port7	P700, P708	✓	—	✓	—	Input / Output
Port8	P814, P815	✓	—	✓	—	Input / Output

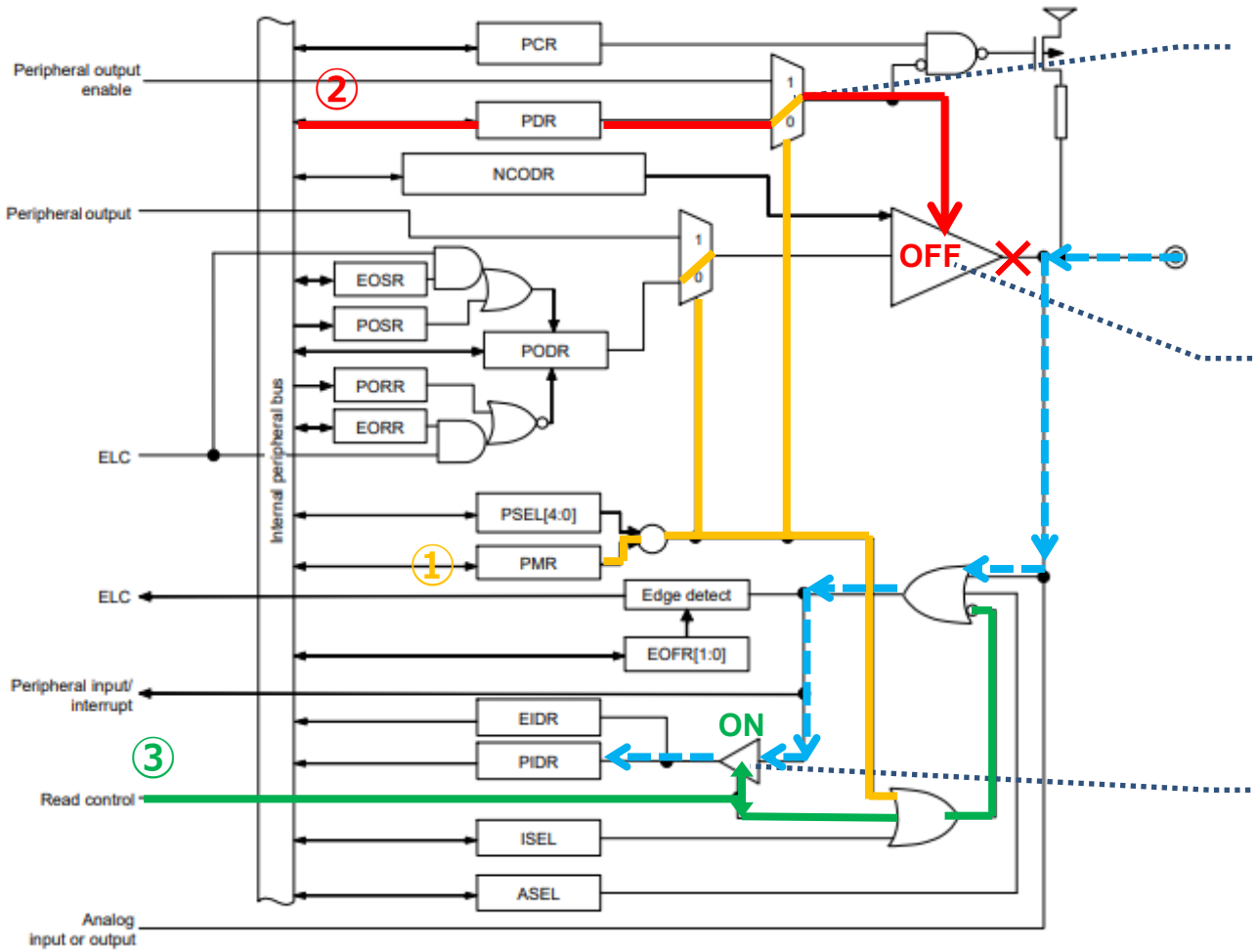
Note: ✓: Available
—: Setting prohibited

The following port functions are also valid for other signals (such as serial and other peripheral functions) that share pins with general-purpose I/O ports.

- Input pull-up function
- Open-drain output function
- Drive ability switching function
- 5V tolerant setting

*This function is described using the RA4L1 as an example.

I/O PORT OPERATION - GENERAL I/O INPUT PORT -

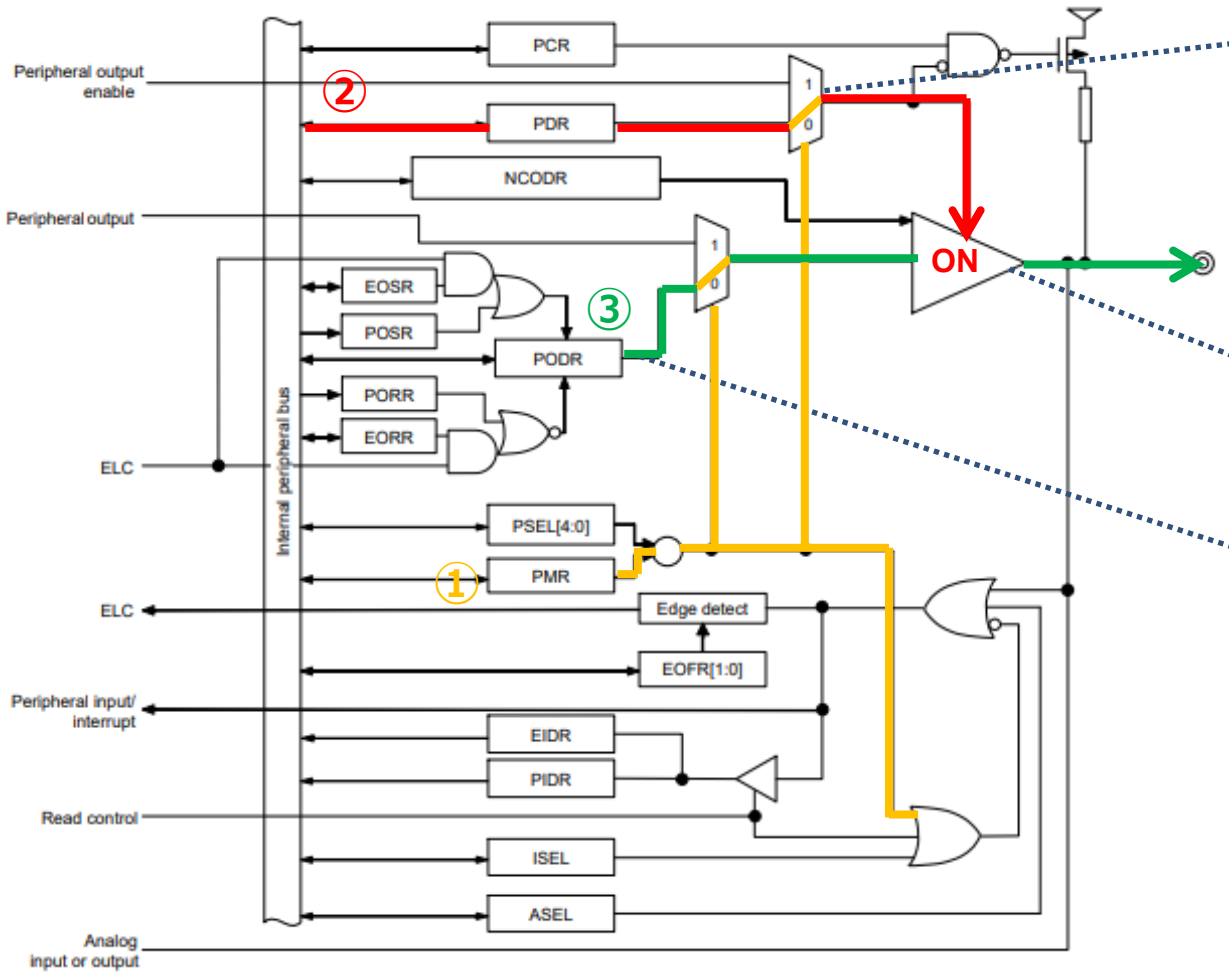


①By setting it to a general-purpose input/output port with the PMR register(PmnPFS.PMR=“0”),
Make the terminal control a general-purpose input/output port.

②By setting it to the input port with the PDR register (PmnPFS.PDR=“0”),
Turn off the output buffer.

③When the port(PmnPFS.PIDR) is read,
The input buffer is turned on and The High/Low of the target port is set to the PIDR.

I/O PORT OPERATION - GENERAL I/O OUTPUT PORT -



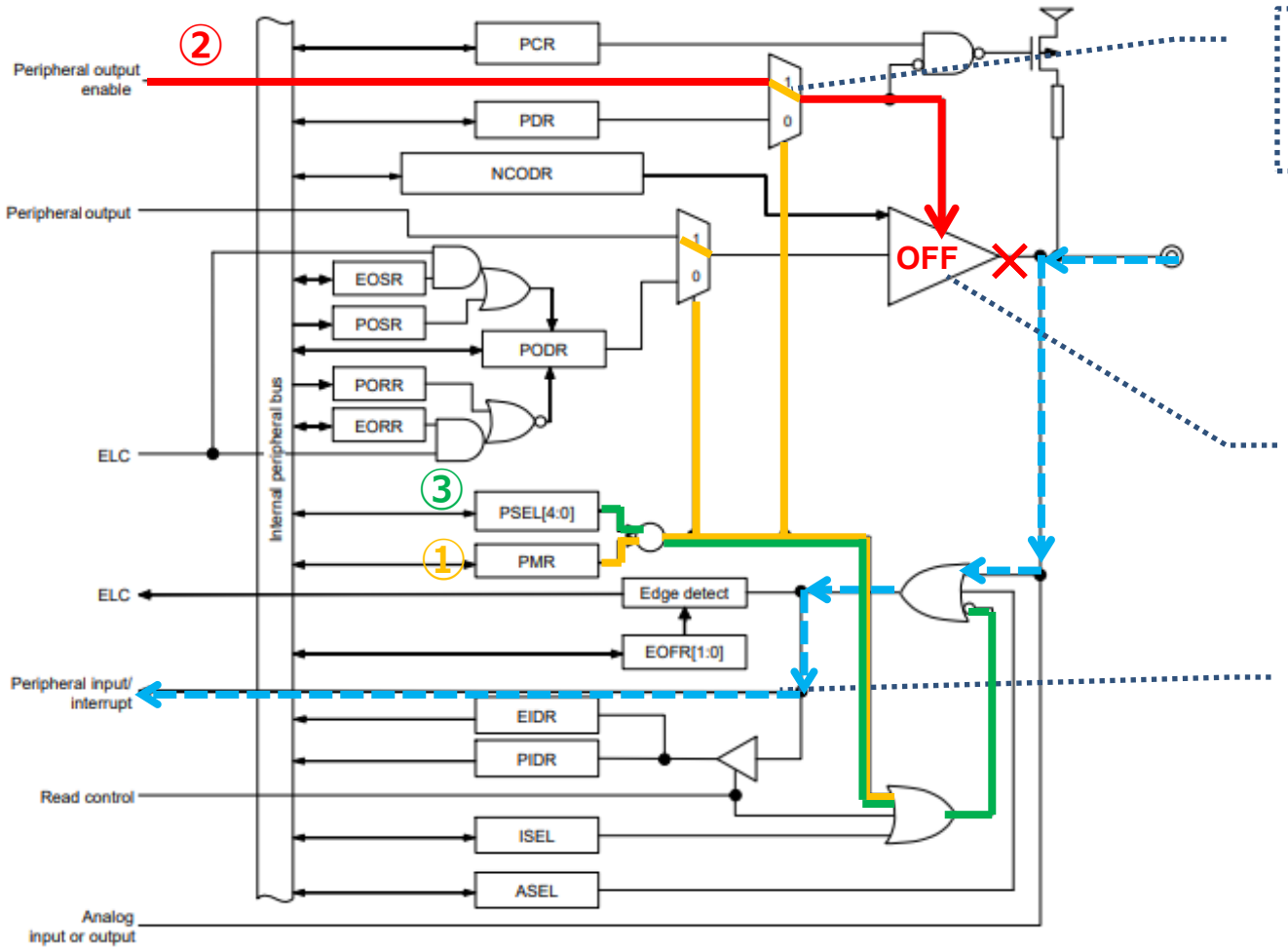
①By setting it to a general-purpose input/output port in the PMR register (PmnPFS.PMR=“0”),
Make the terminal control a general-purpose input/output port.

②By setting it to the output port with the PDR register (PmnPFS.PDR=“1”),
Turn on the output buffer.

③Port Output Data Register(PmnPFS.PODR) is printed from the target port.(”1”:High、”0”:Low)

I/O PORT OPERATION - PERIPHERAL FUNCTION INPUT -

- When the pin function of the port is set to "Use the pin as peripheral function" and the peripheral function to be used is the **input** operation.



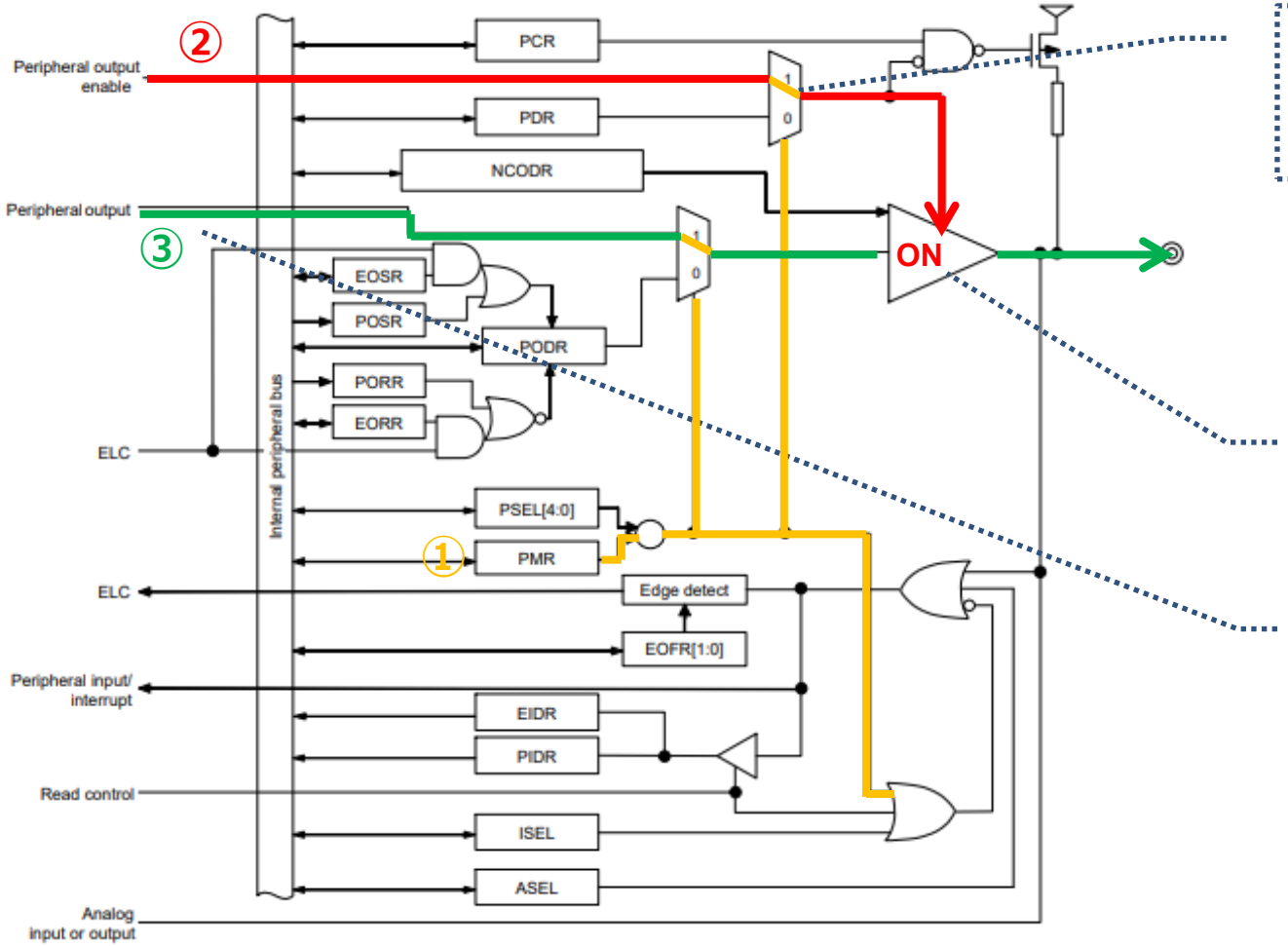
①By setting it as a port for peripheral functions with the PMR register (PmnPFS.PMR="1") , Make the terminal control a peripheral function port.

②Turn off the buffer by prohibiting the output of peripheral functions.

③When the terminal function control register (PmnPFS.PSEL) is set to a peripheral function, the High/Low of the target port is entered into the peripheral function.

I/O PORT OPERATION - PERIPHERAL FUNCTION OUTPUT -

- When the pin function of the port is set to "Use the pin as peripheral function" and the peripheral function to be used is the **output** operation.

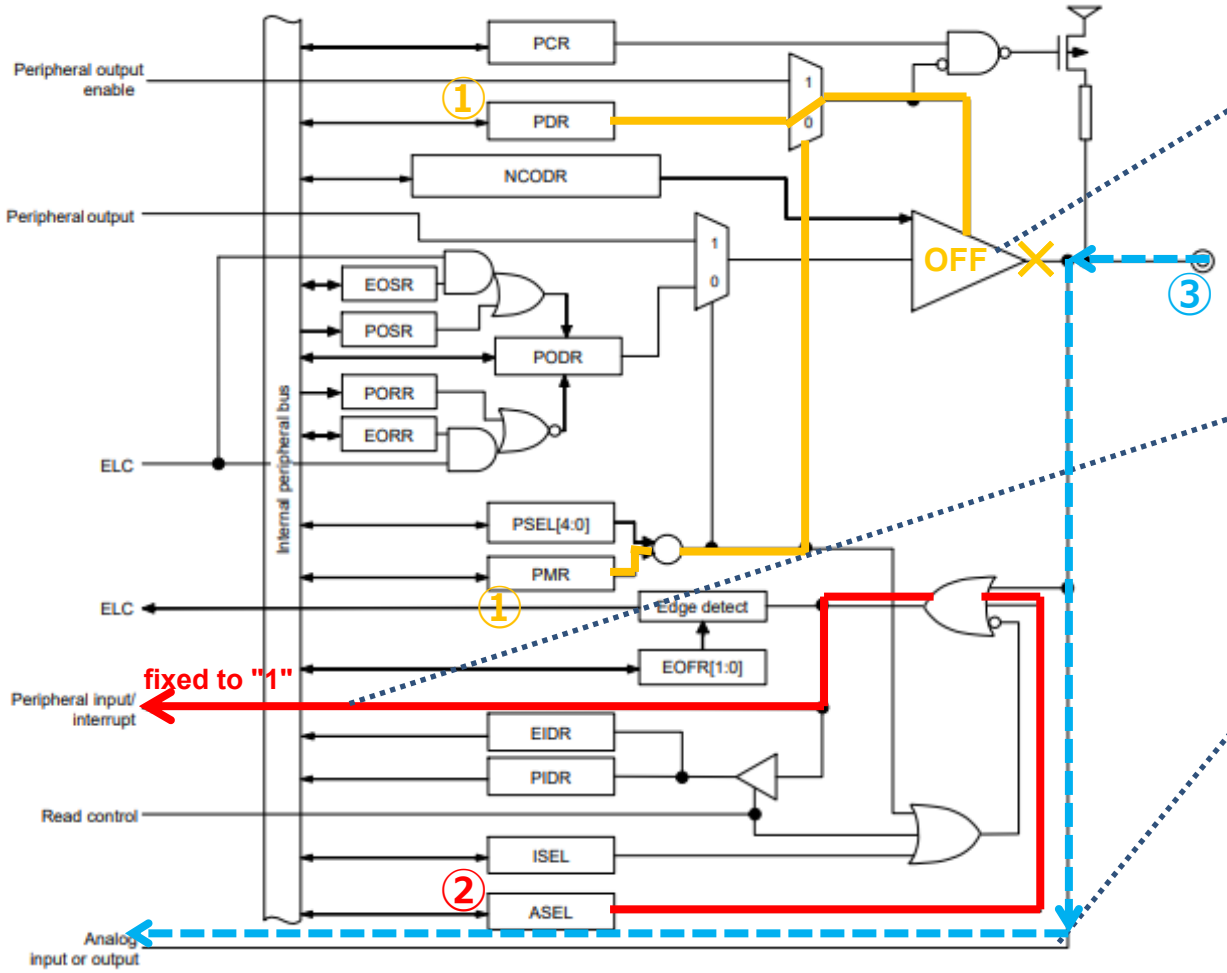


①By setting it as a port for peripheral functions with the PMR register (PmnPFS.PMR="1"), Make the terminal control a peripheral function port.

②Turn on the buffer with the Allow Output Operation of Peripheral Functions.

③Terminal function control register (PmnPFS.PSEL) to the peripheral function, the port output action from the peripheral function outputs High/Low to the target port.

I/O PORT OPERATION - ANALOG FUNCTION INPUT -

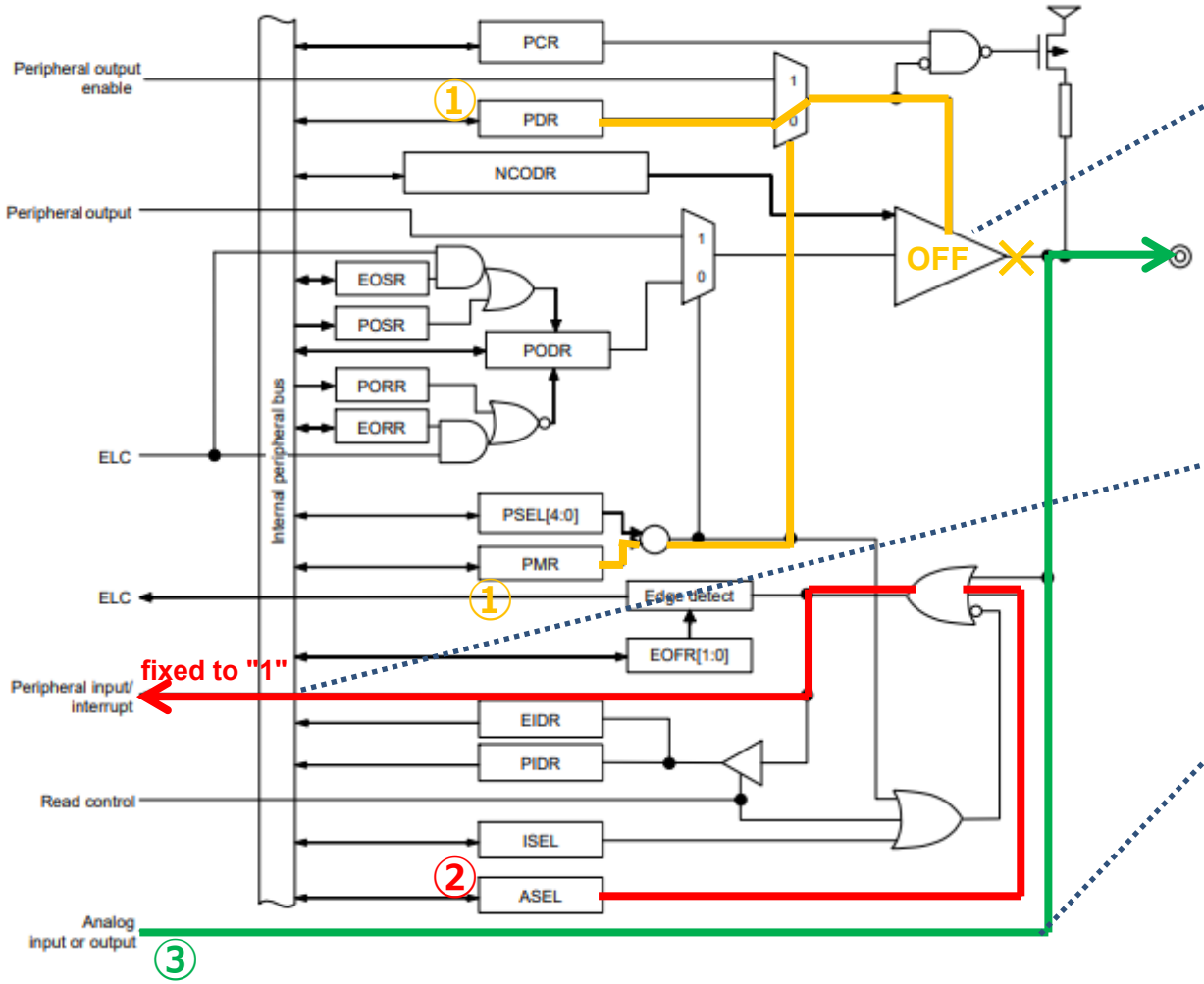


①Set the Port Mode Register (PMR) to "0" and the Port Direction Register (PDR) to "0", and make the pin a generic input port.

②When set to an analog port with a terminal function control register (PmnPFS.ASEL), the internal digital input signal is fixed to "1".

③When the analog input operation is started (such as the A/D sampling operation), the analog input is performed.

I/O PORT OPERATION - ANALOG FUNCTION OUTPUT -

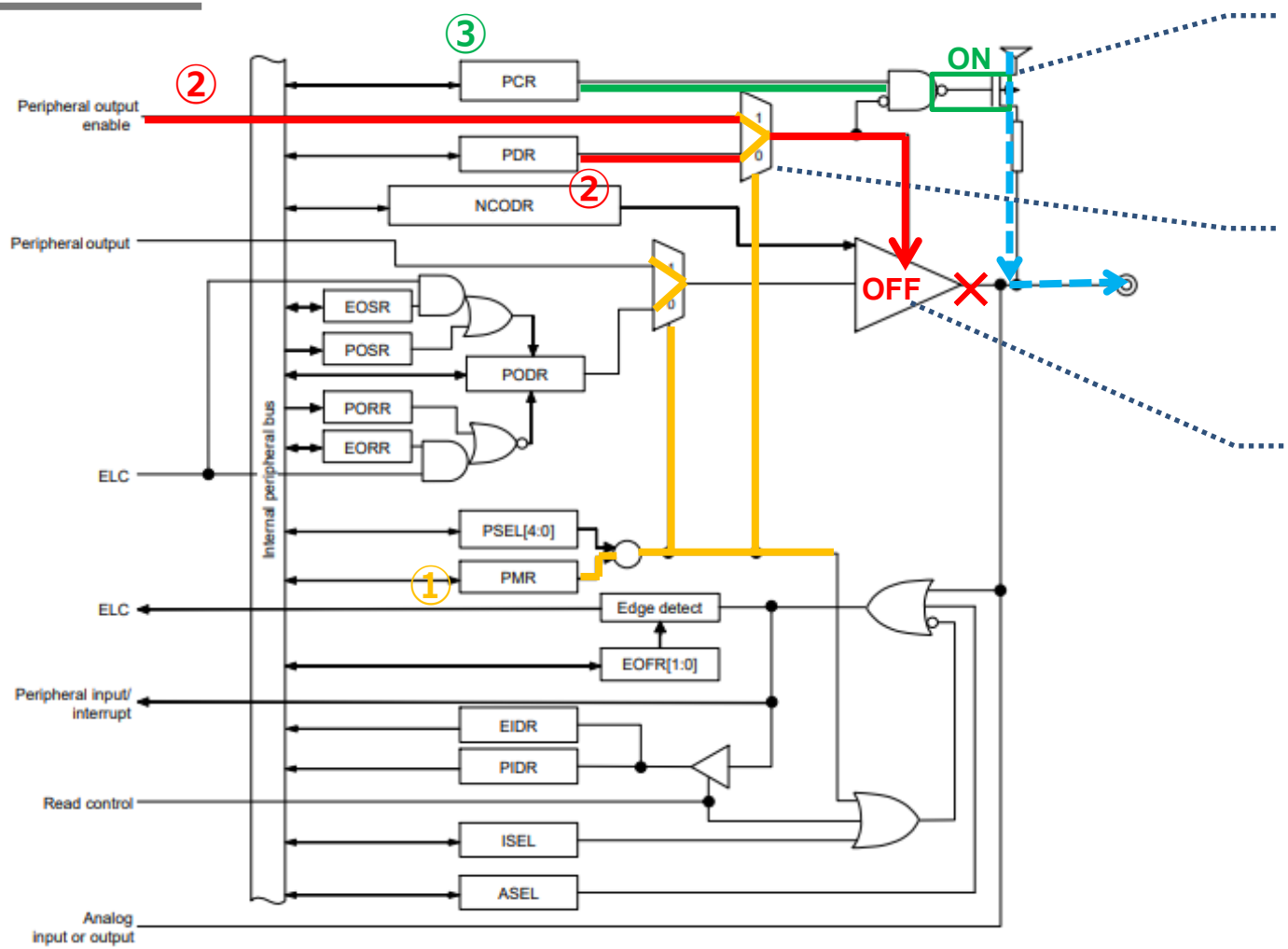


①Set the Port Mode Register (PMR) to "0" and the Port Direction Register (PDR) to "0", and make the pin a generic input port.

②When set to an analog port with a terminal function control register (PmnPFS.ASEL), the internal digital input signal is fixed to "1".

③When the analog output operation is initiated, a D/A signal is output from the target port.

I/O PORT OPERATION - PULL-UP -

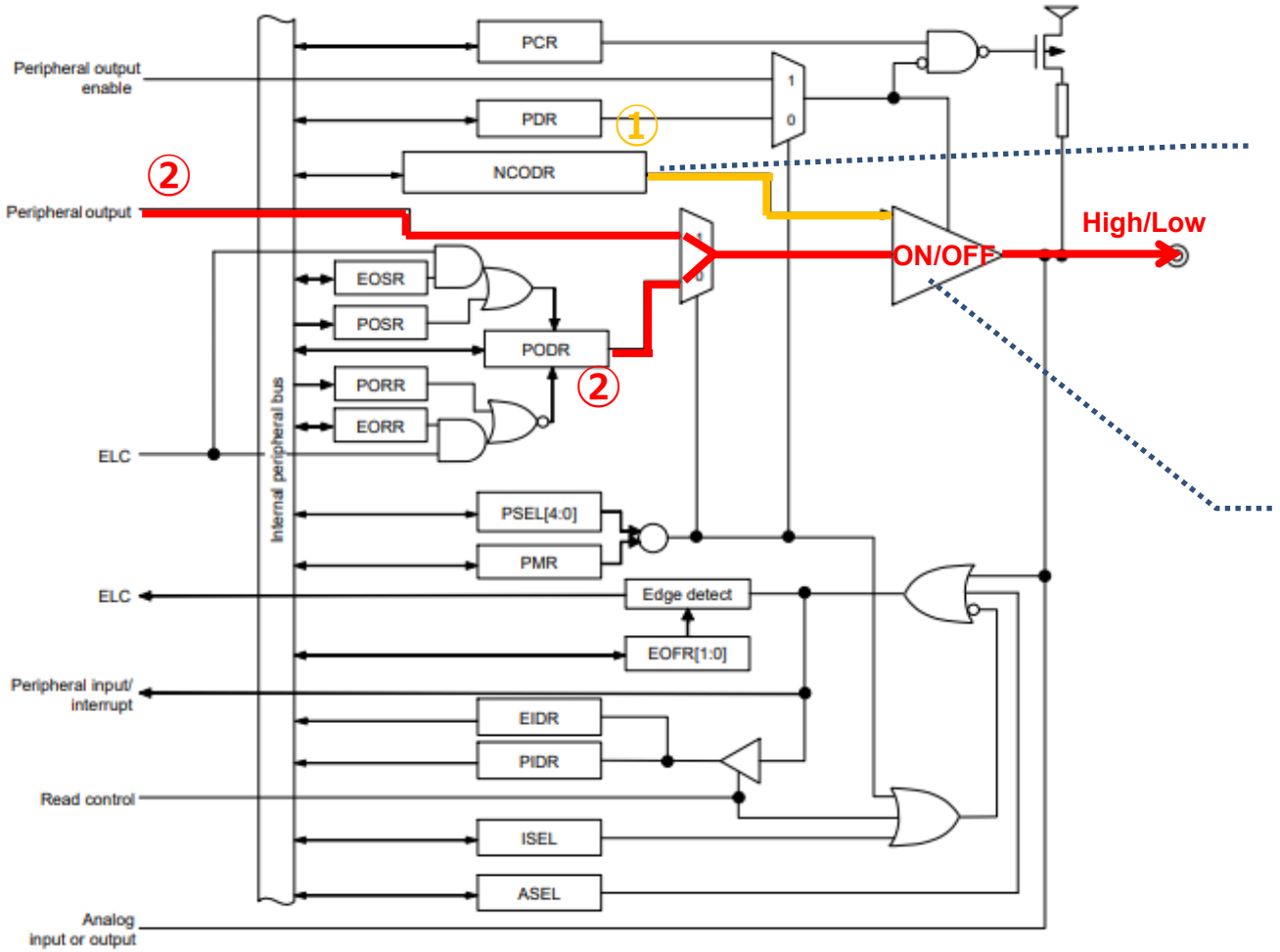


③When the pull-up control register (PmnPFS.PCR="1") is enabled, the pull-up is ON.

①Set the PMR register to a general-purpose I/O port or peripheral function (PmnPFS.PMR =“0” or “1”)。

②Set it to the input port in the PDR register (PmnPFS.PDR = "0"), or turn off the output buffer with the input operation of the peripheral function.

I/O PORT OPERATION - N-CHANNEL OPEN-DRAIN -



①By setting the open drain control register (PmnPFS.NCODR), the terminal function is set to the N-channel open drain terminal.

②The terminal set to the N-channel open drain terminal performs an N-channel open drain operation.
For terminals in N-channel open-drain operation, N-MOS is turned off and the terminal level is set to Hi-Z when "High" is output, and N-MOS is turned on and the terminal level is set to Low when "Low" is output.
It can be used for both general-purpose output and peripheral function operation.

NOTICE FOR I/O PORT SETTINGS

- Common
  - When PmnPFS.PIDR is read, the pin status is read regardless of PmnPFS.PDR and PmnPFS.PMR registers.
  - Pull-up enables the input pull-up resistor of the pin corresponding to the bit with the PmnPFS.PCR register set to “1” when the pin is in the input state. The pull-up resistor is disabled during a reset.
  - The input-pull-up function, open-drain output function, drive capability switching function, and 5V tolerant setting are also valid for other signals that share a port with the general-purpose I/O port.

- Interrupt pins
  - The ISEL bit is set when used as an IRQ input pin (external pin interrupt). It can also be used in combination with peripheral functions. However, it is prohibited to enable IRQn of the same number by two or more pins.

- Analog port
  - When setting the pins as analog pins with ASEL bit, set the relevant bit of the port mode register (PmnPFS.PMR) and the relevant bit of the port direction register (PmnPFS.PDR) to “0” to set the relevant pins as general-purpose inputs, set PmnPFS.ASEL bit to “1”. The pin status cannot be read at this time.

- Peripheral function port
  - The PmnPFS.PSEL[5:0] bit should be changed with the PmnPFS.PMR bit set to “0”.

- Other
  - For ports to which RIIC and RI3C are assigned, set the PmnPFS.PCR bit to “0”.
    (Pull-up is automatically turned off for peripheral function outputs other than RIIC and RI3C.)

WATCHDOG TIMER/ INDEPENDENT WATCHDOG TIMER (WDT/IWDT)

FUNCTIONAL COMPARISON OF WDT AND IWDT

WDT
IWDT

The functional comparison between WDT and IWDT is as follows.

Blue text : Functional difference

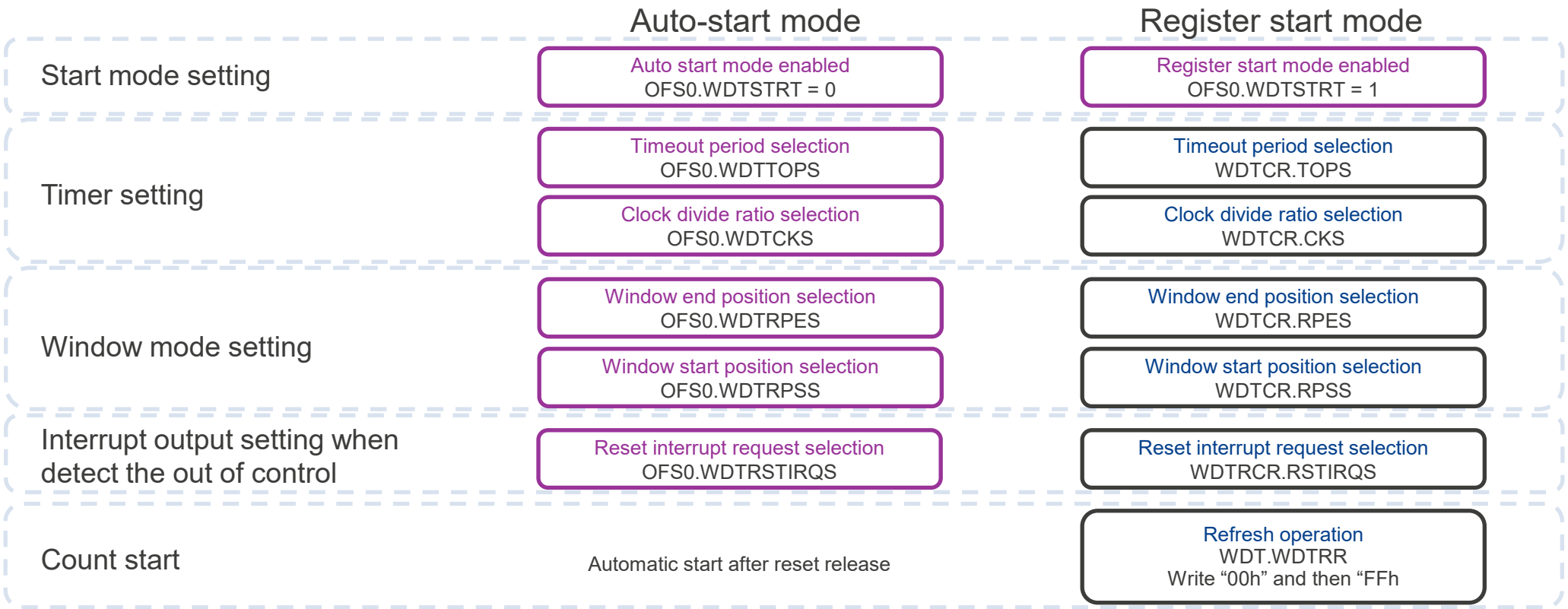
Item	WDT	IWDT
Count source	Peripheral module clock	**IWDT-dedicated clock (IWDTCLK)**
Clock divide ratio	4/64/128/512/2048/8192	**1/16/32/64/128/256**
Conditions for starting the counter	・Auto-start mode: Counting automatically starts after a reset is released ・Register start mode: Counting is started by refresh operation	**・Auto-start mode : Counting automatically starts after a reset**
Conditions for stopping the counter	・Reset ・In low power consumption states(Depends on register setting) ・A counter underflows or a refresh error occurs (only in register start mode)	・Reset ・In low power consumption states(Depends on register setting) ・A counter underflows or a refresh error occurs (only in register start mode)
Window function	Yes	Yes
Reset output sources	・Down-counter underflows ・Refreshing outside the refresh-permitted period (refresh error)	・Down-counter underflows ・Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/ interrupt sources	・Down-counter underflows ・Refreshing outside the refresh-permitted period (refresh error)	・Down-counter underflows ・Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	Enable	Enable
Event link function	Yes	Yes
Output signal (Internal signal)	・Reset output ・Interrupt request output ・Sleep mode count stop control output	・Reset output ・Interrupt request output ・Sleep mode count stop control output
Operations during low power consumption mode	Run / Stop (Selectable) *1	Run / Stop (Selectable) *1

*1 Each low-power modes works differently.
For details, see the Power Consumption Reduction page.

WDT SETTINGS LIST

The watchdog timer has two modes of operation: auto start mode and register start mode.
Each mode is configured by setting registers in the Option Setting Memory (OFS) or WDT.
The following figure shows the registers that need to be set in each operation mode.

: OFS setting
: WDT setting



IWDT SETTINGS LIST

IWDT support auto start mode only.
Auto start mode is configured by setting registers in the Option Setting Memory (OFS).
The following figure shows the registers that need to be set in each operation mode.

Start mode setting	Auto start mode enabled OFS0.IWDTSTRT = 0
Timer setting	Timeout period selection OFS0.IWDTTOPS[1:0] Clock divide ratio selection OFS0.IWDTCKS[3:0]
Window mode setting	Window end position selection OFS0.IWDTRPES[1:0] Window start position selection OFS0.IWDTRPSS[1:0]
Interrupt output setting when detect the out of control	Reset interrupt request selection OFS0.IWDTRSTIRQS
Count stop setting in sleep mode	Sleep Mode Count Stop Control OFS0.IWDTSLCSTP
Count start	Automatic start after reset release

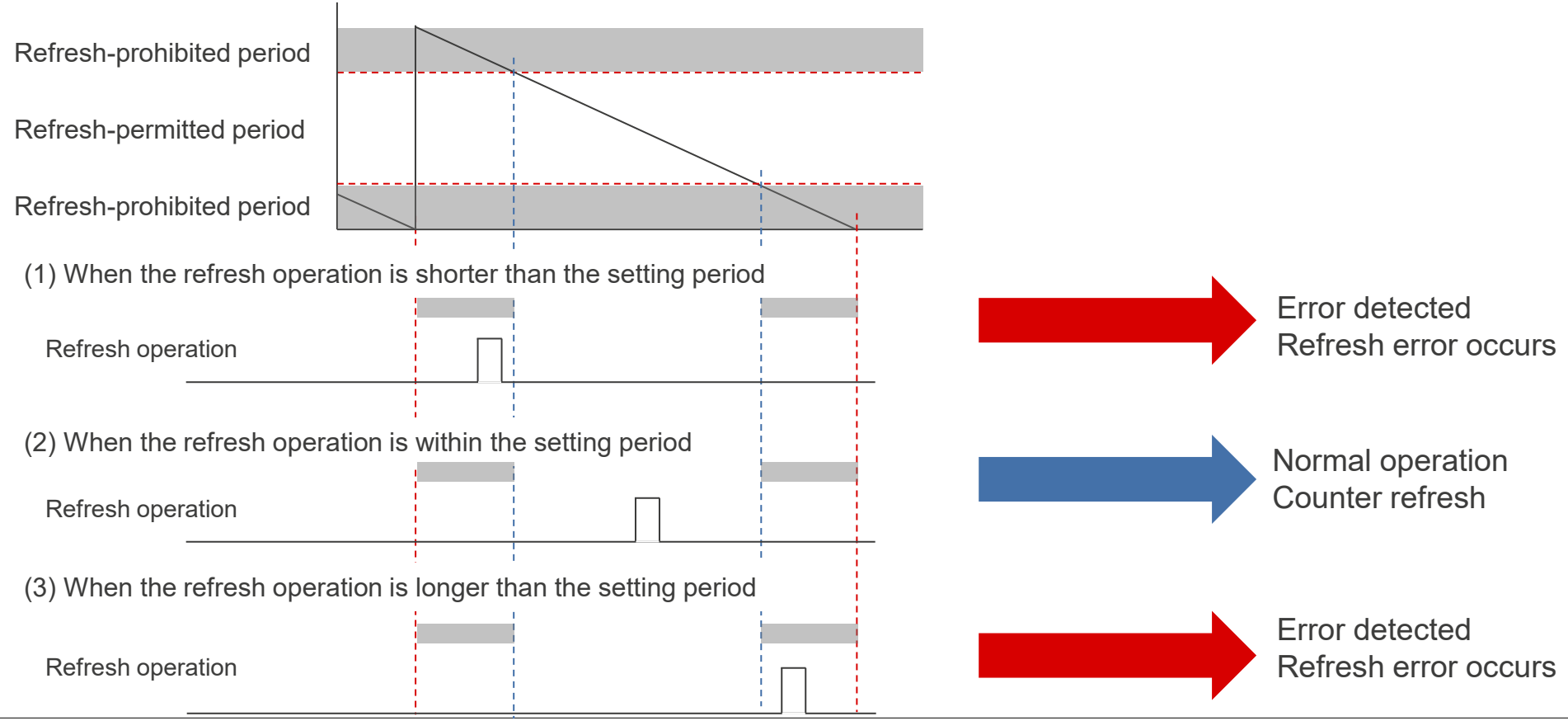
FUNCTION EXPLANATION: WINDOW MODE

WDT
IWDT

In window mode, set the permitted and prohibited periods for refresh operations.

If a refresh operation is executed during the prohibited period, a refresh error occurs and the system is judged to be out of control.

In addition to CPU running out of control, this function can also detect deviations in the processing cycle, making it suitable for applications with high periodicity and reliability requirements.

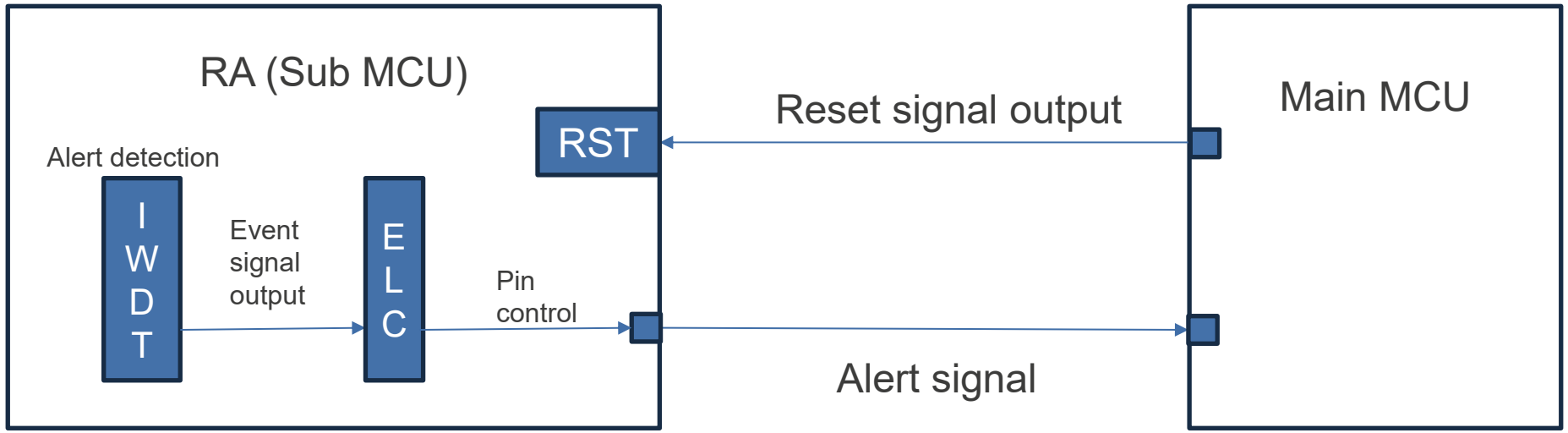


USE CASE:
OUTPUT ERROR ALERT TO EXTERNAL MAIN MCU USING EVENT LINK CONTROLLER (ELC)

WDT
IWDT

WDT or IWDT can output signals to the ELC when a refresh error or underflow occurs and can output external signals from I/O ports using the ELC without going through the CPU.

The figure below shows how to detect an alert in IWDT, send an alert notification to the external main MCU, and execute a hardware reset from the main MCU. The main MCU can check the status of the sub-MCUs and monitor the number of alerts.



*When using ELC, non-maskable interrupt request or interrupt request output must be enabled (IWDTRCR.RSTIRQS = 0).

NOTE

WDT
IWDT

- When WDT or IWDT is operated, it cannot be stopped except under the count stop condition. The stop conditions are as follows.
  - Reset
  - Low power consumption state (IWDT can be enabled/disabled by register setting)
  - In case underflow or refresh error occurs (only in register start mode)

- When debugging on the emulator, the WDT and IWDT counts stop during the break. The stopped counts are restarted during program execution.

REVISION HISTORY

Revision	Date	Page	Contents
1.00	April, 2026	-	First edition, issued