Reading the Phase Accumulator of the HSP45106

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The Block Diagram shown below illustrates the method of reading the phase accumulator of the NCO16 from a microprocessor. The setup shown is very similar to that used when the part is used for generating a complex sinusoid, except that the internal SIN/COS lookup is bypassed by setting the TEST pin to a logic 1 (high). While the TEST pin is high, the phase accumulator continues to drive the inputs of the SIN/COS Generator while the most significant 28 bits of the phase accumulator are multiplexed out onto the output pins. Because of this, the part can be operated in two modes, one where the SIN/COS Generator is permanently bypassed, and one where the phase accumulator output is brought out to the outputs as a check.

Figure 1 shows the circuit for reading out the phase accumulator all the time. In this case, a microprocessor loads the frequency and phase registers of the NCO16. This is fairly straightforward, except for the Start Logic Block, which needs to be synchronous to the oscillator clock and the microprocessor interface. This has been left as an undefined function, since it is dependent on the implementation. Also note that all COS outputs (COS0-15) are connected, although only COS4-15 are valid in this application. The microprocessor reads the sine and cosine data busses as if they were RAMs, using the decoded address bus to select one or the other.

The timing for loading the Center Frequency Register (MSB and LSB) and data being output on COS0-15 and SIN0-15 is shown in Figure 2. This timing is independent of whether the output data represents the phase accumulator data or the SIN/COS Generator output.

When it is desired for the output of the NCO16 to be switched back and forth between sine/cosine and the phase accumulator, a circuit such as the one shown in Figure 3 could be used. In this case, the sinusoidal output cannot be interrupted, so the phase accumulator must be read out between samples. This is possible due to the fact that the TEST signal is simply the control line for a multiplexer on the output of the SIN/COS Generator, but carries with it a limitation on the maximum possible clock rate. Since TEST is a synchronous input, the output of the NCO16 must be either driven by the SIN/COS Generator or the phase accumulator for an entire clock cycle. Therefore, the part must be driven at twice the desired speed at all times so there is a clock cycle available for TEST, when necessary. Note that the processor must be driven from the same clock that generates the NCO clock in order to maintain synchronous operation.

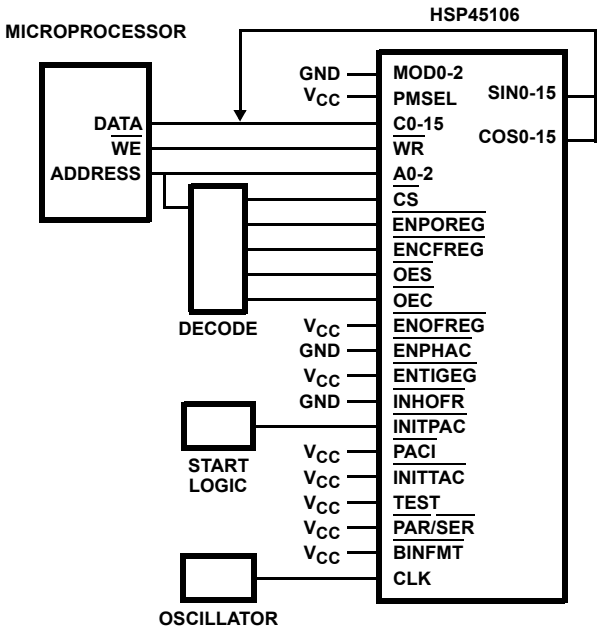

FIGURE 1. CIRCUIT FOR READING PHASE ACCUMULATOR OF NCO16

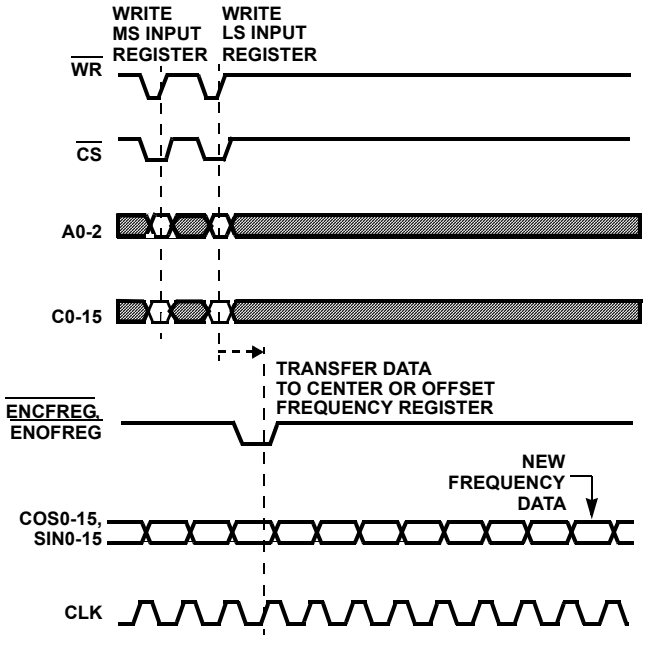

FIGURE 2. NCO16 PIPELINE DELAY

The timing is identical to that shown in Figure 2 with CLK replaced with CLK/2.

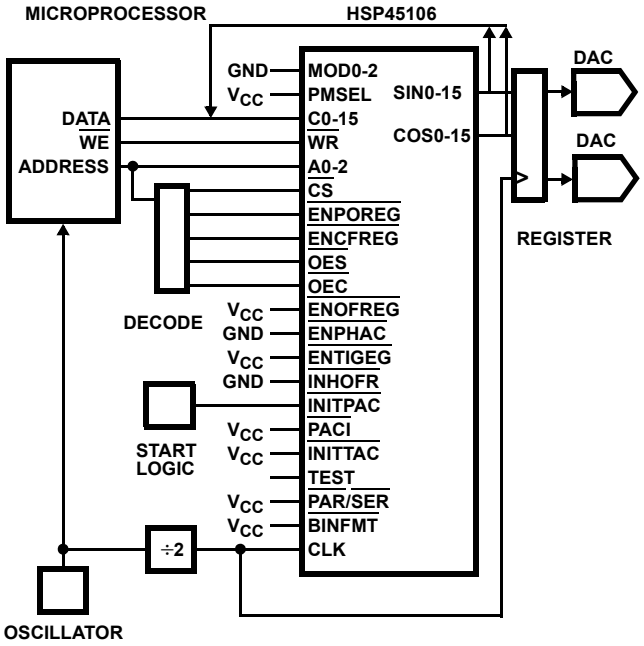

FIGURE 3. CIRCUIT FOR READING PHASE ACCUMULATOR OF NCO16 WHILE GENERATING SINUSOID

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