ISL62771

Disabling the North Bridge Regulator

TB497
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The ISL62771 is a feature rich power supply controller targeted for AMD SVI2 compliant processors that is capable of controlling two independent rails. One of the rails, referred to as the Core regulator, can be configured as either a two-phase regulator or a single-phase regulator. The second rail is a single phase regulator and is referred to as the North Bridge regulator.

Many applications require a single AMD SVI2 compliant power supply that utilizes only one or two phases. The ISL62771 can support these requirements but it lacks an option for disabling the North Bridge regulator so that only the Core regulator is running. This technical brief describes the method that can be used to effectively disable the North Bridge regulator so that the ISL62771 is controlling a single output.

Figure 1 shows how to configure the ISL62771 with the North Bridge regulator disabled and the Core regulator configured as a two-phase system.

Figure 2 shows how to configure the ISL62771 with the North Bridge regulator disabled and the Core regulator configured as a single-phase system.

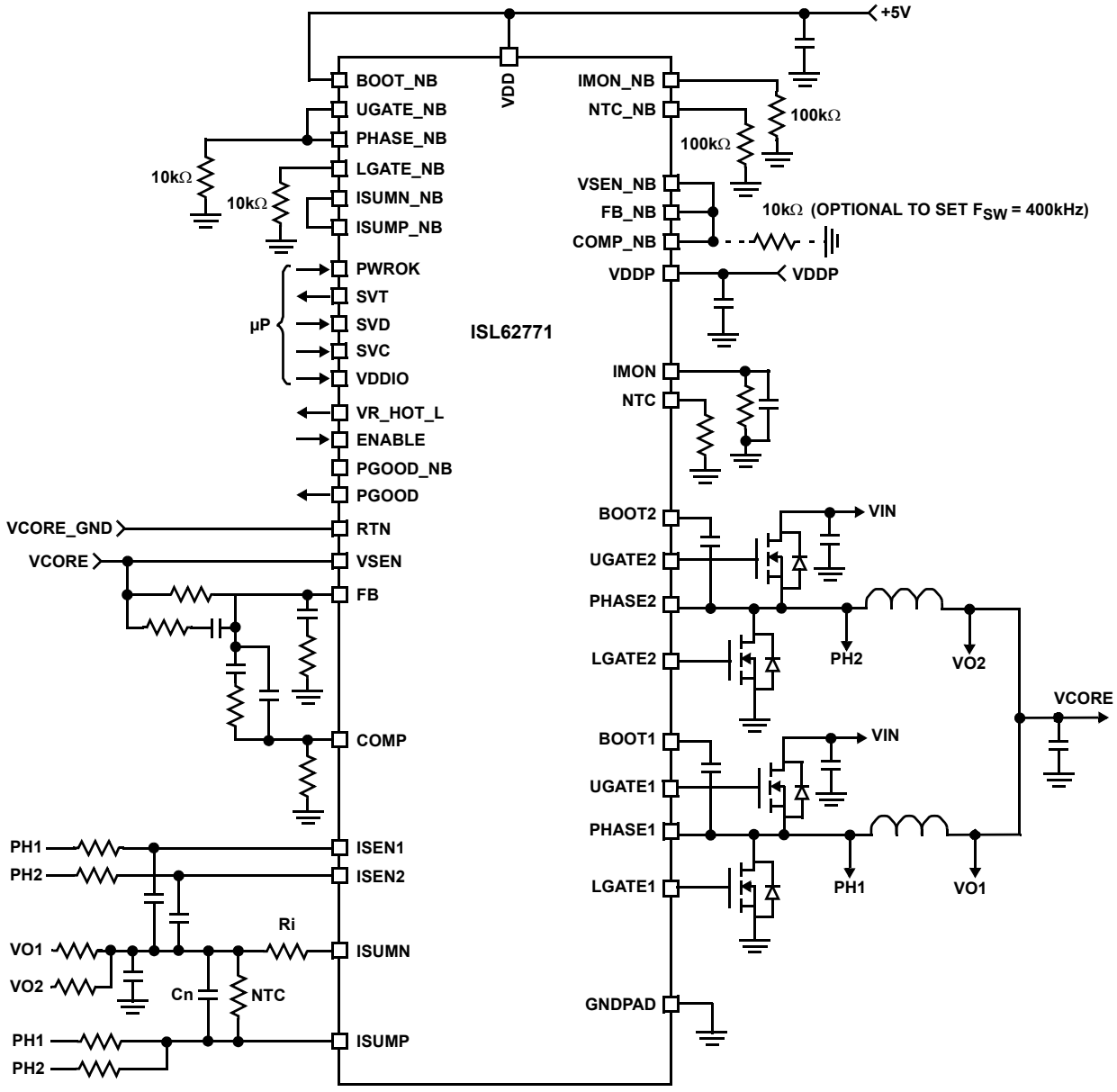

FIGURE 1. TWO-PHASE CORE REGULATOR WITH NORTH BRIDGE DISABLED

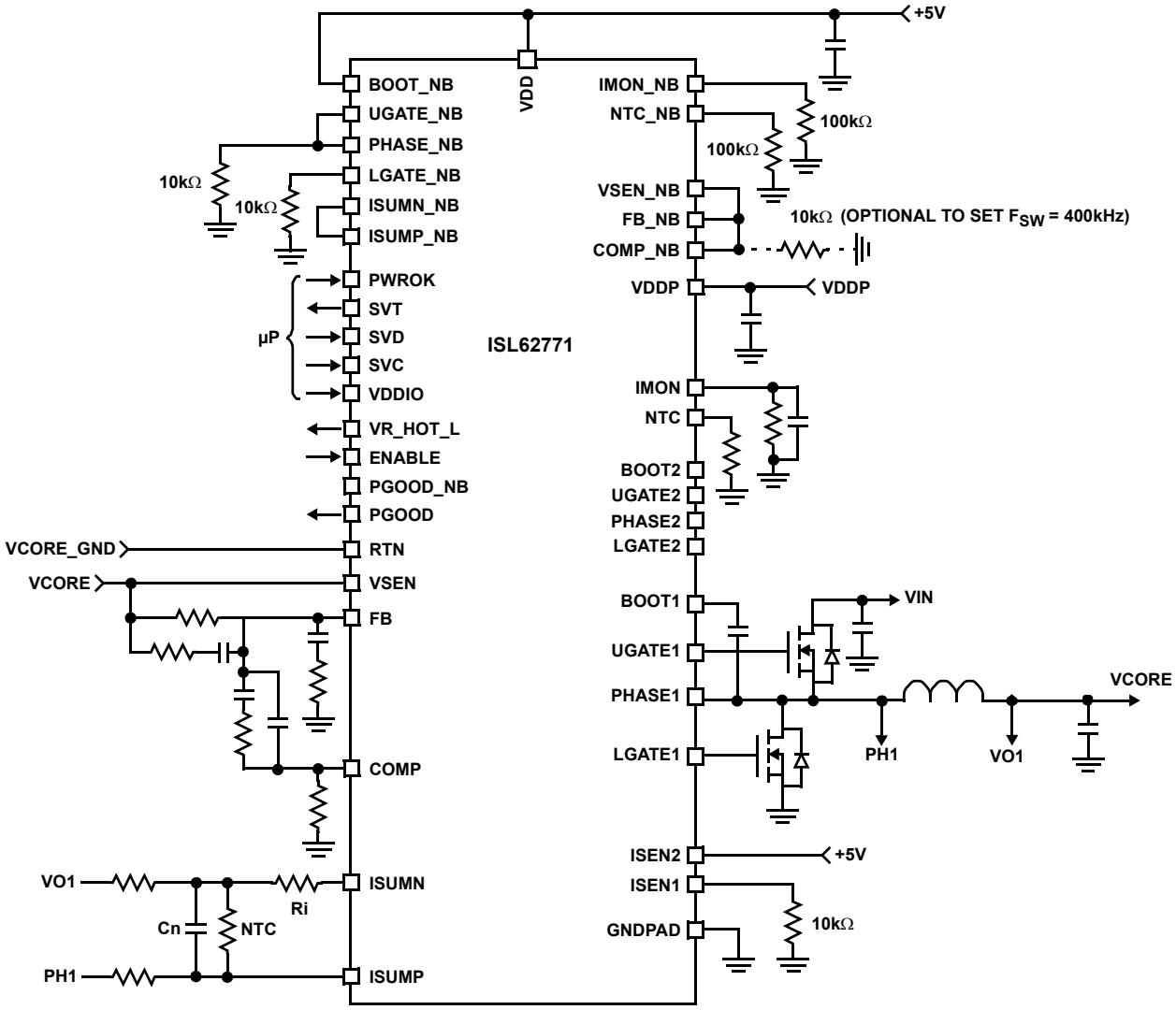

FIGURE 2. SINGLE-PHASE CORE REGULATOR WITH NORTH BRIDGE DISABLED

The Core regulator is configured as either a one- or two-phase system per the instructions given in the ISL62771 datasheet. Whether the Core regulator is configured as a one- or two-phase system, the North Bridge regulator is disabled in the same manner:

1. Short the following pins together: COMP_NB (pin 36), FB_NB (pin 37), and VSEN_NB (pin 38).
2. Short the following pins together: ISUMN_NB (pin 39) and ISUMP_NB (pin 40).
3. Tie pin IMON_NB (pin 2) to ground through a 100kΩ resistor.
4. Tie pin NTC_NB (pin 1) to ground through a 100kΩ resistor.
5. Tie pin BOOT_NB (pin 31) to pin VDD (pin 25).
6. Tie pin PHASE_NB (pin 33) to pin UGATE_NB (pin 32).
7. Tie pin LGATE_NB (pin 34) to ground through a 10kΩ resistor.
8. Tie pin UGATE_NB (pin 32) to ground through a 10kΩ resistor.
9. Pin PGOOD_NB (pin 35) can be left floating.

These instructions will yield a system with a switching frequency of 300kHz. In order to obtain a 400kHz switching frequency, the COMP_NB pin should be tied to ground through a 10kΩ resistor.

Programming an offset on the Core regulator is accomplished through the prescribed method in the ISL62771 datasheet.

Behavior of the ISL62771

With the ISL62771 configured as described in this technical brief, the internal circuitry for the North Bridge regulator is not powered down nor is it disabled. All feedback, control, protection, and gate driver circuits are active. Due to this, there is a minor bias current draw for this active circuitry.

The shorting of the COMP_NB and FB_NB pins places a unity gain on the North Bridge amplifier. This will force the North Bridge DAC voltage on both of these pins after soft-start. Shorting the VSEN_NB pin to COMP_NB and FB_NB insures that there will be no over or undervoltage events that could shut the regulators down.

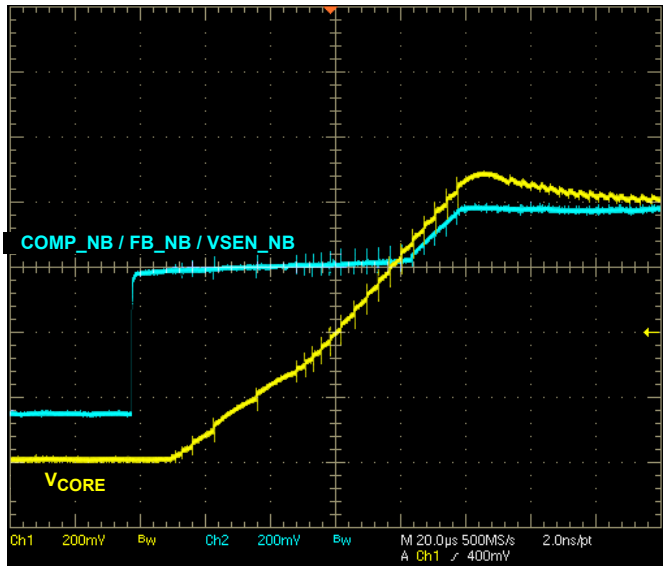

FIGURE 3. STARTUP WITH NORTH BRIDGE DISABLED

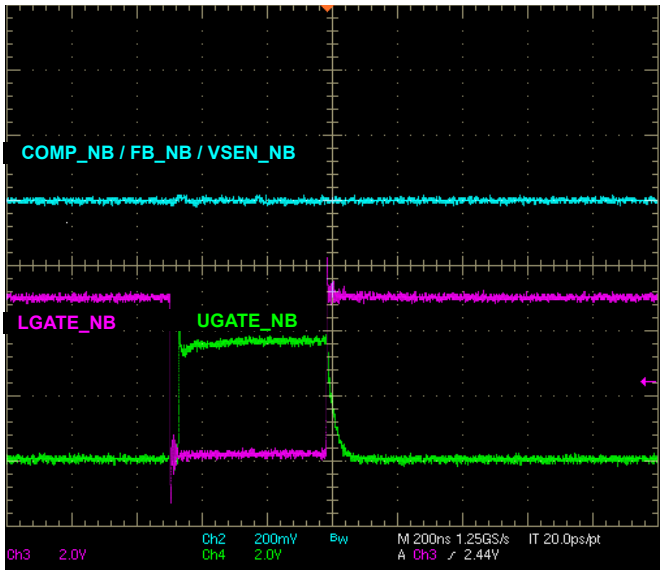

FIGURE 4. NORTH BRIDGE GATE SIGNALS

Figure 3 shows how the VSEN_NB, COMP_NB, and FB_NB pins will act during startup. Following startup, these pins will remain at whatever the MetalVID voltage is, unless an SVID command is sent to change the North Bridge DAC value.

If an SVI command is sent to the ISL62771 that commands the North Bridge DAC to a particular VID level, the COMP_NB, FB_NB, and VSEN_NB pins will ramp to that new VID level, tracking the DAC as it ramps. If an SVI command is never sent to the North Bridge regulator, then the COMP_NB, FB_NB, and VSEN_NB voltages will remain at the MetalVID voltage that was prescribed by the initial SVC and SVD voltages at startup.

Shorting the ISUMP_NB and ISUMN_NB pins together will force the current sensing amplifiers to measure a zero load current. As such, there can be no shutdowns due to a sensed overcurrent by the North Bridge circuitry.

Both the IMON_NB and NTC_NB pins are tied to ground through a 100kΩ resistor. These resistors will insure that there will be no overcurrent or thermal shutdown initiated by the North Bridge control circuitry.

The gate drivers for the North Bridge regulator remain active in this configuration. For this reason, the BOOT_NB pin is tied to VDD so that the upper gate driver retains a bias. The 10kΩ resistors on the UGATE_NB and LGATE_NB pins allow for a minimal amount of current to flow through the drivers when turned on. The PHASE_NB pin is tied to the UGATE_NB pin to simulate the switching of the PHASE node.

Figure 4 shows what the upper and lower gate signals will look like for the North Bridge regulator in this configuration. Figure 5 shows a number of switching cycles. If an SVI command is sent to the North Bridge regulator and the DAC is changed, the duty cycle of the gate signals will likely change. If the North Bridge DAC is commanded to a low enough voltage, the COMP_NB signal can fall below the oscillator and switching could halt entirely.

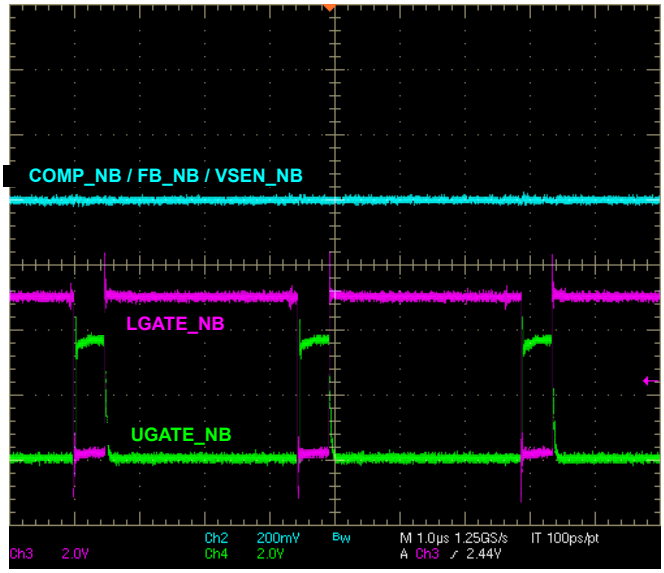

FIGURE 5. NORTH BRIDGE GATE SIGNALS SHOWING DUTY CYCLE

References

For Intersil documents available on the web, see www.intersil.com

[1] ISL62771 Datasheet

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

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