



# Tsi109™ Dual MPC7448 Reference Design Manual

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## About this Document

This document discusses the board architecture and detailed functional requirements of the Tsi109 dual MPC7448 reference design board. Its purpose is to provide a design reference for board designers who are implementing the schematic design.

## Related Information

- *Tsi108/109 User Manual*
- *Tsi109 Dual MPC7448 Reference Design Schematics*

## Revision History

### **60B5020\_MA001\_02, Formal, November 2009**

This version of the document was rebranded as IDT. It does not include any technical changes.

### **60B5020\_MA001\_01, Formal, December 2005**

This is the first version of the *Tsi109 Dual MPC7448 Reference Design Manual*.

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# 1. Board Architecture

## 1.1 Overview

The reference design connects dual MPC7448 PowerPC microprocessors from Freescale Semiconductor to the IDT Tsi109 host bridge. The Tsi109 provides a seamless interconnection from the processors to numerous types of peripheral devices. This design demonstrates how the features of the Tsi109 host bridge enhance the power of the MPC7448.

## 1.2 Features

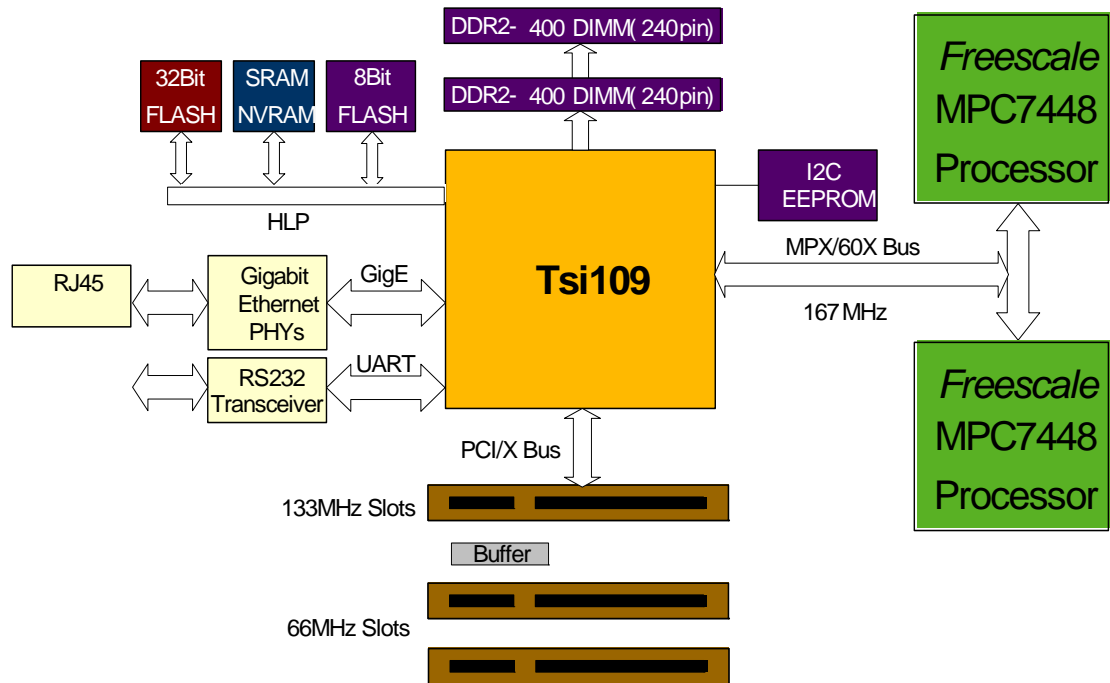
The MPC7448 implements the full PowerPC 32-bit architecture, and is targeted at networking and computing systems applications. The device supports both 60x and MPX bus protocols.

The Tsi109 dual MPC7448 reference design has the following features:

- Two Freescale MPC7448 processors
- One IDT Tsi109 host bridge
- Supports both MPX and 60x mode up to 167 MHz
- Two DDR2 240-pin DIMM slots support both unbuffered and registered DIMMs
- Up to 400M double data rate on the Memory Controller
- 512 KB 8-bit wide socket Flash
- 512 KB 8-bit wide SRAM
- 32 MB 32-bit wide Flash
- 32 KB Ferroelectric Nonvolatile RAM (FRAM)
- Two 10/100/1000BASE-TX Ethernet ports
- One 133-MHz PCI-X slot and two 66-MHz PCI/X slots.
- Two RS-232 serial ports
- Supports WindRiver PowerICE debugger tool
- Powered by a standard ATX power supply

## 1.3 Architecture

Figure 1: Board Block Diagram



## 2. Design Specifications

### 2.1 Processor

#### 2.1.1 MPX/60x Bus

The MPC7448 MPX/60x bus connects gluelessly to the Tsi109. Both processors are configured with the same bus and address mode. The Tsi109 Processor Interface voltage is set at the nominal 1.8V.

The MPX/60x bus signals listed in [Table 1](#) are not supported by the Tsi109, and are pulled appropriately.

**Table 1: MPX/60x Bus Non-supported Signals**

| Signal name | Description                    | Connection         |
|-------------|--------------------------------|--------------------|
| DTI[0]      | Data Transaction Index (Input) | Pull down          |
| WT          | Write-Through (Output)         | Pull up test point |
| CI          | Cache Inhibit (Output)         | Pull up test point |
| SHDn[0]     | Shared Signal (Bi-Dir)         | Pull up            |
| SHDn[1]     | Shared Signal (Bi-Dir)         | Pull up            |

#### 2.1.2 Interrupts and Resets

The Tsi109 drives the MPC7448 system clock. Since the system clock has to be stable before the processor is taken out of reset, the Tsi109 has to control the MPC7448 reset sequence. The HRESETn signal is connected to the Tsi109 PB\_RESETn output. TRSTn is controlled by on-board CPLD to support WindRiver PowerICE debugger. The SRESETn pin is connected to the COP header only.

The Tsi109 drives the MPC7448 interrupt signals: the Machine Check Interrupt (MCP) and the main Interrupt input (INT). The System Management Interrupt (SMI) is left with a pull up. The processor interrupt mapping for the reference board is listed in the following table.

**Table 2: Processor Interrupt Mapping**

| Signal name | Description                      | Connection     |
|-------------|----------------------------------|----------------|
| MPC_0       | CPU0 machine check interrupt     | Tsi109 PB_INT0 |
| INT_0       | CPU0 interrupt                   | Tsi109 PB_INT1 |
| SMI_0       | CPU0 system management interrupt | Pull up        |
| MPC_1       | CPU1 machine check interrupt     | Tsi109 PB_INT2 |
| INT_1       | CPU1 interrupt                   | Tsi109 PB_INT3 |
| SMI_1       | CPU1 system management interrupt | Pull up        |

### 2.1.3 System Clocks

The Tsi109 supplies the processor system clock (see [Section 2.3 on page 11](#)). The clock frequency can be set to 133 MHz or 167 MHz by a DIP switch. The MPC7448 PLL configuration pins are connected to the DIP switch. Both processors have the same PLL configuration setting.



DMAPE\_ACK[0:1] must be pulled up to 1.8V to set the Tsi109 device ID.

### 2.1.4 JTAG Header

The JTAG connector, which daisy chains the two processor's JTAG ports, is form factor and pinout compatible with the WindRiver Power ICE debugger. The connector is a standard 100mil spacing strip header.

## 2.2 Host Bridge

The Tsi109 connects the MPC7448 processors to numerous types of peripheral devices. Each peripheral, and its connection to the host bridge, is explained in the following sections of this document. This section discusses Tsi109-specific topics.

### 2.2.1 Power-up Configuration Options

The Tsi109 power-up options are set on the HLP bus either using resistors or DIP switches. The configuration options set with switches are listed in [Table 3](#).

**Table 3: Power-up Option Settings — DIP Switches**

| Description                         | Switch position and setting                                                                                                                            | HLP pin |
|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| PCI software reset                  | <b>0</b> : Release software reset after reset is released.<br><b>1</b> : Hold PCI Interface in software reset after reset is released.                 | AD[2]   |
| Host local port bus width           | <b>00</b> : 8-bit<br><b>01</b> : 16-bit<br><b>10</b> : 32-bit<br><b>11</b> : Reserved                                                                  | AD[4:3] |
| Processor bus mode select (60X/MPX) | <b>0</b> : MPX mode (controlled by CPLD)<br><b>1</b> : 60x mode (controlled by CPLD)                                                                   | AD[6]   |
| Processor bus holds software reset. | <b>0</b> : Enable Processor Interface reset after reset is released.<br><b>1</b> : Hold Processor Interface in software reset after reset is released. | AD[7]   |
| Host local port latch mode          | <b>0</b> : Enable latch mode<br><b>1</b> : Non-latch mode                                                                                              | AD[9]   |
| Processor boot vector select        | <b>0</b> : Maps boot vector 0x0_FFF0_0100 to HLP address 0x0_0000_0100<br><b>1</b> : Maps boot vector 0x0_FFF0_0100 to HLP address 0x0_0FF0_0100       | AD[14]  |



Board designers can change the power-up configuration options that are set using resistors by swapping the pull-up/pull-down resistors. Changing the default configuration is not recommended since it may cause the reference board to malfunction. The default configuration is described in [Table 4](#).

**Table 4: Power-up Option Settings — Pull-up/down Resistors**

| Description               | Default setting          | HLP pin | Level       |
|---------------------------|--------------------------|---------|-------------|
| PCI arbiter enable        | Enabled                  | AD[0]   | Pulled-up   |
| PCI PLL enable            | Enabled                  | AD[1]   | Pulled-down |
| PB PLL enable             | Enabled                  | AD[5]   | Pulled-down |
| PB pull-up enable         | Enabled                  | AD[8]   | Pulled-up   |
| SDRAM PLL enable          | Enabled                  | AD[10]  | Pulled-down |
| Host Local Port byte swap | Do not perform byte swap | AD[11]  | Pulled down |
| Processor bus timing      | MOT optimized timing     | AD[12]  | Pulled-up   |

## 2.2.2 Clock Generator Configuration

The Tsi109 is used as a clock generation and clock distribution hub for all components on the reference board. The device uses an external 33.3330MHz oscillator as a clock source, and internal PLLs multiply the source clock by a user-defined ratio. The Tsi109 generates clock signals for the processor, SDRAM, and PCI/X bus. Configuration pins on the Tsi109 set the clock generator's output frequencies during power up. The configuration pins are connected to a DIP switch. The default settings are:

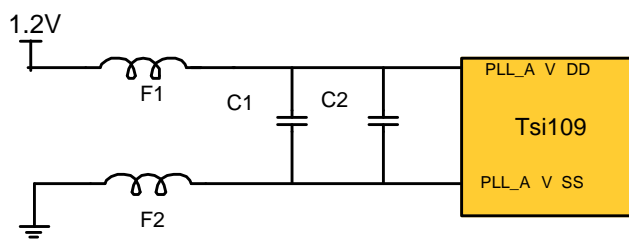
**Table 5: Tsi109 Clocking Configuration**

| Clock output  | Default frequency         | Default Setting     |
|---------------|---------------------------|---------------------|
| Processor bus | 167 MHz                   | Reference clock x 4 |
| SDRAM clocks  | 200 MHz                   | Reference clock x 6 |
| PCI clocks    | Dependant of PCIXCAP[0:1] | Set by CPLD         |

### 2.2.3 PLL Supply Filtering

It is critical that clean PLL\_VDD and PLL\_VSS are provided in order to reduce clock jitter. The PLL power supplies are supplied via the 1.2V rail, which is also supplying the Tsi109 core voltage. The PB\_PLL, SD\_PLL, PCI\_PLL, and CG\_PLL are filtered from the 1.2V\_core with a L-C circuit recommended by the PLL IP vendor.

**Figure 2: Tsi109 PLL Supply Filtering**



C1, C2: 0.01uF

F1 and F2: 50 Ohm ferrite bead similar to Murata P/N: BLM31PG500SN or Panasonic P/N: EXC-CL4532U1

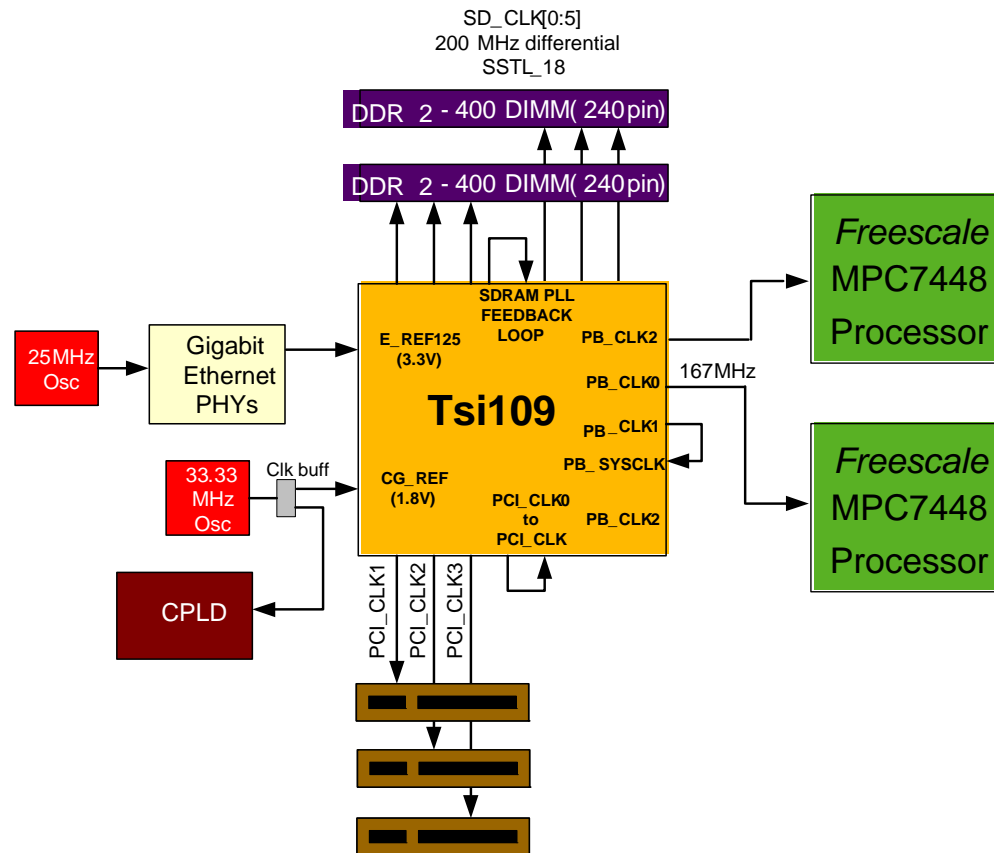
### 2.2.4 JTAG Port

The Tsi109 has its stand-alone JTAG header to support the internal registers access with boundary scan operation, and is 3.3V LVCMOS compatible.

## 2.3 System Clocking

The Tsi109 is used as a clock distributor for all timing critical interfaces. It uses a single 33.33MHz oscillator to generate clock outputs for the SDRAM, Processor bus, and PCI/X slots. A separate oscillator is required for the Gigabit Ethernet transceiver. All clock inputs are 1.8V except for the Ethernet reference clock (E\_125REF, 3.3V).

**Figure 3: Tsi109 System Clocking Distribution**



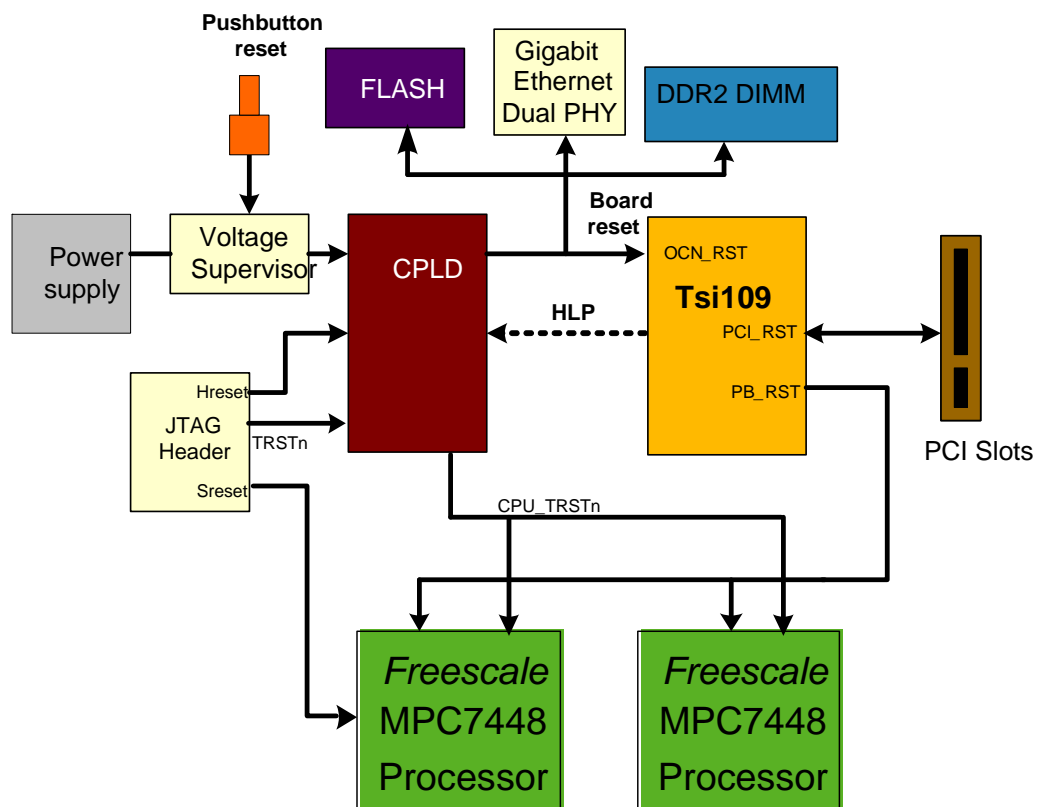
## 2.4 Board Reset Control

Net BOARD\_RESETh is the main reset signal across the reference board. It is generated from a voltage supervisor/reset controller circuit. The supervisor monitors the 3.3V rail, which is the last one to ramp up (according to the power sequencing requirement). As the rail reaches 3.3V, the supervisor holds the reset for about 100ms. A push-button switch also activates the reset signal from the voltage supervisor. The voltage supervisor reset is combined with the reset signal from the JTAG debugger tool in the CPLD. The CPLD generates the main board reset connected to all other components.

The Tsi109 controls the processor reset. When board reset is released, the Tsi109 will not release the processor reset until its PLLs have locked. The Tsi109 drives the PCI/X reset signal. The PCI/X Interface directs the board reset signal to the PCI/X bus.

Software reset to the processor is driven by JTAG based debugger. CPU TRSTn glue logic to support WindRiver debugger is implemented by CPLD.

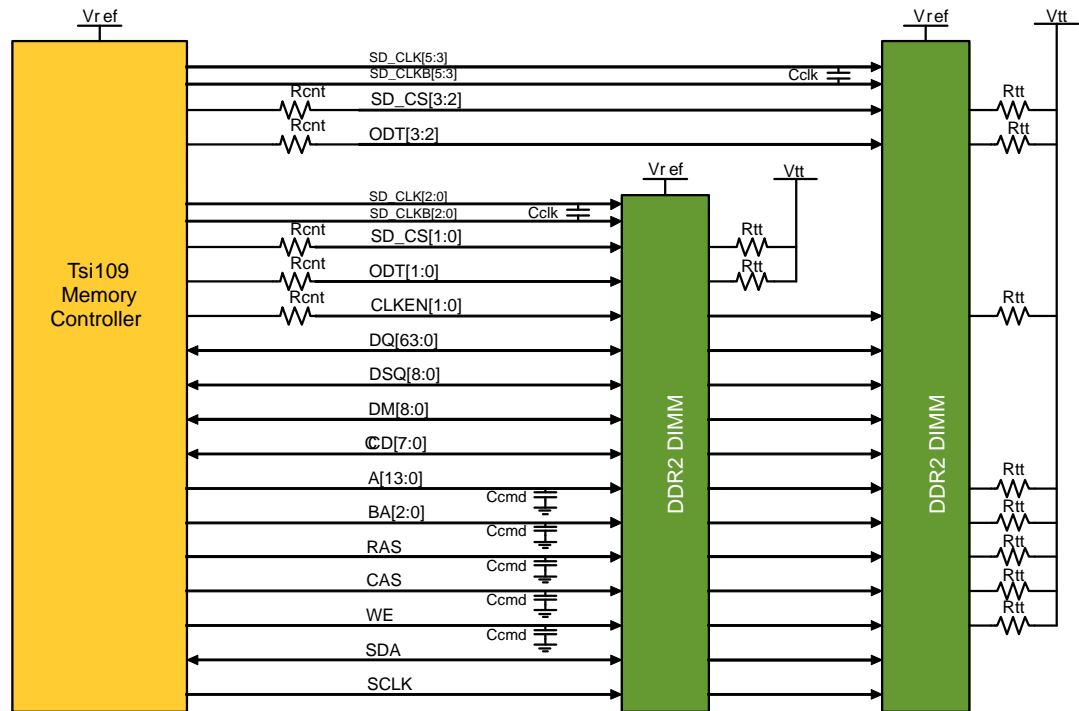
**Figure 4: Board Reset Control**



## 2.5 Memory Controller

The reference board incorporates two DDR2 DIMM connectors and the appropriate termination circuit. The Tsi109 supports two registered DIMMs at full DDR2-400 speed, and supports 2G of addressing space. The connection diagram displayed in **Figure 5** describes the connection between the Tsi109 Memory Controller and the DDR2 slots. Vtt and Vref are generated by a SSTL\_18 specific regulator, LP2997 from National Semiconductor.

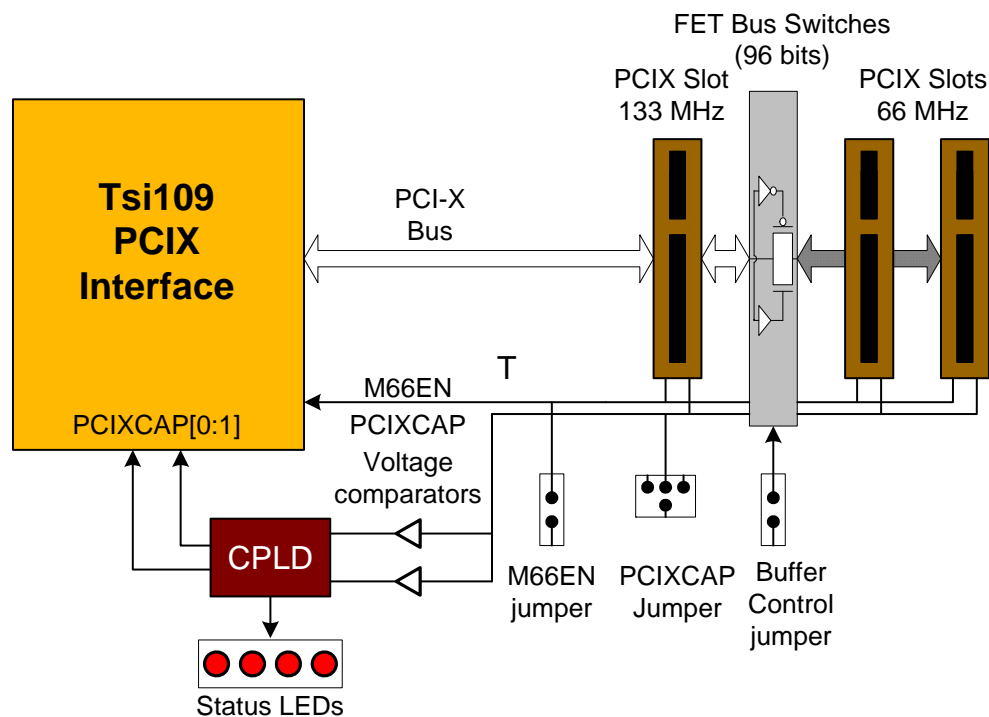
**Figure 5: Tsi109 Memory Controller**



## 2.6 PCI/X Bus

Three PCI/X slots are available on the reference board. The slot closest to the Tsi109 is designed to meet 133MHz PCI-X timing. This slot is isolated from the other slots by a FET bus switch. The FET switch reduces the load and the stub length seen from the Tsi109. The FETs are on (passing traffic) when the jumper is present. The FETs are off (isolating slot 1 from the other two) only when the jumper is off. The capacitive load is 4pF (in off state) and the propagation delay is 200ps.

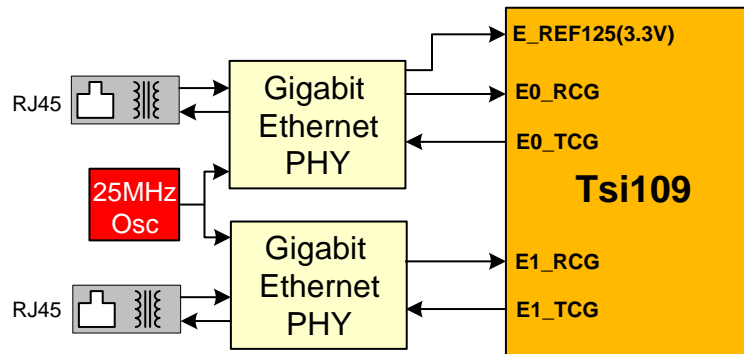
**Figure 6: Board PCI/X Bus**



## 2.7 Ethernet Interface

The Ethernet circuit is composed of two RJ45 connectors (with LEDs); isolation transformers, and two single Broadcom 10/100/1000BASE-T Ethernet copper transceivers (BCM5461). The clock source is a single 25MHz oscillator driving the two transceivers. One 125MHz reference clock output from the transceivers is connected to the Tsi109.

**Figure 7: Tsi109 Ethernet Interface**



## 2.8 CPLD Function

The target CPLD is a Xilinx CoolRunner XC2C32A-VQ44. The functions of the CPLD are:

- Reset control
- Processor bus and address mode control
- PCI/X slot capability detection
- LED driver

## 2.9 FLASH, SRAM, and NVRAM Memory

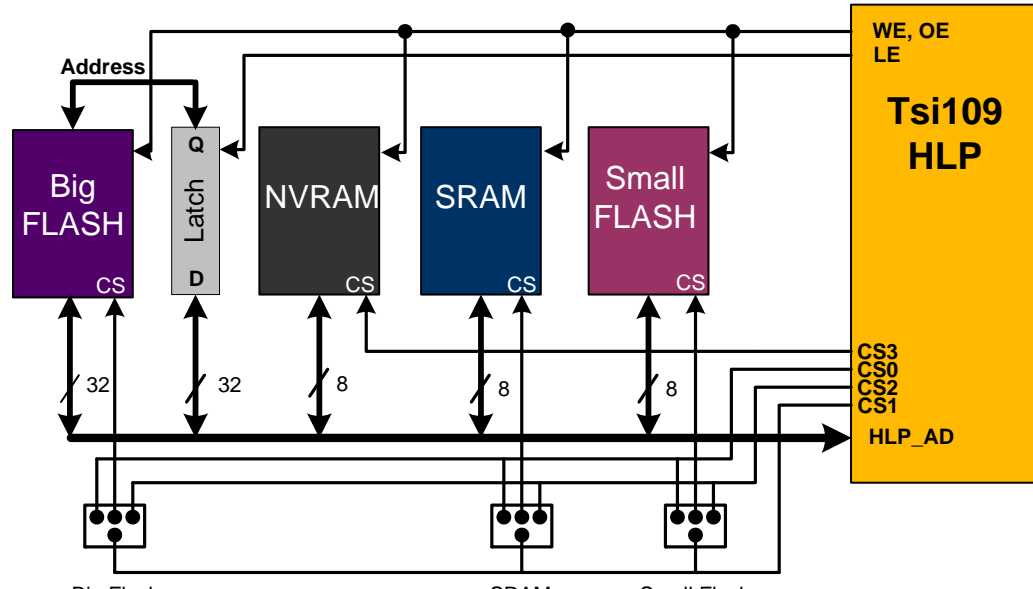
The non-volatile memory configuration is as follows:

- Big FLASH configuration is two 8Mx16 FLASH from Intel (28F128J). The data bus width is 32 bit. The two FLASH devices share the same chip select.
- Small FLASH is composed of one socket 512-Kbyte FLASH from AMD (Am29LV040B) in PLCC package. The data bus width is 8 bit.
- SRAM is composed of one 512Kx8 chips from Samsung. The data bus width is 8 bits.
- NVRAM is composed of a single 32Kx8 FRAM (Ferroelectric RAM) from RAMTRON (FM18L08-70S).

The memory devices are connected on Tsi109's Host Local Port (HLP). Each memory "type" is connected to a separate Chip Select output of the Tsi109. The default Chip Select assignment is:

- Small FLASH on CS0
- Big FLASH on CS1
- SRAM on CS2
- NVRAM on CS3

**Figure 8: Board Boot Memory Topology**





## 2.10 RS-232 Ports

The dual RS-232 ports are connected to two separate DB9 connectors. One dual RS-232 transceiver is required to do RS-232 level conversion. The DB9 connector pin-out is compliant with standard RS-232 DB9 null-model cables.

## 2.11 SEEP and Real-time Clock

One Serial EEPROM (SEEP) is connected on the Tsi109 I<sup>2</sup>C chain. The device (24LC16) from Microchip is used to store configuration information for the Tsi109. The real-time clock device is on the same I<sup>2</sup>C chain as the SEEP. The DS1337 provides time of day and date information.

## 2.12 Power Supply

### 2.12.1 Power Requirement

The power requirement is calculated from “worst case” figures from the component datasheets. The challenge is to properly evaluate the SDRAM requirement. The unknown parameters are the type of DIMMs populated (a 2G DIMM draws much more current than a 256K) and the actual activity on each DIMM.

**Table 6: Power Requirements**

| Device           | 1.2V | 1.1V    | 1.8V | 2.5V | 3.3V   | 5V   | +/-12V | Notes    |
|------------------|------|---------|------|------|--------|------|--------|----------|
| Tsi109           | 1122 | -       | 1200 | -    | 735    | -    | -      |          |
| MPC7448X2        | -    | 15000X2 | 185  | -    | -      | -    | -      | MPC7447A |
| DDR2 DIMM (x2)   | -    | -       | 3800 | -    | -      | -    | -      |          |
| GigE PHYs (x2)   | 500  | -       | -    | 200  | 450    | -    | -      |          |
| PCI/X Slot (x3)  | -    | -       | -    | -    | (7.6A) | (5A) | (0.5A) |          |
| Xilinx CPLD      | -    | -       | 100  | -    | 100    | -    | -      |          |
| AMD Flash (x2)   | -    | -       | -    | -    | 120    | -    | -      |          |
| Intel Flash (x2) | -    | -       | -    | -    | 160    | -    | -      |          |
| SRAM (x2)        | -    | -       | -    | -    | 60     | -    | -      |          |
| NVRAM            | -    | -       | -    | -    | 15     | -    | -      |          |
| FET busSw (x3)   | -    | -       | -    | -    | 40     | -    | -      |          |
| Bus Latch        | -    | -       | -    | -    | 1      | -    | -      |          |
| RS232 trans      | -    | -       | -    | -    | 1      | -    | -      |          |

**Table 6: Power Requirements (Continued)**

| Device      | 1.2V   | 1.1V    | 1.8V   | 2.5V  | 3.3V   | 5V  | +/-12V | Notes     |
|-------------|--------|---------|--------|-------|--------|-----|--------|-----------|
| Cooling Fan | -      | -       | -      | -     |        | -   | -      |           |
| TOTAL (A)   | 1622mA | 30000mA | 5285mA | 200mA | 1682mA | -   | -      |           |
| TOTAL (W)   | 1.95W  | 33W     | 9.5W   | 0.5W  | 5.5W   | -   | -      | Total 51W |
| ATX SUPPLY  | -      | -       | -      | -     | 30A    | 30A | -      |           |

DDR2 power is based on 512M registered modules. 2000mA/rank is an average between Operating Burst Write current and Burst Refresh Current. The maximum current is based on one rank because ranks and banks not accessed simultaneously. Then 500mA is added for active standby current per rank (total 1500mA). 300mA is added for Vtt supply.

### 2.12.2 Power Sequencing Requirement

The Tsi109 power-sequencing requirement is:

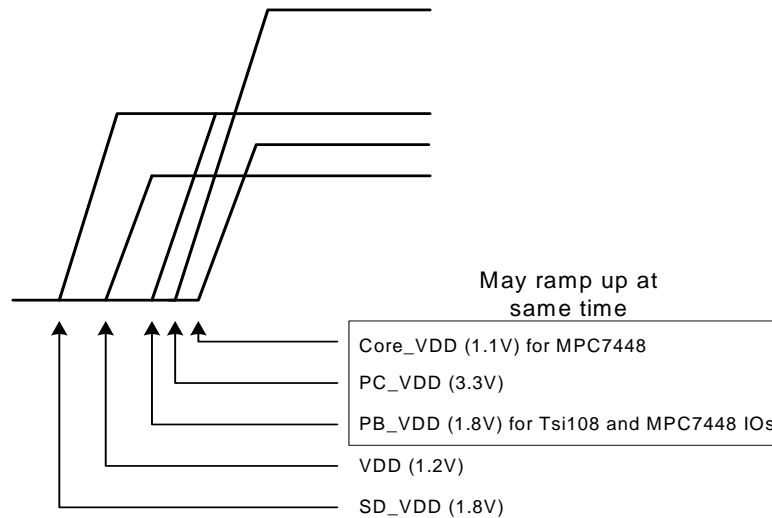
- SD\_VDD (1.8V) ramps up before VDD (1.2V)
- PB\_VDD (1.8V) and PC\_VDD (3.3V) ramp up after VDD.

The MPC7448 power-sequencing requirement is

- OVDD (1.8V) powers up before or at the same time as VDD (1.1V). (VDD must not exceed OVDD by more than 1V)

The combined power-up sequence diagram is displayed in **Figure 9**. The power sequencing circuit has to control two stages of power sequence:

1. Detect SD\_VDD (1.8V) good, and enable VDD (1.2V)
2. Detect VDD (1.2V) good and enable the rest of the rails

**Figure 9: Board Power-on Sequencing**

### 2.12.3 Power Supply Design

The power source is ATX power supply. The 5V, 3.3V, and +/-12V rails are directly connected to the PCI/X slots. All other rails, except for 3.3V, are regulated on the reference board.

The reference board is turned on/off with a push-button.

The first supply to ramp up on the reference board is the SD\_VDD (1.8V) rail. It drives the DIMM modules and the Tsi109 SDRAM I/Os. Due to power sequencing requirements, this rail has to come up first. Its output is used to enable the Tsi109\_core (1.2V) supply. An Austin MicroLynx adjustable module that can provide up to 5A of current supplies SD\_VDD.

A small adjustable switching regulator provides sufficient current for the Tsi109 core voltage (VDD, 1.2V). The Enable input has to be >4.5V for the device to turn on. A Level shifter (FET) is used to drive the Enable pin.

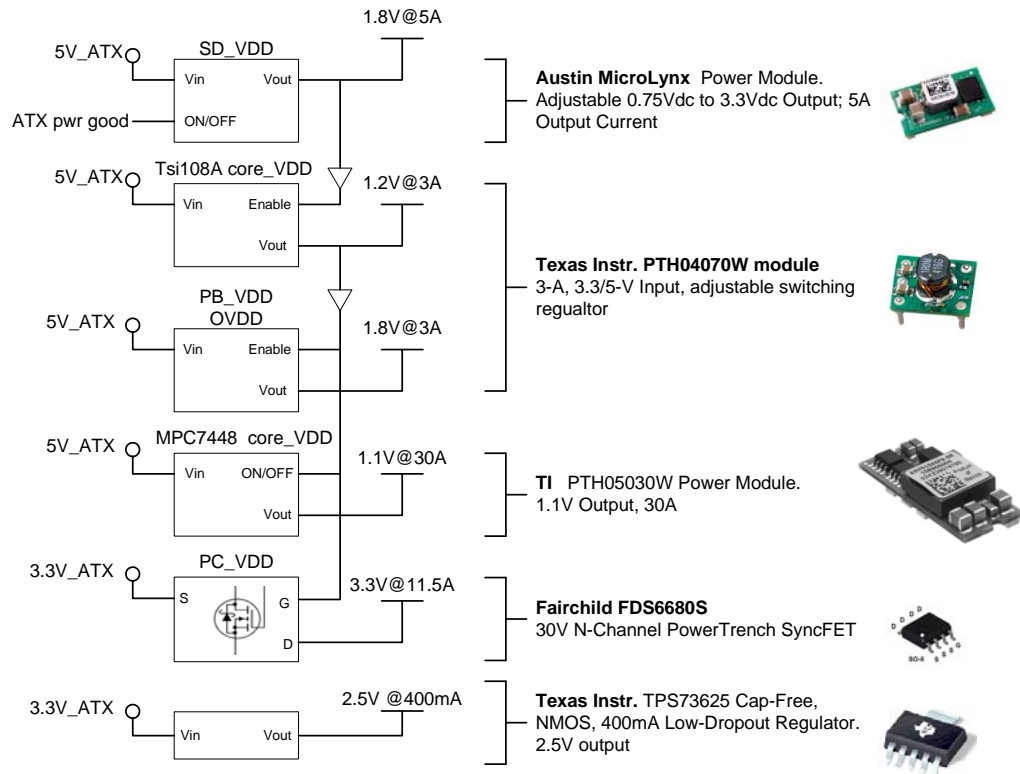
The 1.8V rail for the processor interfaces (PB\_VDD and OVDD) is supplied by a switching regulator of the same type as VDD. The regulator is enabled from the VDD rail, again with a level shifter.

The processor core is supplied with TI DC/DC switching module. The module is adjustable and can provide up to 30A and any voltage in its output range. It is tracking Tsi109 VDD\_PB power supply.

To maintain proper power sequencing, the 3.3V rail of the Tsi109 has to be delayed until VDD (Tsi109 core) is up. A pair of MOSFET is used to gate the 3.3V rail until VDD is up. The transistor can drive 11Amps.

A small LDO is used to generate 2.5V for the Ethernet PHY.

**Figure 10: Power Regulator Selection**



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