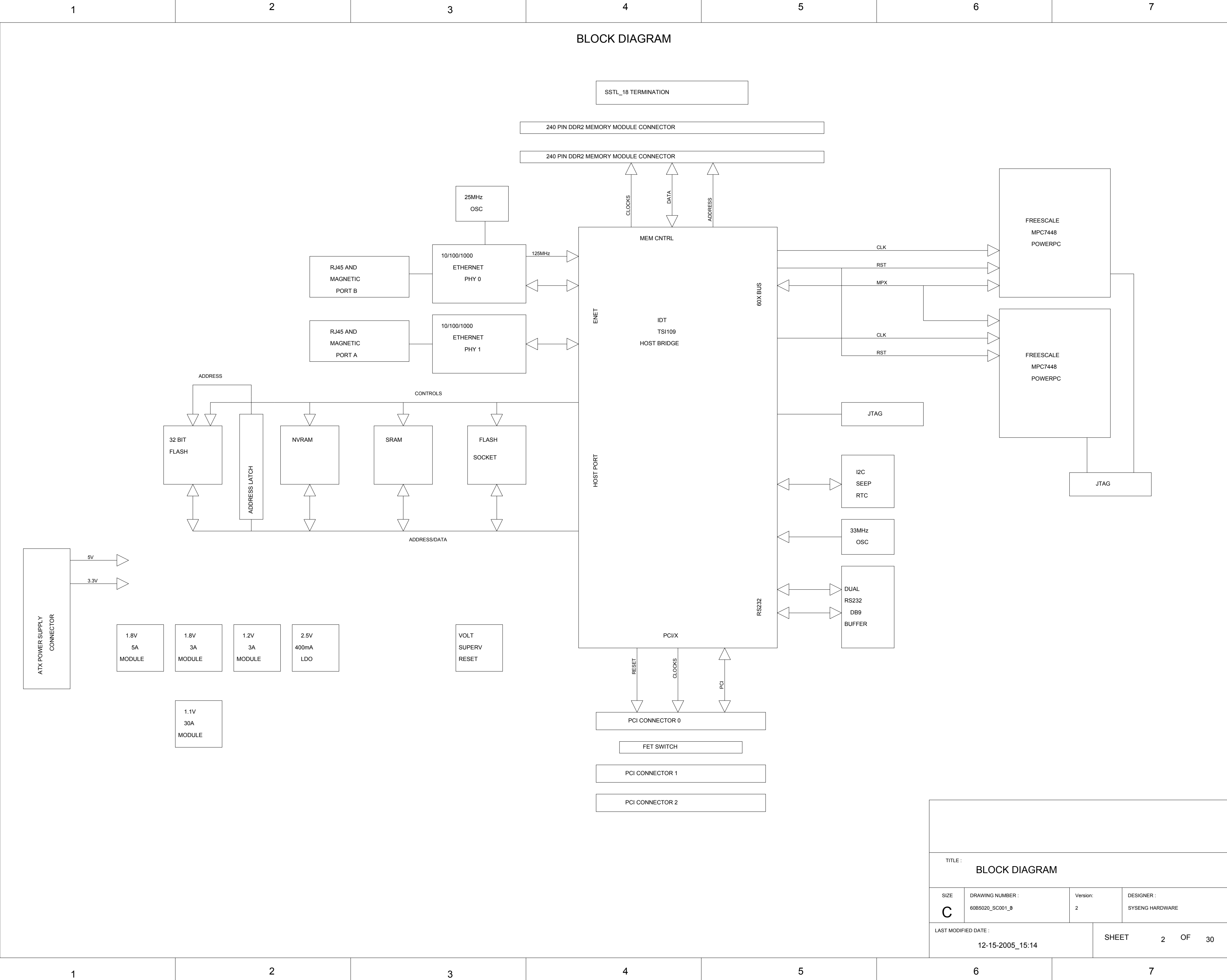


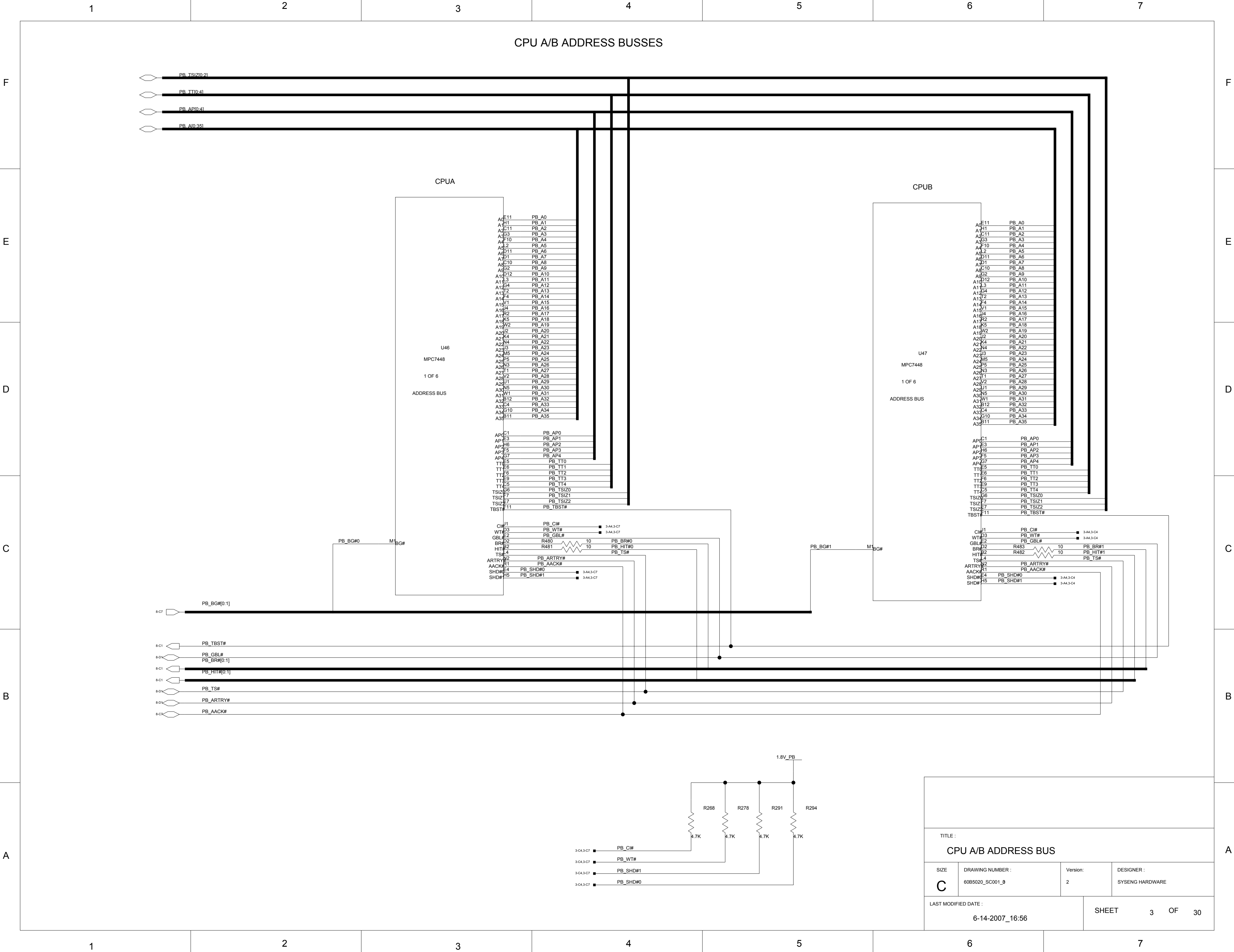
# TSI109 Dual MPC7448 Reference Design Schematic

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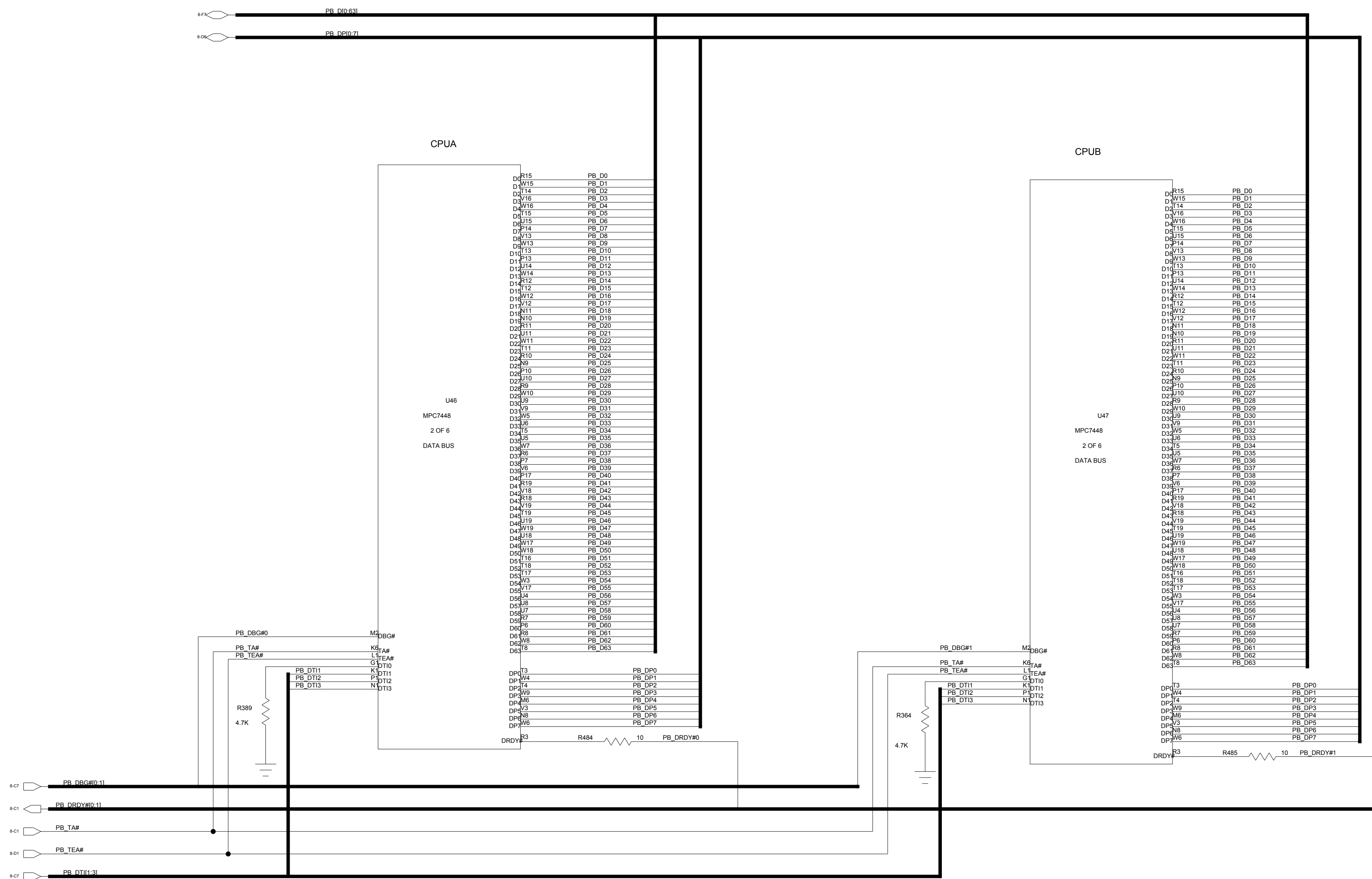
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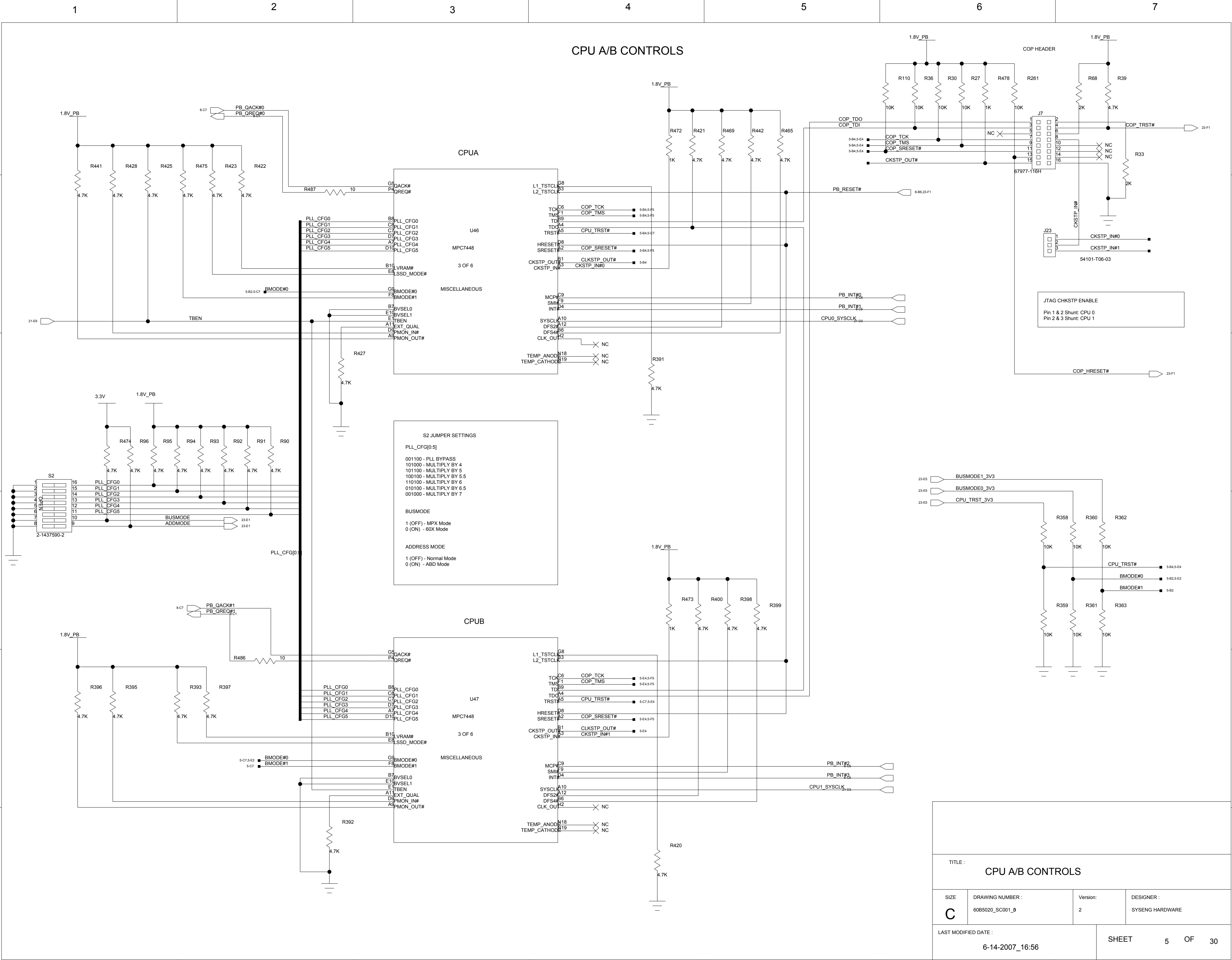
TITLE : INDEX			
SIZE C	DRAWING NUMBER : 60B5020_SC001_0	Version: 2	DESIGNER : SYSENG HARDWARE
LAST MODIFIED DATE : 12-15-2005_15:14		SHEET 1 OF 30	



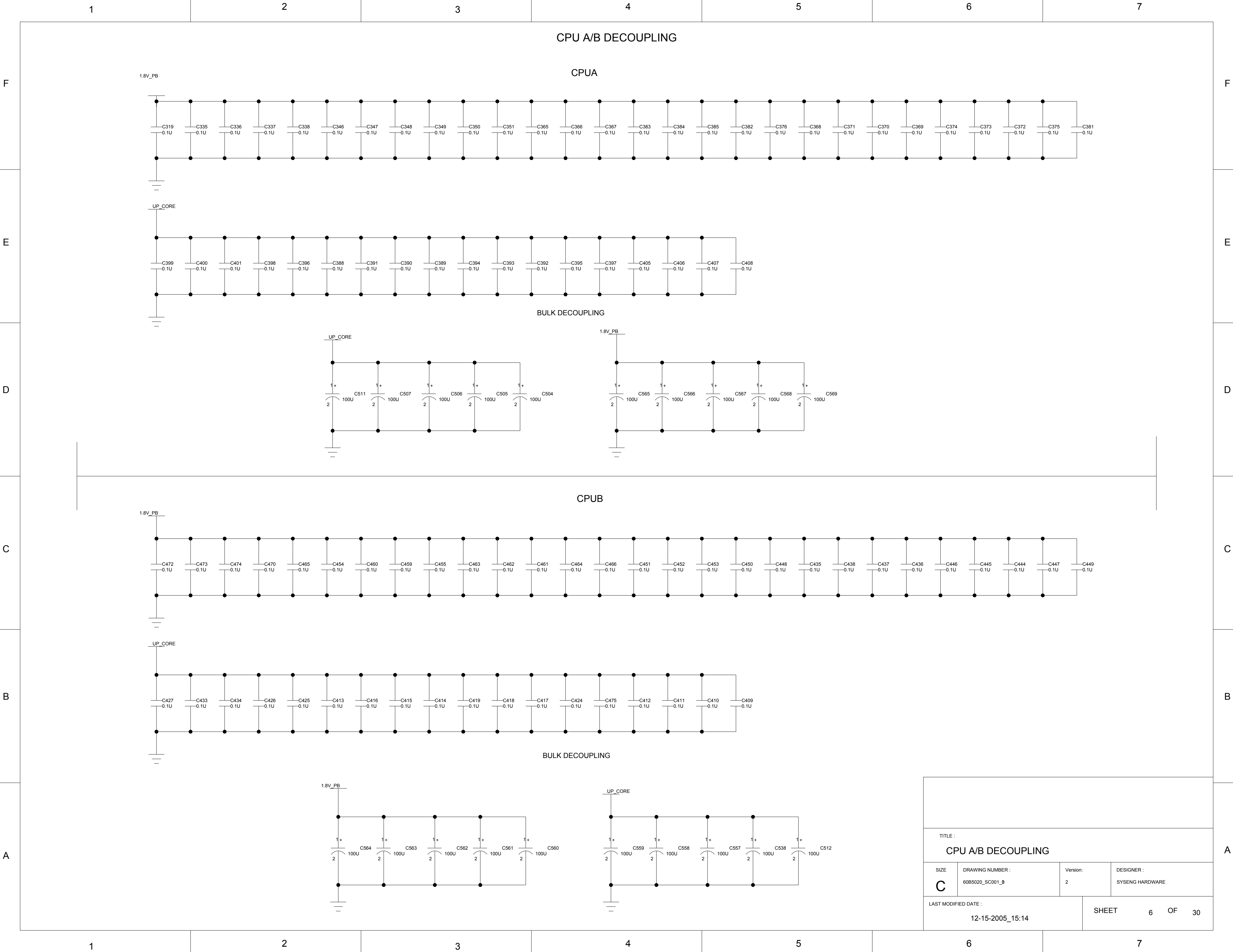


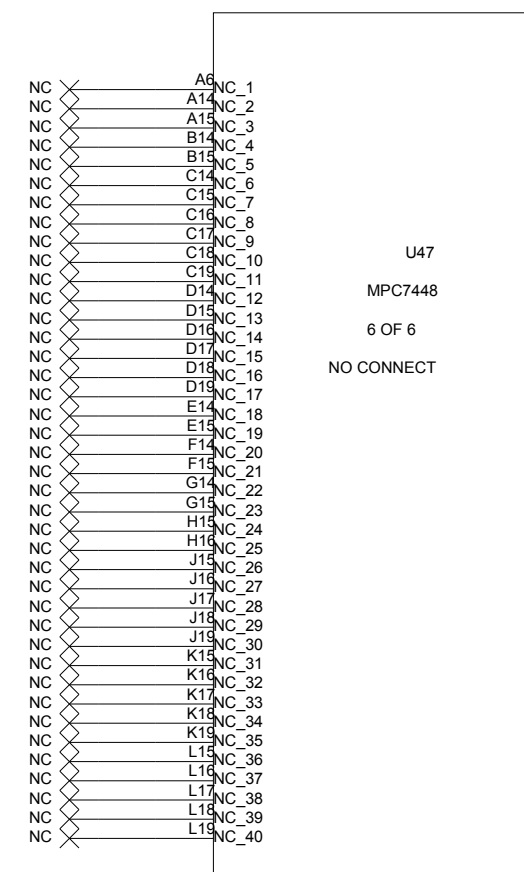
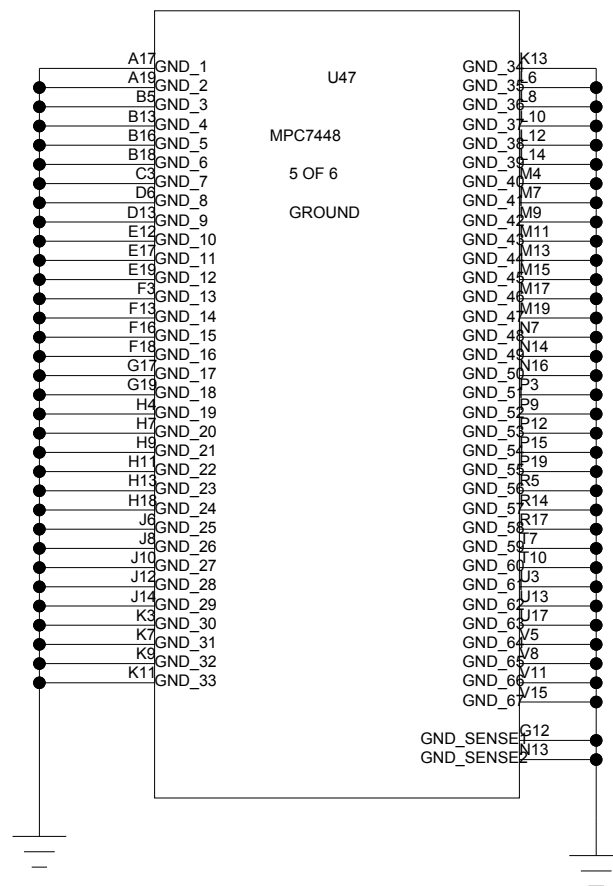
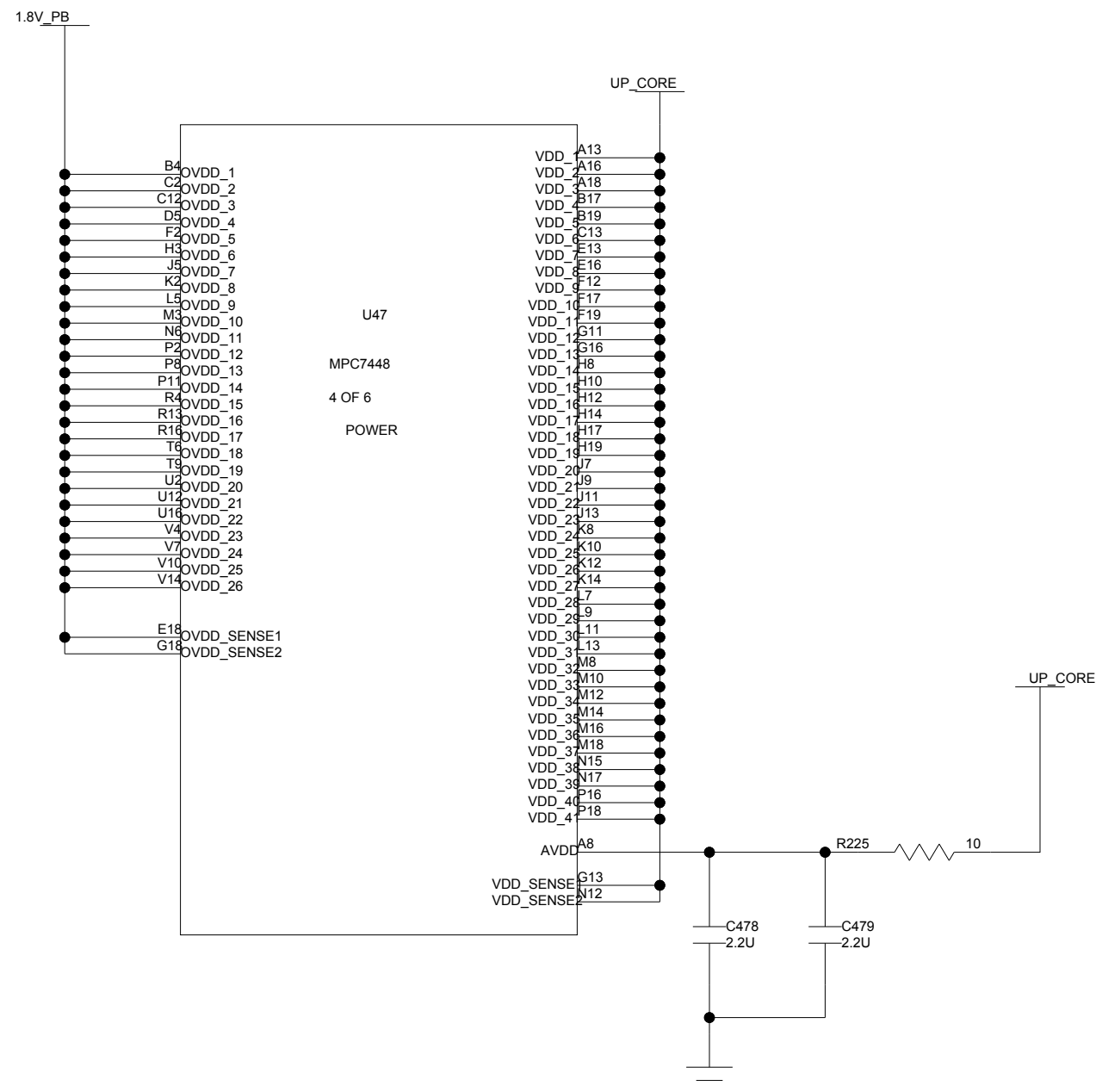
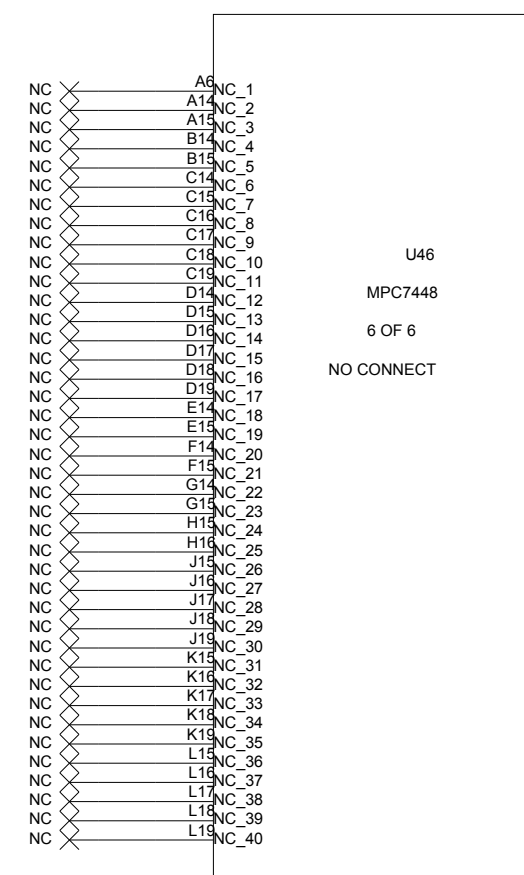
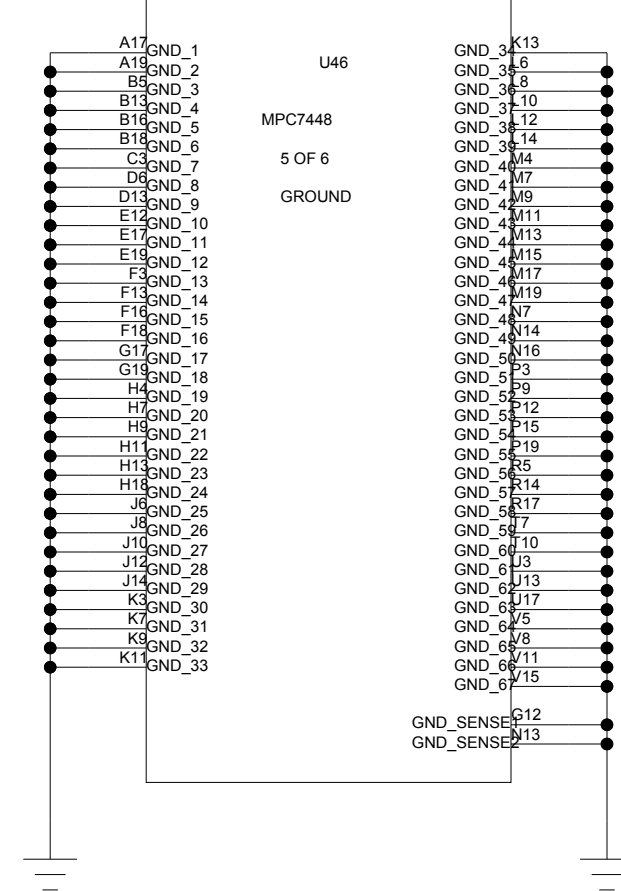
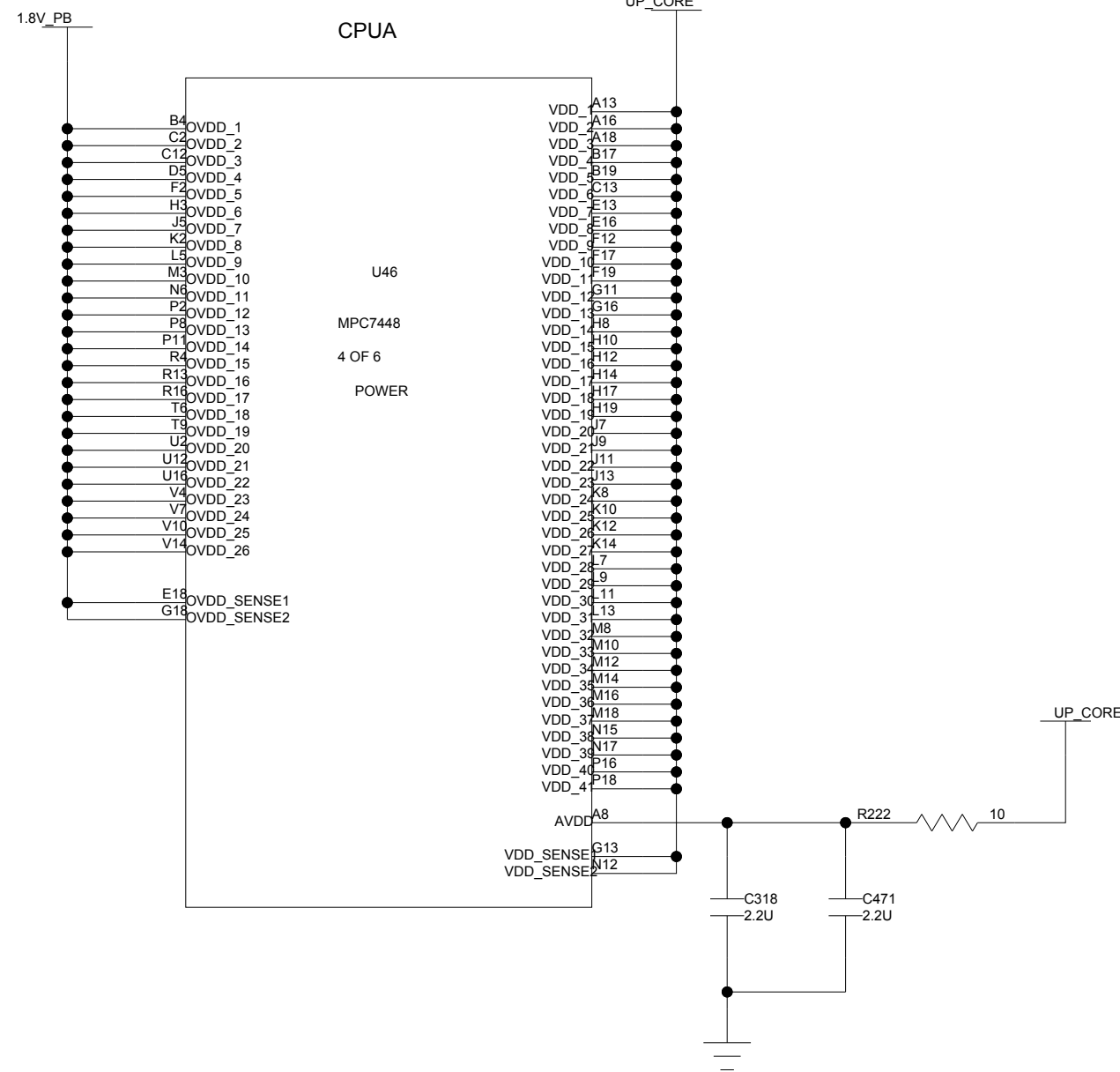
## CPU A/B DATA BUSES





TITLE : CPU A/B CONTROLS			
SIZE C	DRAWING NUMBER : 60B5020_SC001_0	Version: 2	DESIGNER : SYSENG HARDWARE
LAST MODIFIED DATE : 6-14-2007_16:56		SHEET 5 OF 30	





TITLE :			
CPU A/B POWER/GROUND/NC			
SIZE <b>C</b>	DRAWING NUMBER : 60B5020_SC001_9	Version: 2	DESIGNER : SYSENG HARDWARE
LAST MODIFIED DATE : 12-15-2005_15:14		SHEET 7 OF 30	

TITLE :			
TSI109 PB INTERFACE			
SIZE <b>C</b>	DRAWING NUMBER : 60B5020_SC001_0	Version: 2	DESIGNER : SYSENG HARDWARE
LAST MODIFIED DATE : 6-14-2007_16:56		SHEET 8	



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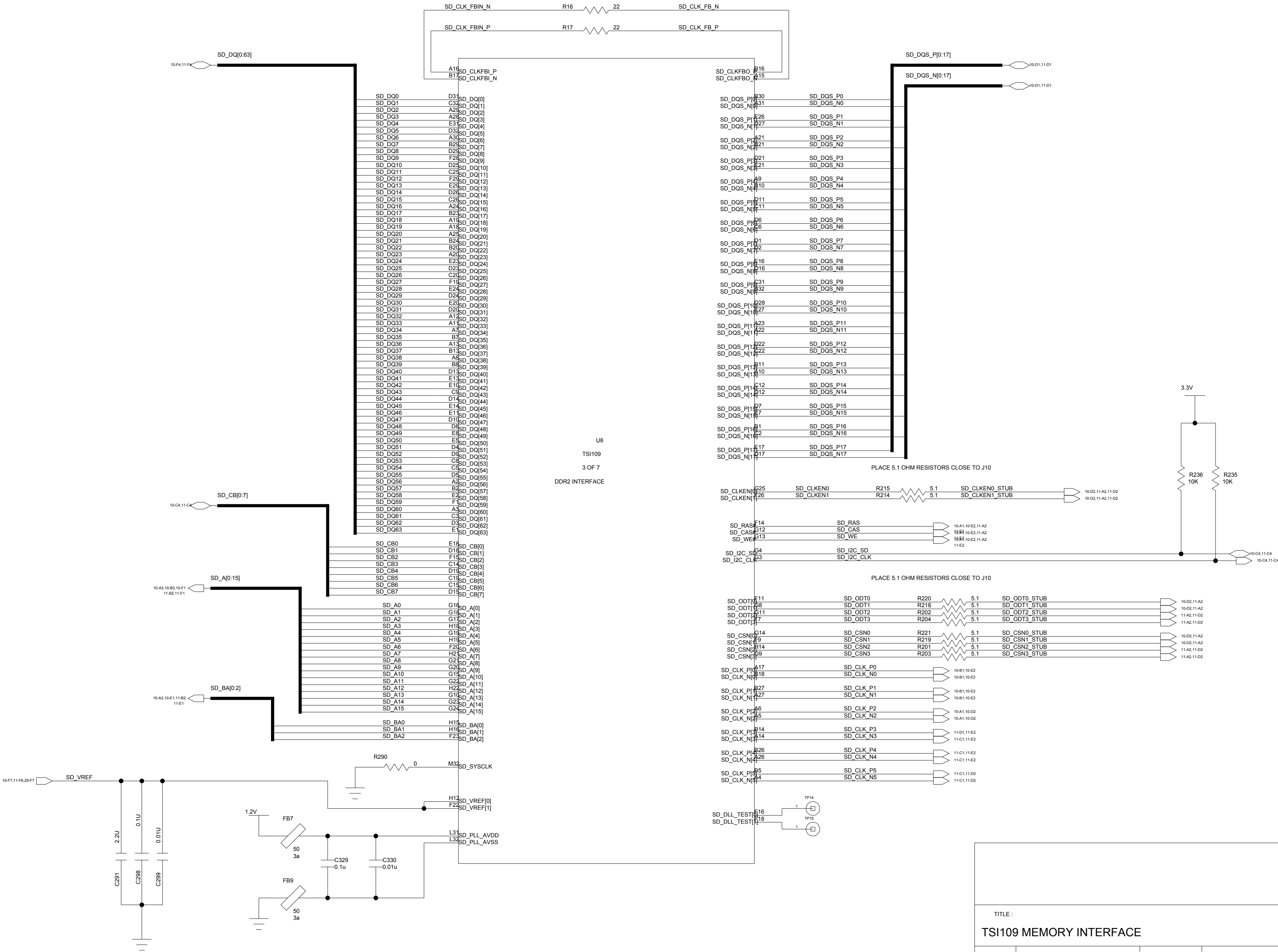
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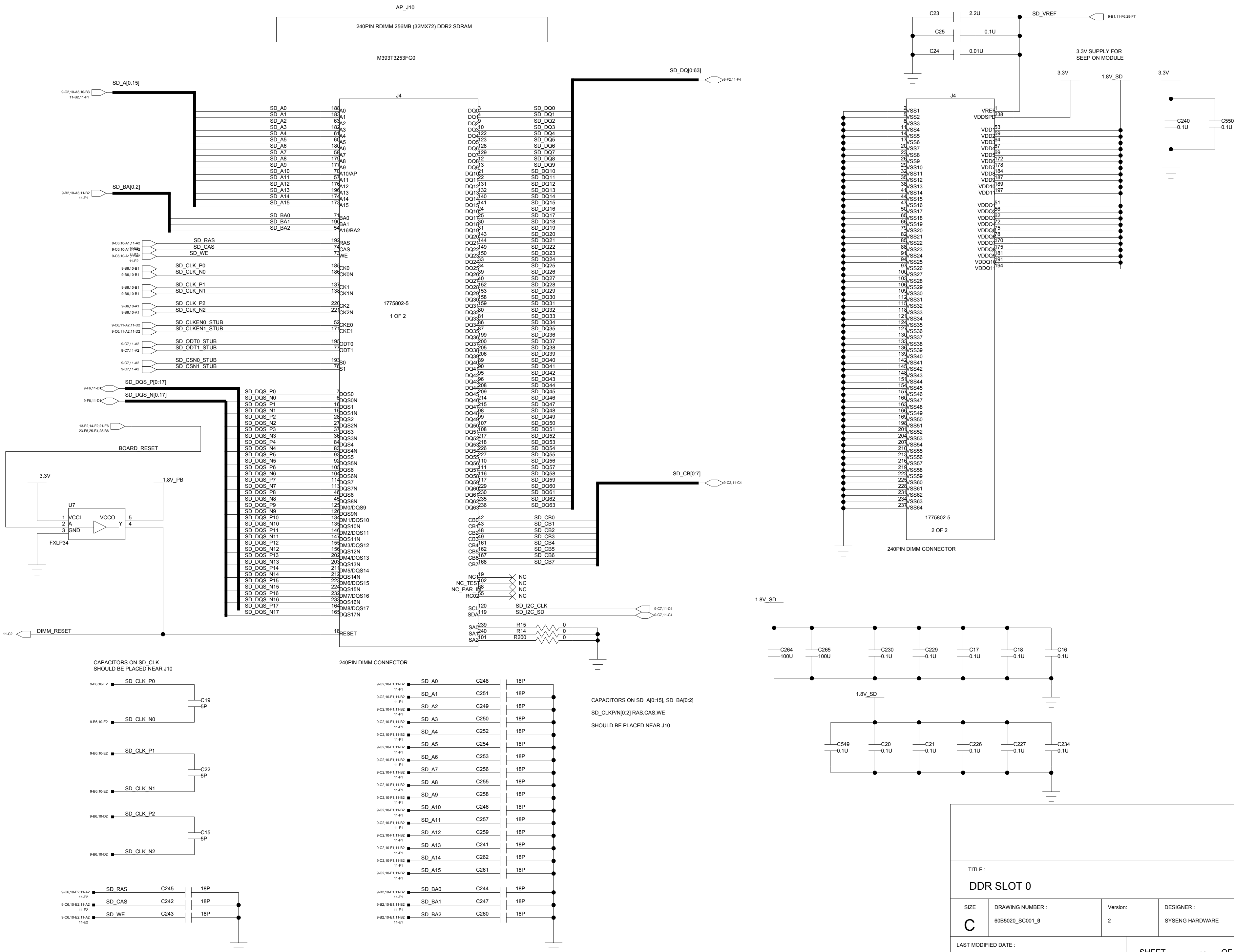
A

TSI109 MEMORY INTERFACE



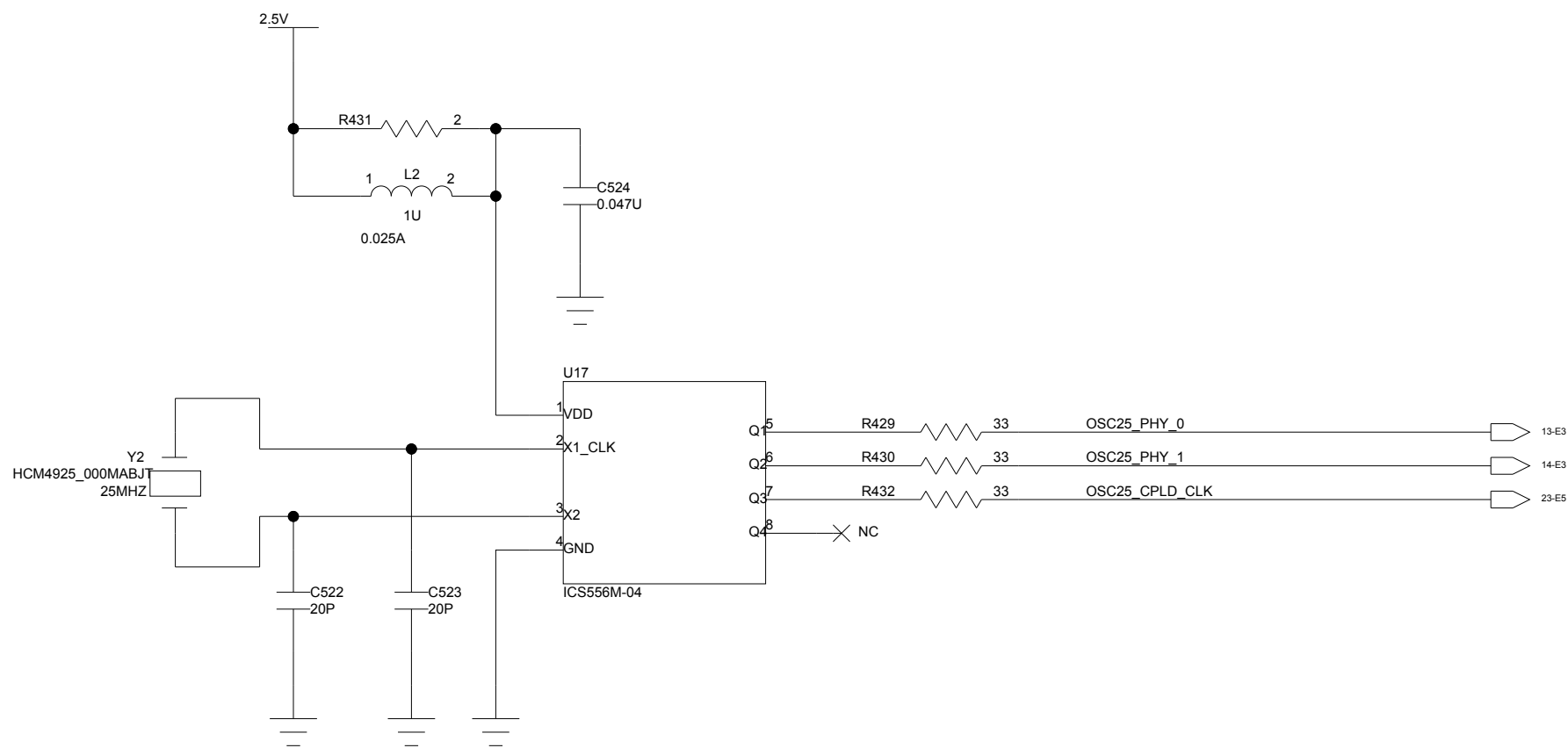
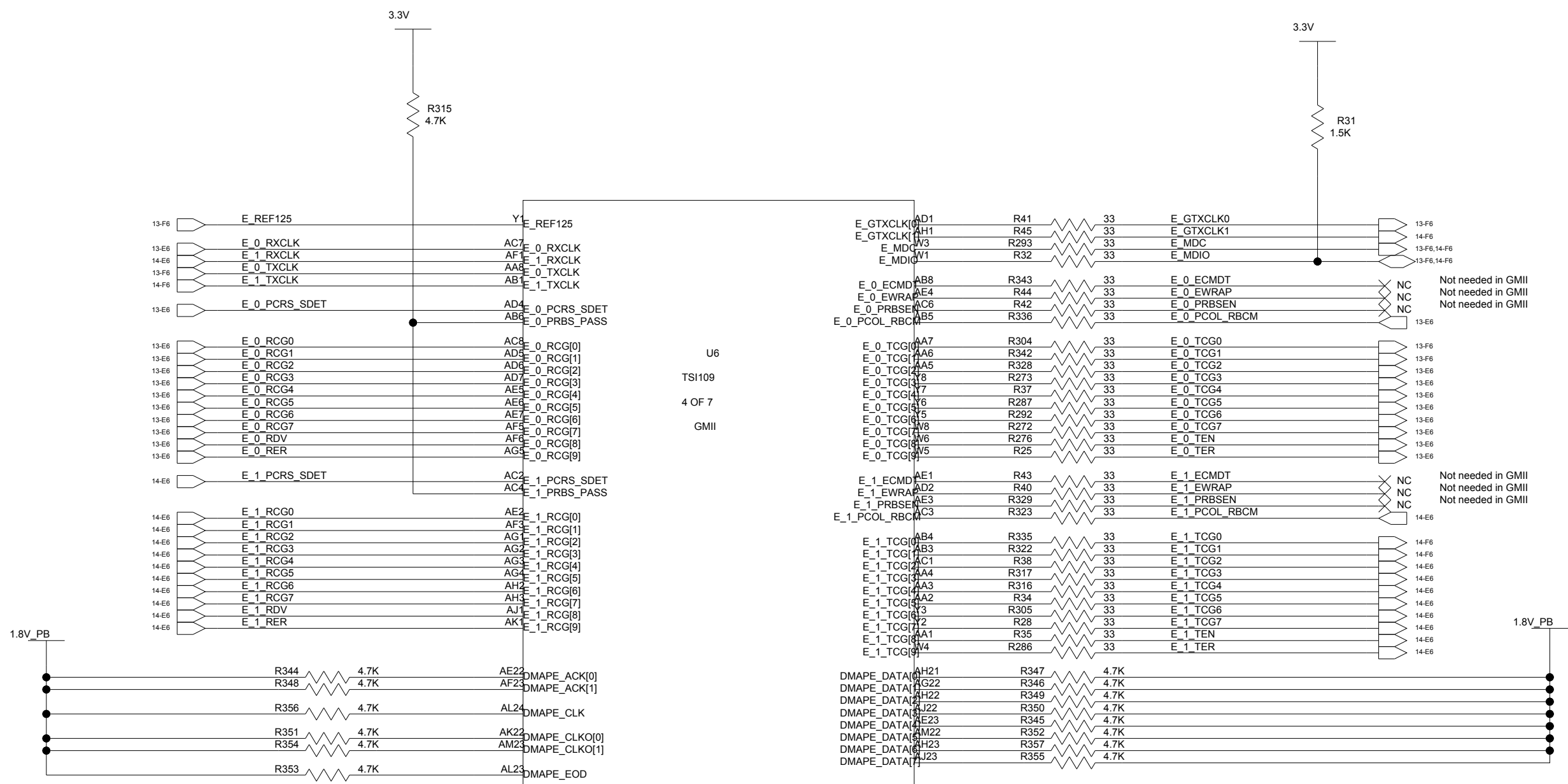
TITLE :			
TSI109 MEMORY INTERFACE			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60B5020_SC001_0	2	SYSENG HARDWARE
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DDR2 DIMM CONNECTOR SLOT 0

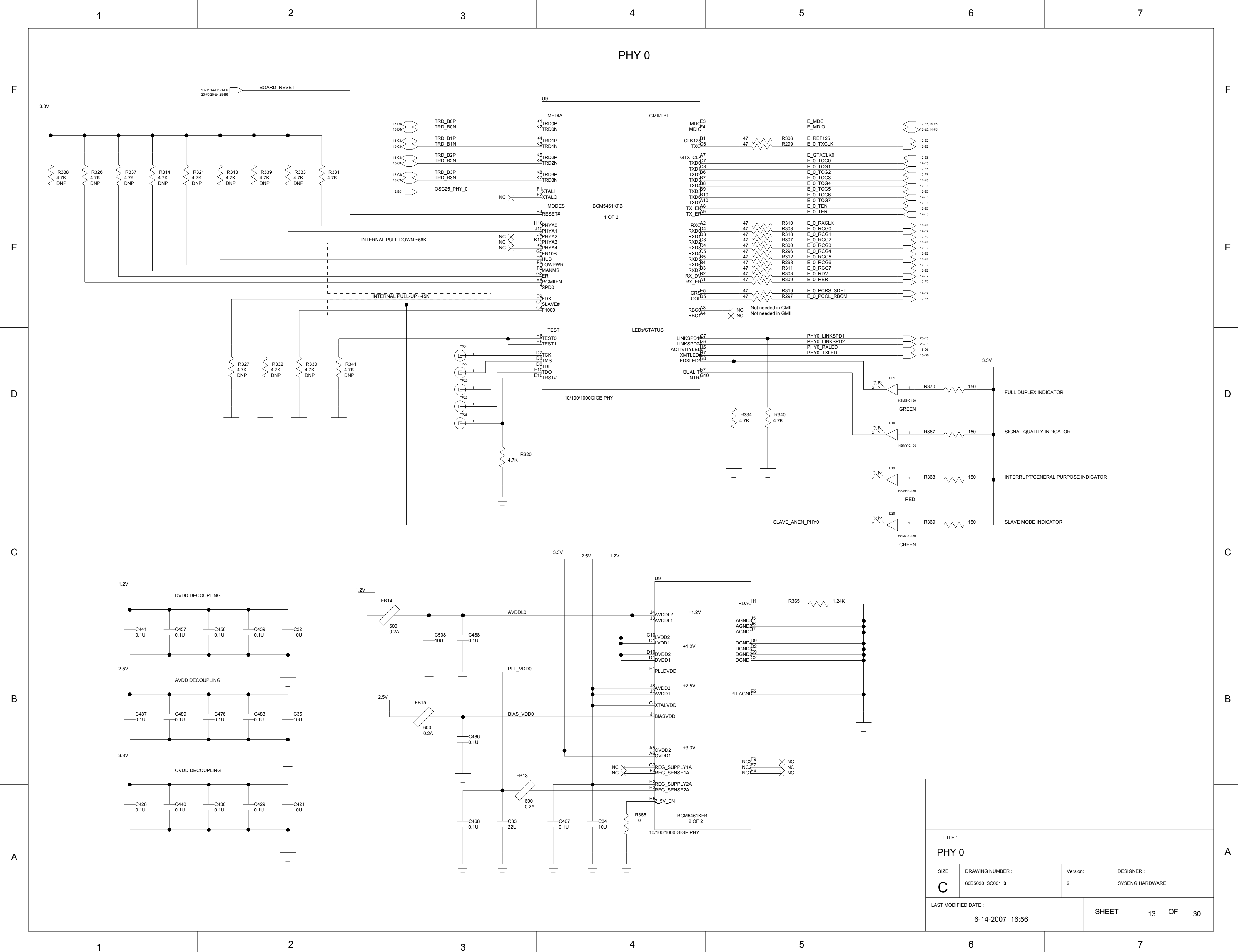


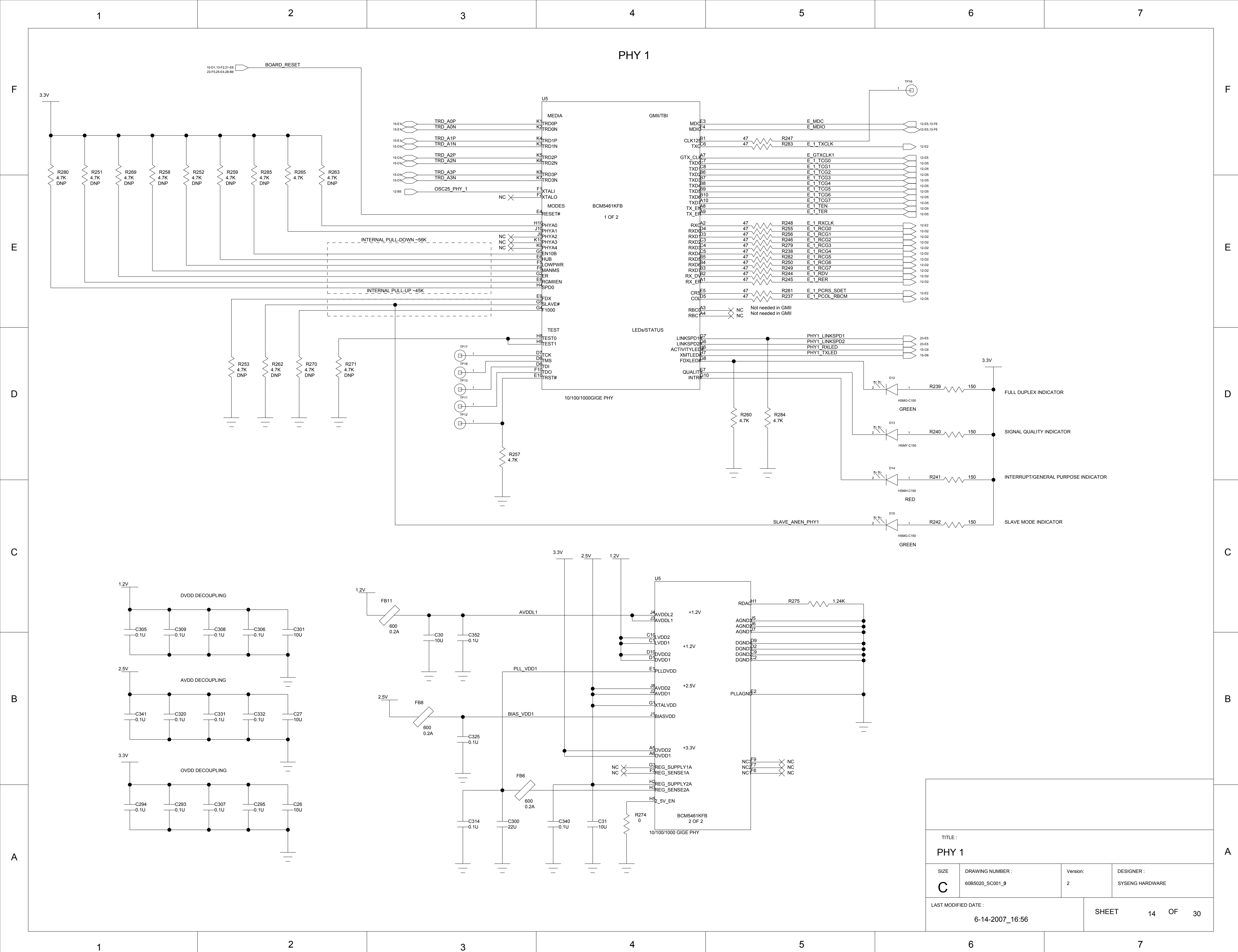


TSI109 ETHERNET INTERFACE



TITLE :			
TSI109 ETHERNET			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60B5020_SC001_0	2	SYSENG HARDWARE
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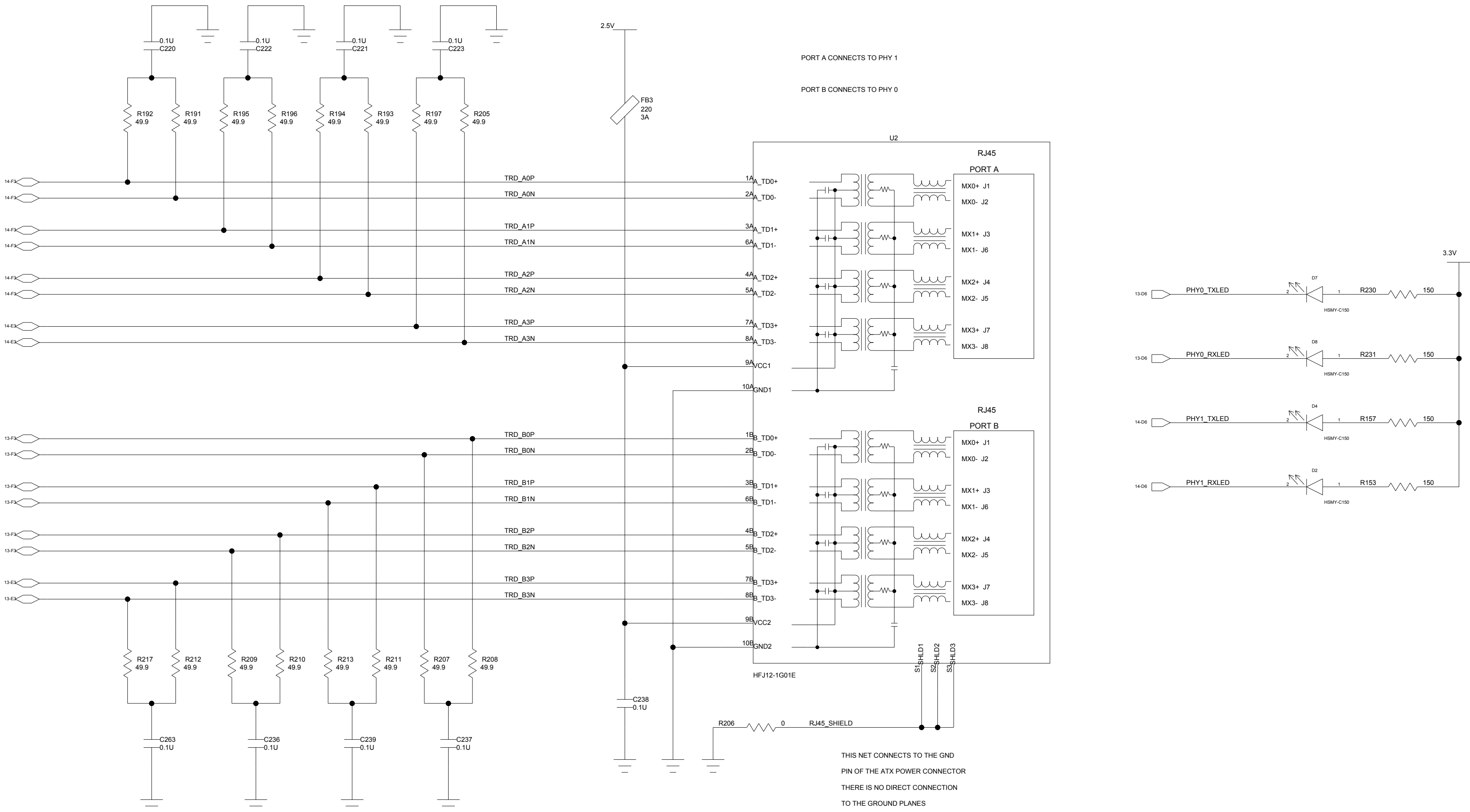
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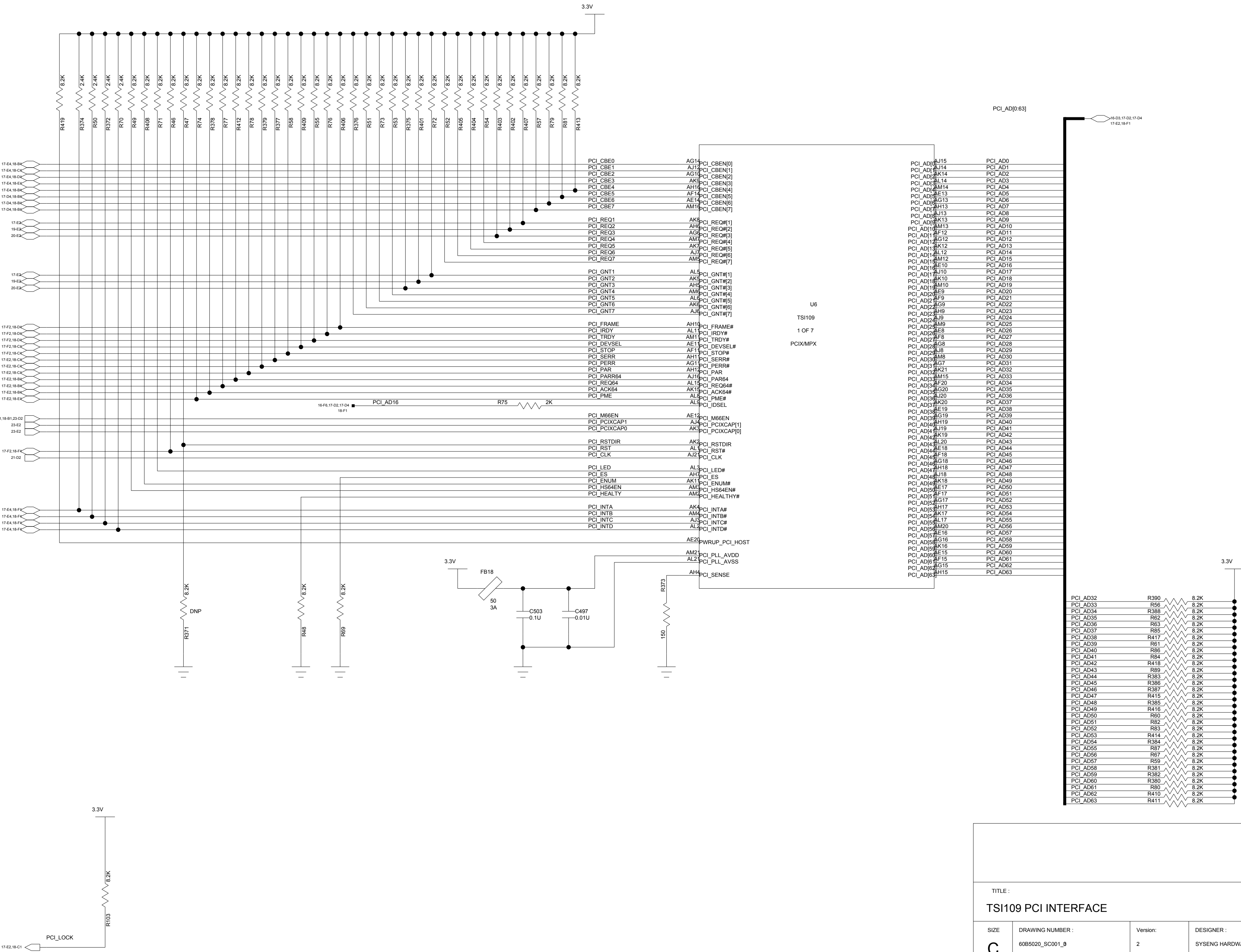
A

RJ45 AND MAGNETICS



TITLE :			
RJ45/MAGNETICS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60B5020_SC001_0	2	SYSENG HARDWARE
LAST MODIFIED DATE :			SHEET
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TSI109 PCI INTERFACE



TITLE :			
TSI109 PCI INTERFACE			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60B5020_SC001_0	2	SYSENG HARDWARE
LAST MODIFIED DATE :		SHEET	
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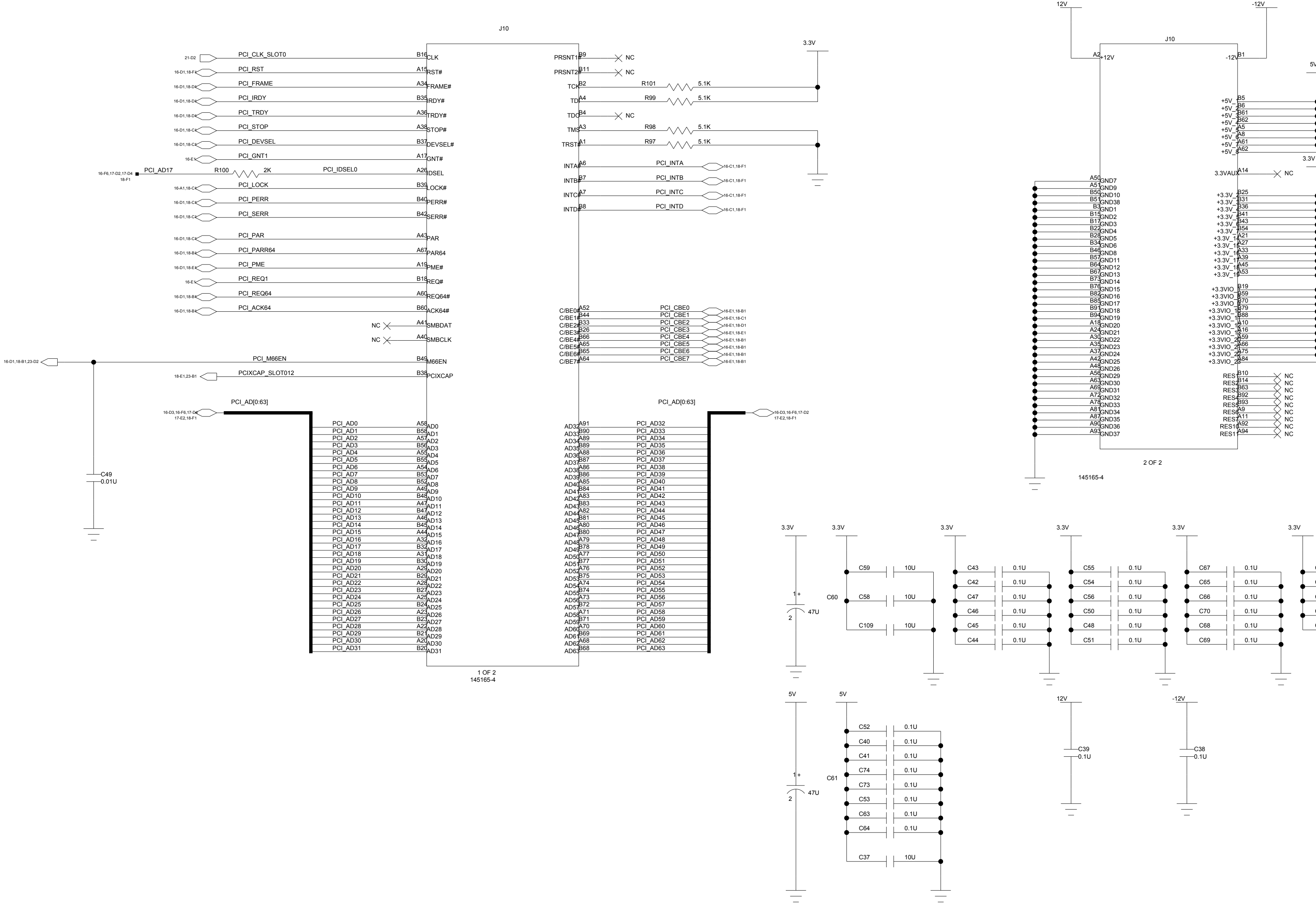
D

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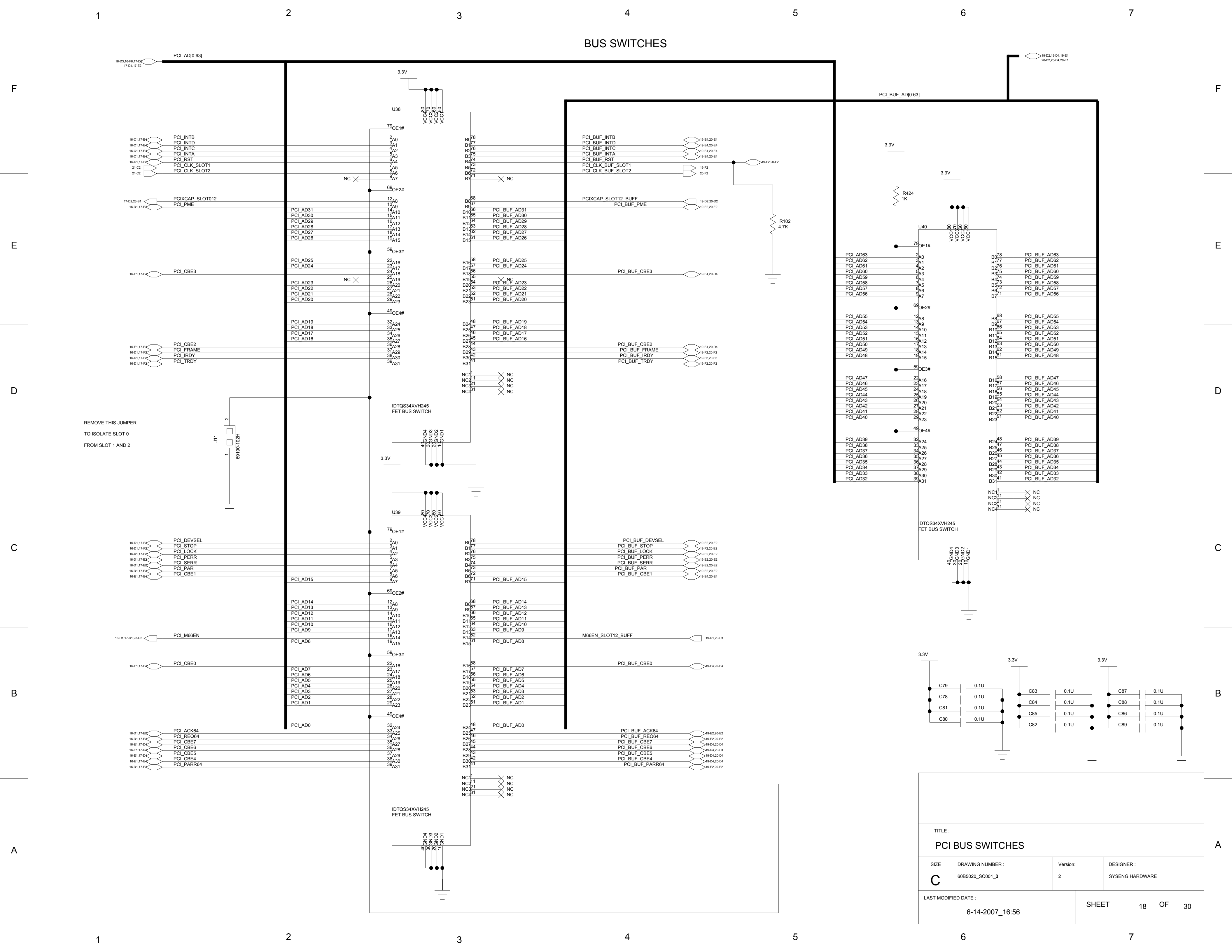
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PCI SLOT 0



TITLE : PCI SLOT 0			
SIZE C	DRAWING NUMBER : 60B5020_SC001_0	Version: 2	DESIGNER : SYSENG HARDWARE
LAST MODIFIED DATE : 6-14-2007_16:56		SHEET 17 OF 30	



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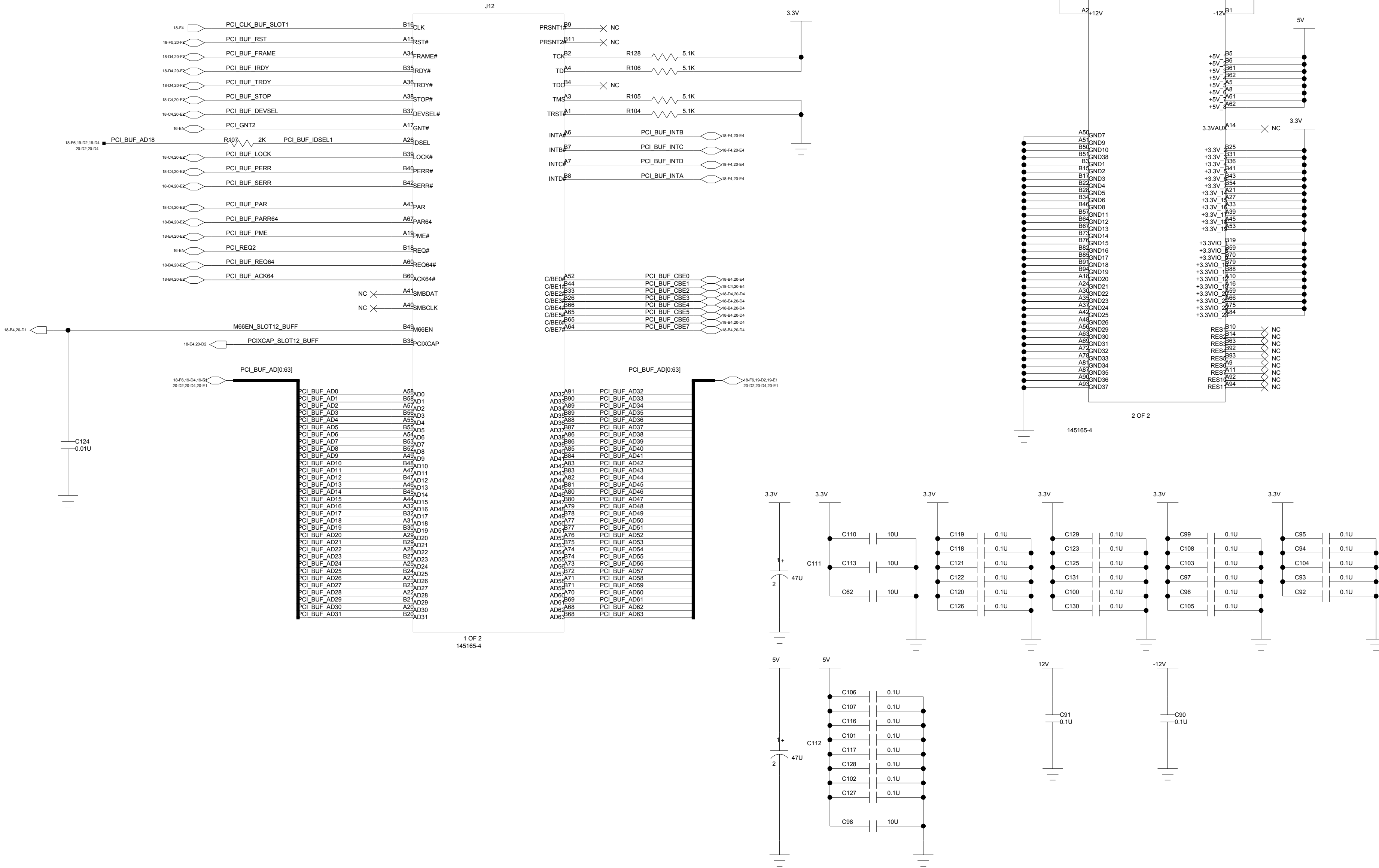
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Note: IDSEL resistor should be 100 Ohms for PCI and 2K for PCIX

PCI SLOT 1



TITLE : PCI SLOT 1			
SIZE C	DRAWING NUMBER : 60B5020_SC001_0	Version: 2	DESIGNER : SYSENG HARDWARE
LAST MODIFIED DATE : 6-14-2007_16:56		SHEET 19 OF 30	

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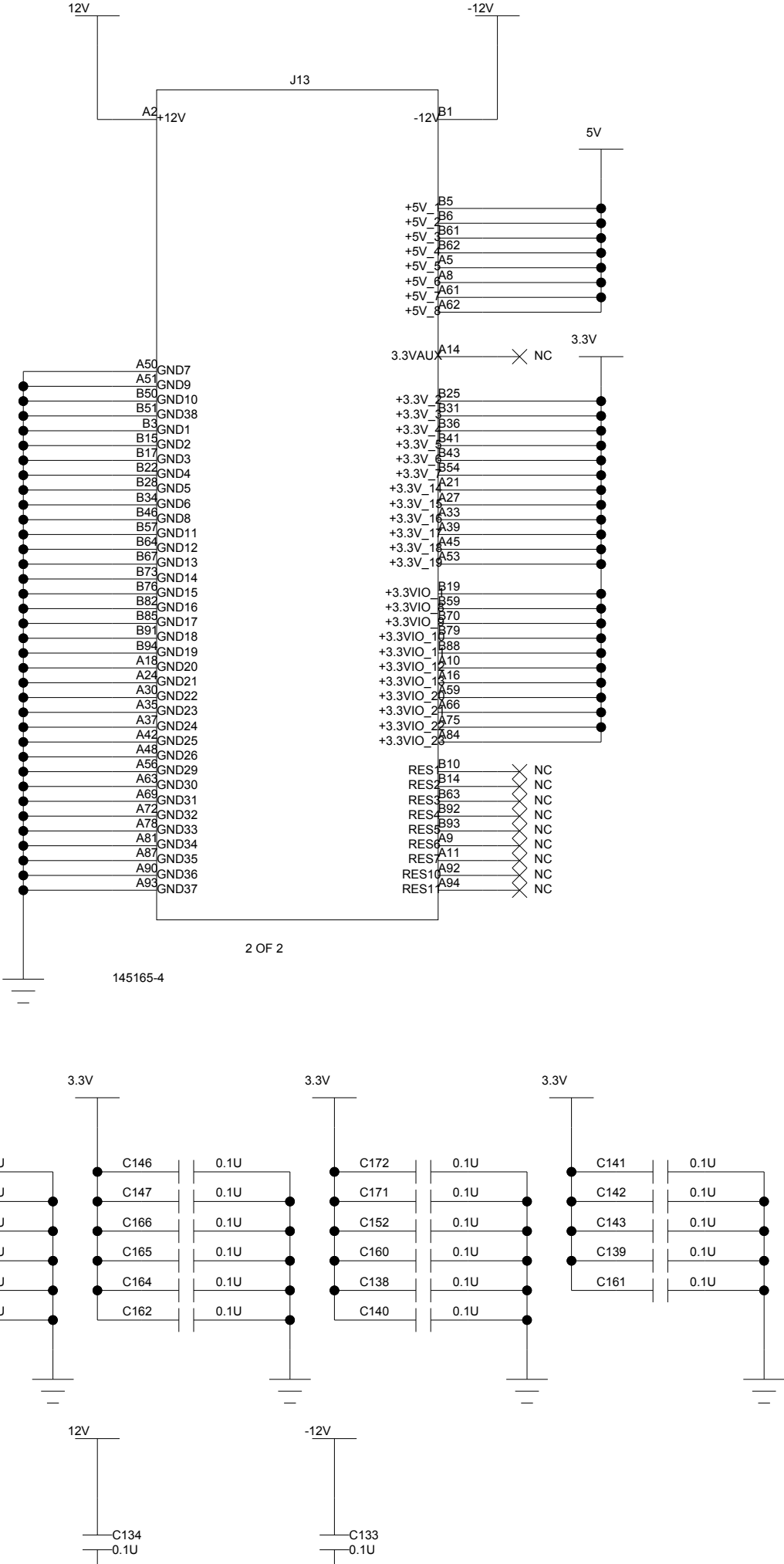
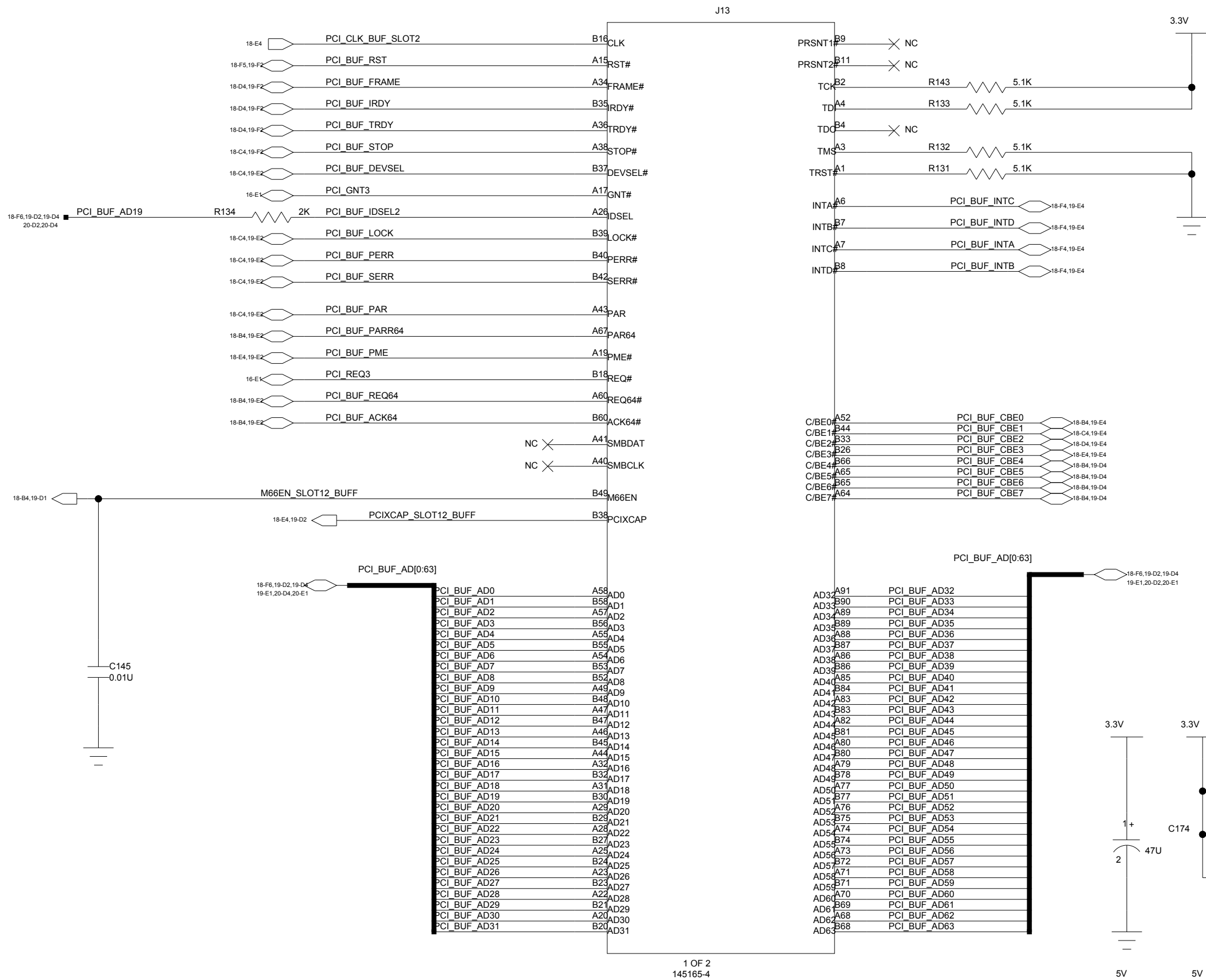
C

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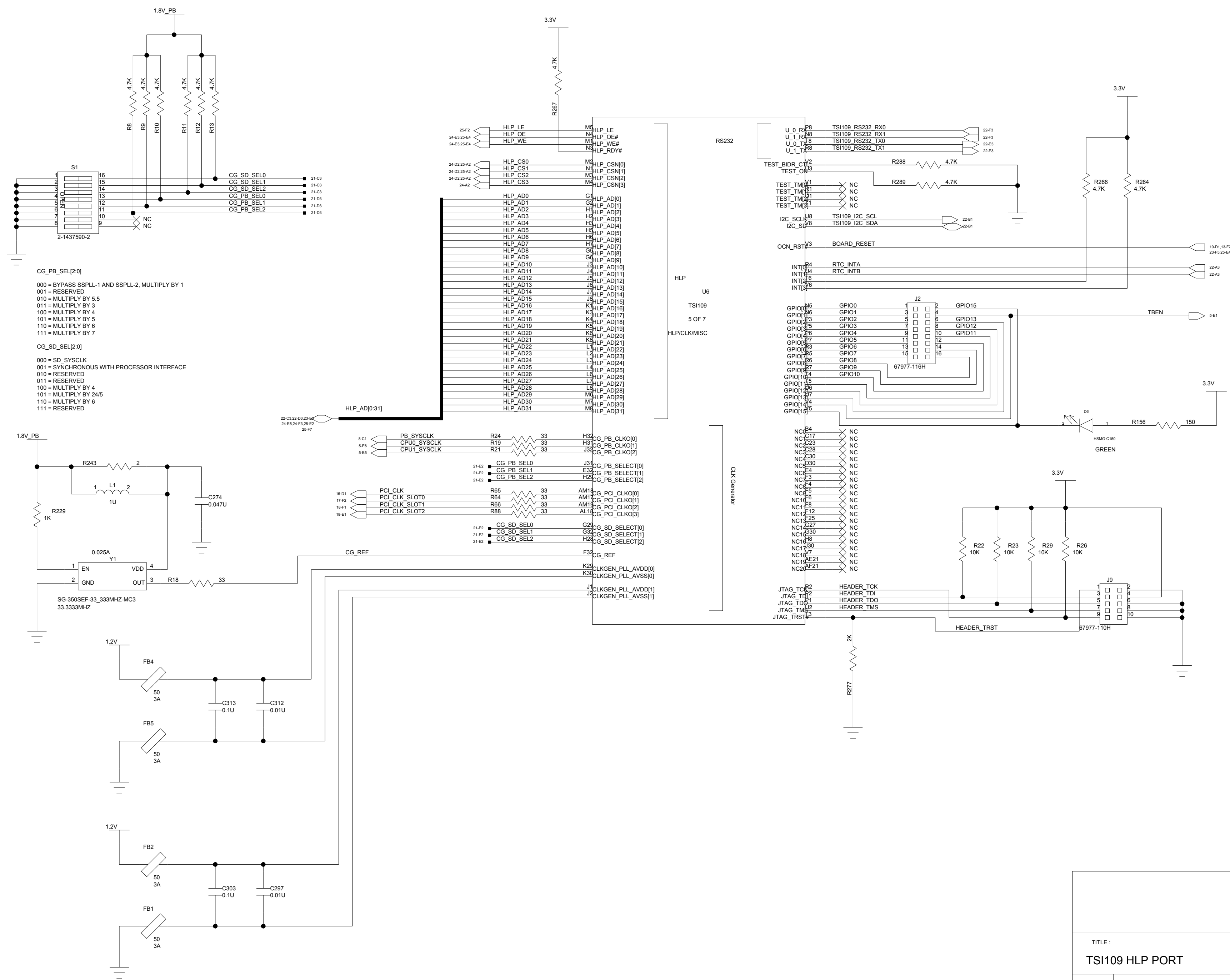
PCI SLOT 2

Note: IDSEL resistor should be 100 Ohms for PCI and 2K for PCIX



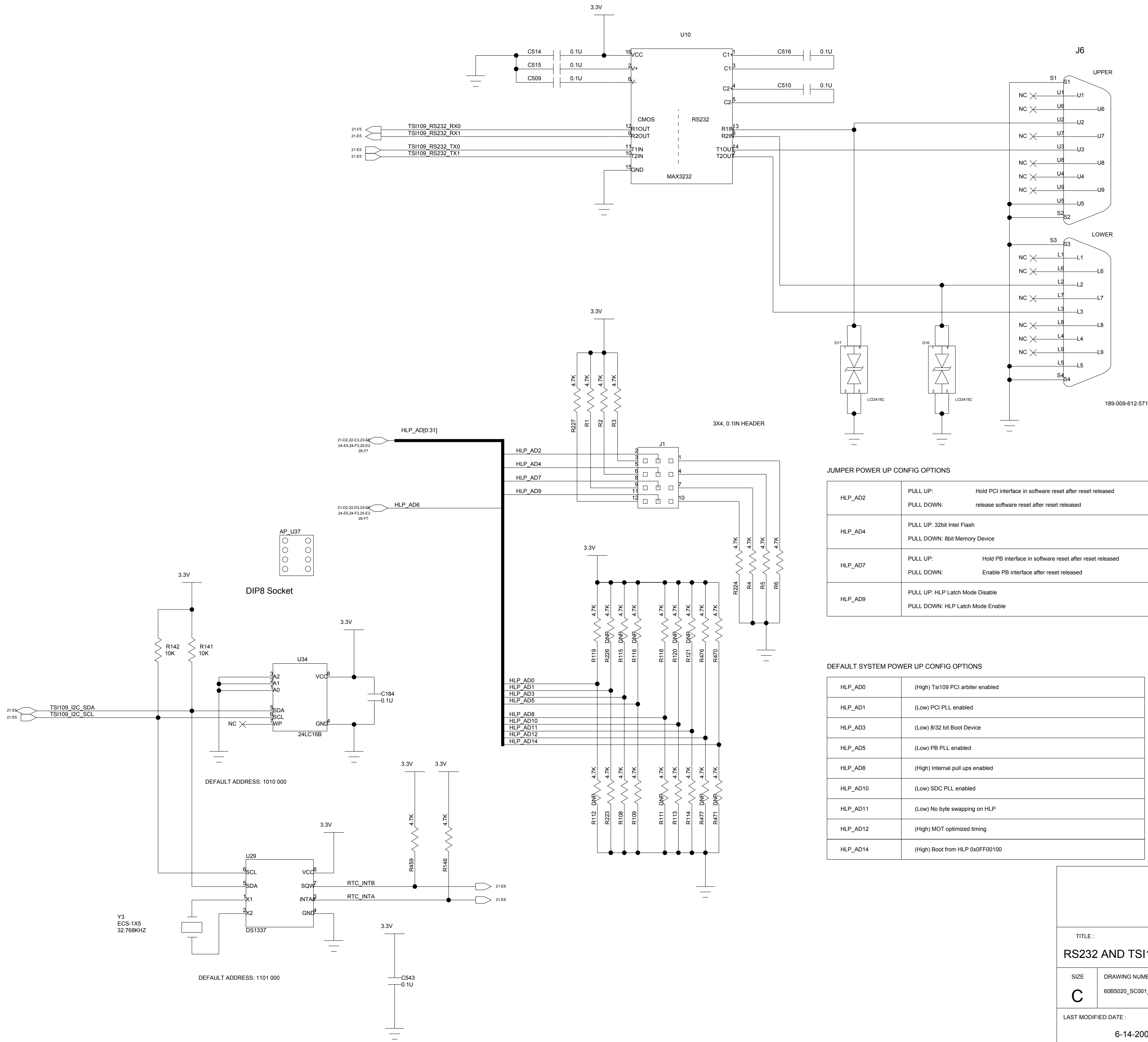
TITLE : PCI SLOT 2			
SIZE C	DRAWING NUMBER : 60B5020_SC001_0	Version: 2	DESIGNER : SYSENG HARDWARE
LAST MODIFIED DATE : 6-14-2007_16:56		SHEET 20 OF 30	

TSI109 HOST LOCAL PORT



TITLE :			
TSI109 HLP PORT			
SIZE C	DRAWING NUMBER : 60B5020_SC001_0	Version: 2	DESIGNER : SYSENG HARDWARE
LAST MODIFIED DATE : 6-14-2007_16:56		SHEET 21 OF 30	

RS232 AND POWER-UP CONFIGURATION



JUMPER POWER UP CONFIG OPTIONS

HLP_AD2	PULL UP: Hold PCI interface in software reset after reset released PULL DOWN: release software reset after reset released
HLP_AD4	PULL UP: 32bit Intel Flash PULL DOWN: 8bit Memory Device
HLP_AD7	PULL UP: Hold PB interface in software reset after reset released PULL DOWN: Enable PB interface after reset released
HLP_AD9	PULL UP: HLP Latch Mode Disable PULL DOWN: HLP Latch Mode Enable

DEFAULT SYSTEM POWER UP CONFIG OPTIONS

HLP_AD0	(High) Tsi109 PCI arbiter enabled
HLP_AD1	(Low) PCI PLL enabled
HLP_AD3	(Low) 8/32 bit Boot Device
HLP_AD5	(Low) PB PLL enabled
HLP_AD8	(High) Internal pull ups enabled
HLP_AD10	(Low) SDC PLL enabled
HLP_AD11	(Low) No byte swapping on HLP
HLP_AD12	(High) MOT optimized timing
HLP_AD14	(High) Boot from HLP 0x0FF00100

TITLE : RS232 AND TSI109 CONFIG			
SIZE C	DRAWING NUMBER : 60B5020_SC001_0	Version: 2	DESIGNER : SYSENG HARDWARE
LAST MODIFIED DATE : 6-14-2007_16:56		SHEET 22 OF 30	

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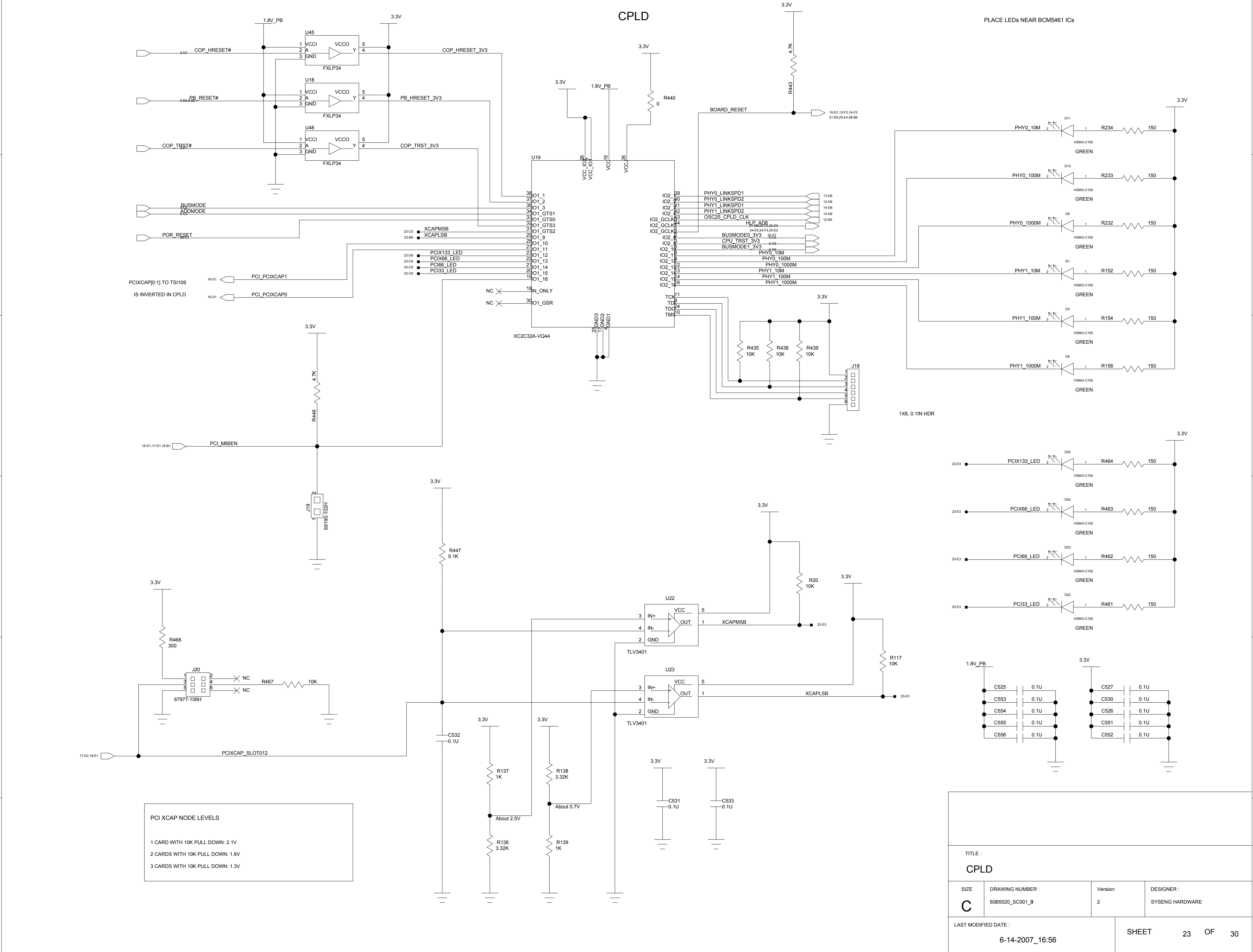
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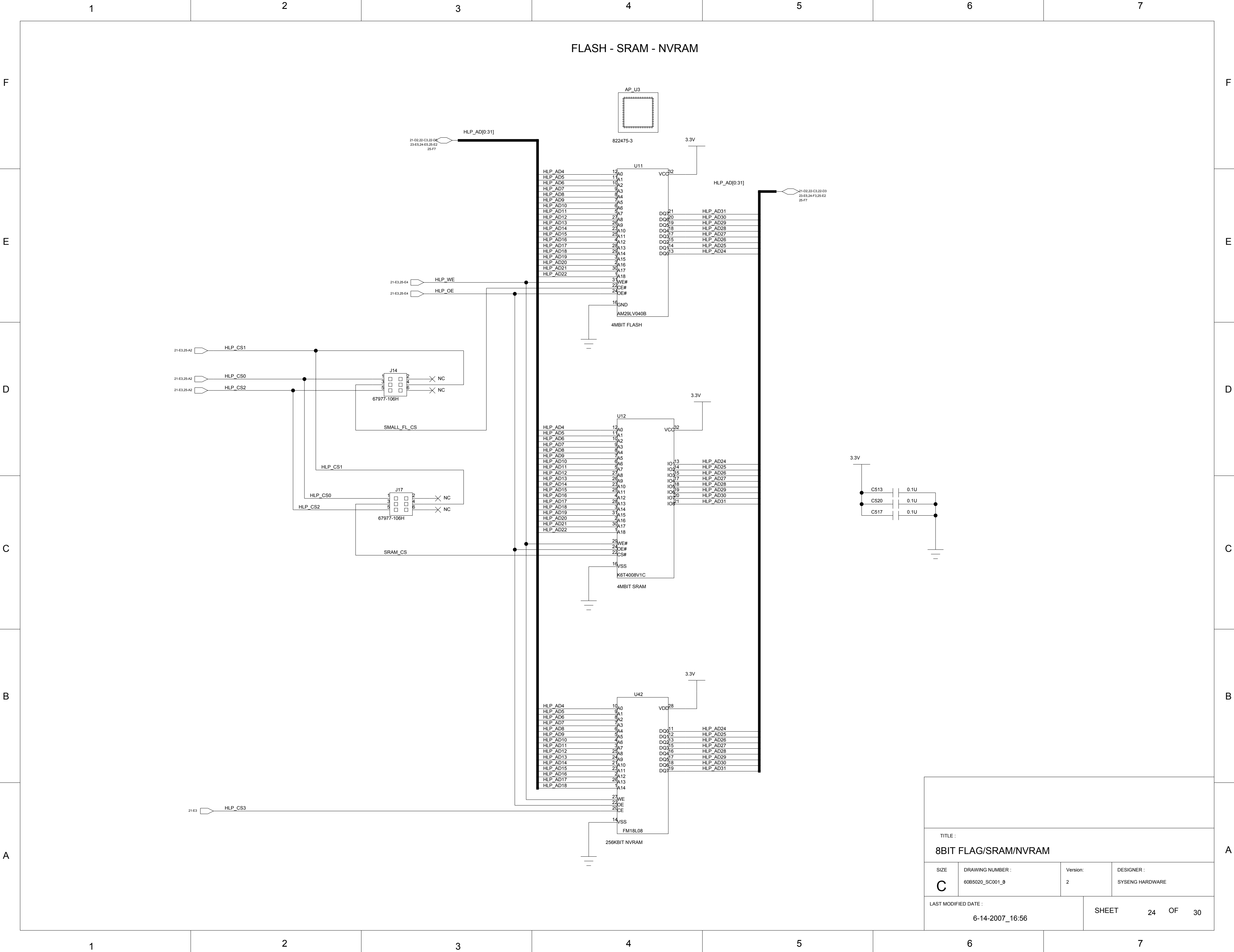
A



PCI XCAP NODE LEVELS

1 CARD WITH 10K PULL DOWN: 2.1V  
2 CARDS WITH 10K PULL DOWN: 1.6V  
3 CARDS WITH 10K PULL DOWN: 1.3V

TITLE : CPLD			
SIZE C	DRAWING NUMBER : 60B5020_SC001_0	Version: 2	DESIGNER : SYSENG HARDWARE
LAST MODIFIED DATE : 6-14-2007_16:56		SHEET 23 OF 30	



TITLE :			
8BIT FLAG/SRAM/NVRAM			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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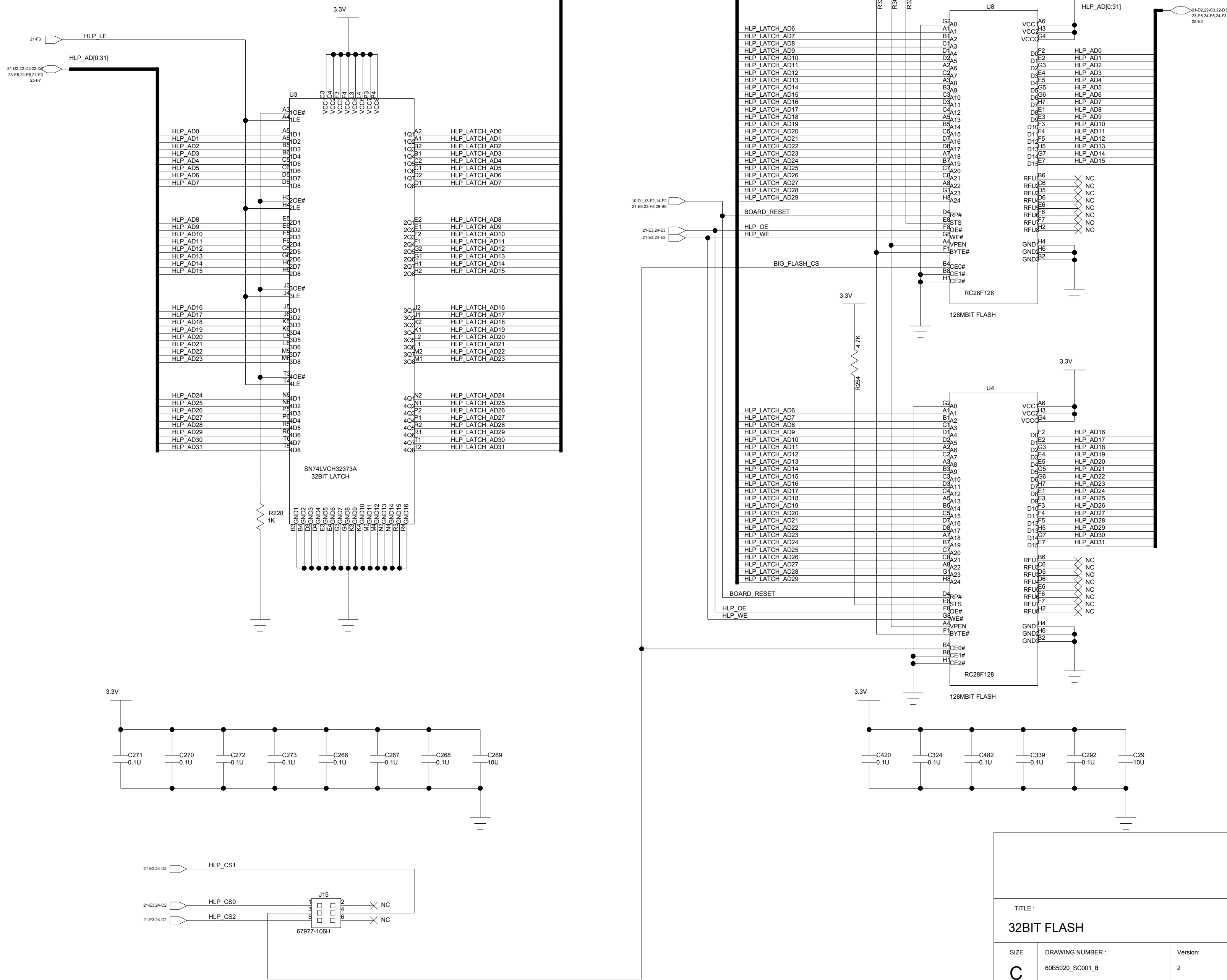
D

C

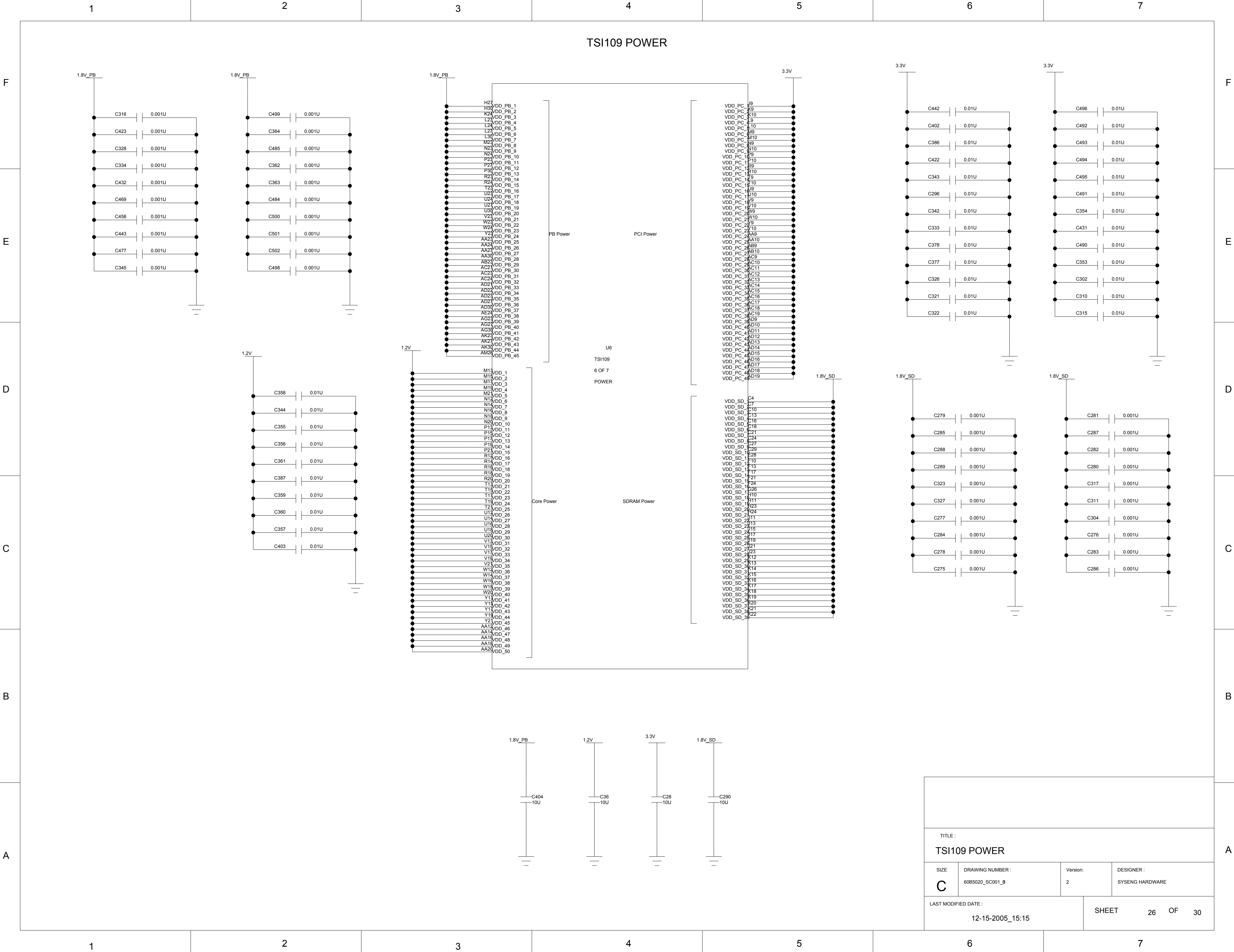
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LATCH AND FLASH



TITLE :			
32BIT FLASH			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60B5020_SC001_0	2	SYSENG HARDWARE
LAST MODIFIED DATE :		SHEET 25 OF 30	
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3.3V

C442

0.01U

C402

0.01U

C386

0.01U

C422

0.01U

C343

0.01U

C296

0.01U

C342

0.01U

C333

0.01U

C378

0.01U

C377

0.01U

C326

0.01U

C321

0.01U

C322

0.01U

3.3V

C496

0.01U

C492

0.01U

C493

0.01U

C494

0.01U

C495

0.01U

C491

0.01U

C354

0.01U

C431

0.01U

C490

0.01U

C353

0.01U

C302

0.01U

C310

0.01U

C315

0.01U

1.8V\_PB

C404

10U

1.2V

C36

10U

3.3V

C28

10U

1.8V\_SD

C290

10U

TSI109 POWER

U6

TSI109

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POWER

PB Power

PCI Power

Core Power

SDRAM Power

1.8V\_PB

1.2V

3.3V

1.8V\_SD

TITLE :

TSI109 POWER

SIZE

DRAWING NUMBER :

Version:

DESIGNER :

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60B5020\_SC001\_0

2

SYSENG HARDWARE

LAST MODIFIED DATE :

12-15-2005\_15:15

SHEET

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30

TSI109 GROUND

[illegible]

TITLE :

TSI109 GROUND

SIZE

DRAWING NUMBER :

Version:

DESIGNER :

C

60B5020\_SC001\_0

2

SYSENG HARDWARE

LAST MODIFIED DATE :

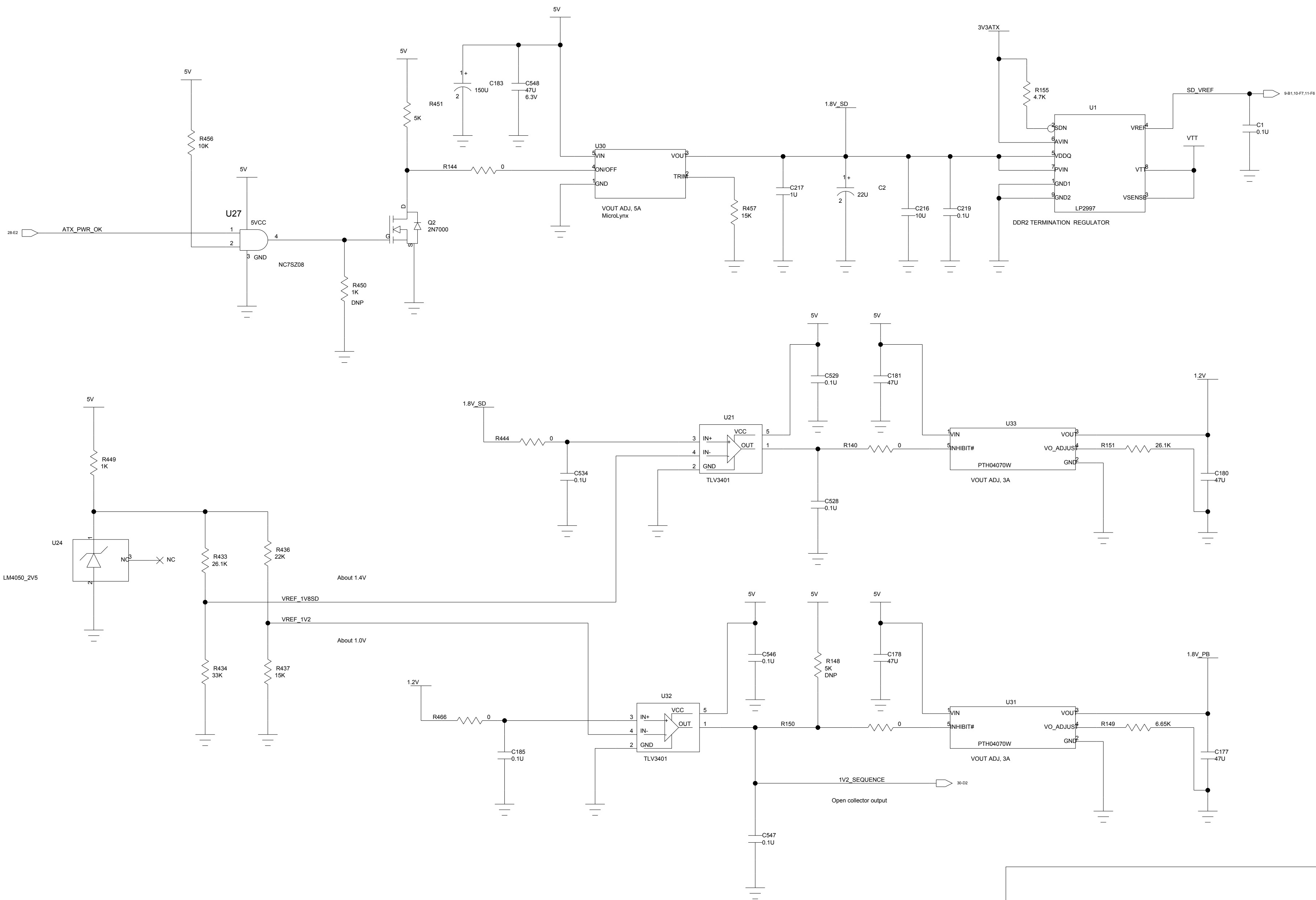
12-15-2005\_15:15

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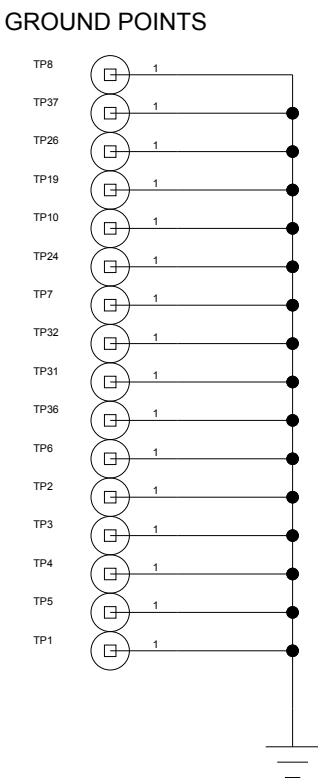
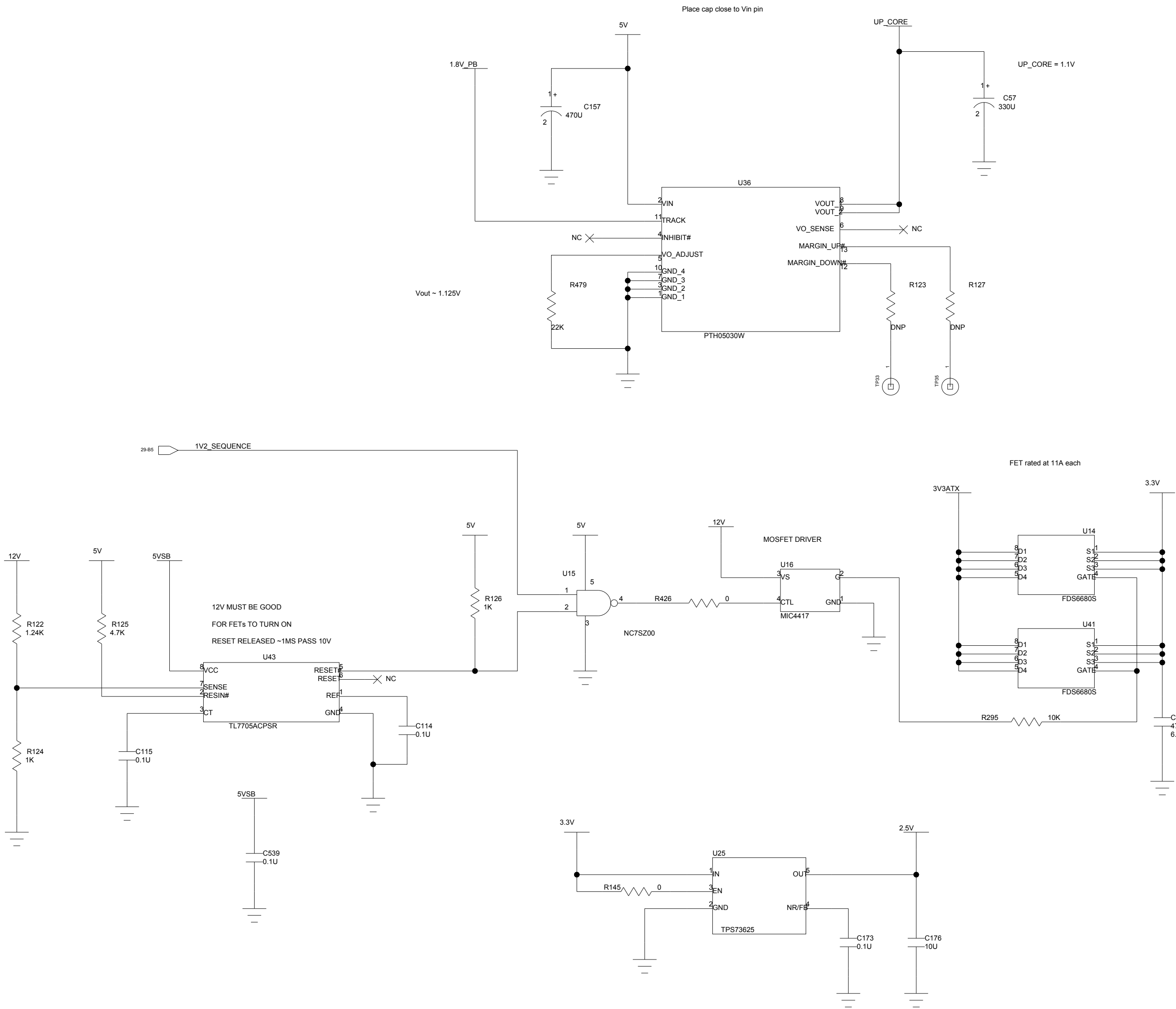
POWER SUPPLY - REGULATORS AND SEQUENCING

Place these caps close to Vin pins



TITLE :			
POWER REGULATORS 1			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60B5020_SC001_0	2	SYSENG HARDWARE
LAST MODIFIED DATE :			SHEET
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POWER SUPPLY - REGULATORS



TITLE :			
POWER REGULATORS 2			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60B5020_SC001_0	2	SYSENG HARDWARE
LAST MODIFIED DATE :		SHEET 30 OF 30	
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