



# Implementing an Arbiter Extension CPLD for Tsi381™/Tsi382™ Based Systems

602000\_AN001\_02

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6024 Silver Creek Valley Road San Jose, California 95138

Telephone: (408) 284-8200 • FAX: (408) 284-3572

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# 1. Implementing an Arbiter Extension CPLD for Tsi381/Tsi382 Based Systems

This application note describes the implementation of an arbiter extension in a system where Tsi381 is used in a system with more than four PCI devices. The proposed solution implements an arbiter extension in a low cost CPLD.

## Revision History

### **60E2000\_AN004\_02, Formal, September 2009**

This document was rebranded as IDT.

### **60E2000\_AN004\_01, Formal, June 2008**

This is the first release of the document.

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## 1.1 Overview

The arbiter extension CPLD is a simple arbiter signal multiplexer. It takes request signals from two PCI masters and multiplexes them onto one Tsi381 request line. In the opposite direction, it takes one grant output from the Tsi381 and assigns it to the PCI master that issued the request. In the event two PCI masters request the bus at the same time, the multiplexer alternates evenly between the two masters.

This arbiter extension solution is applicable to Tsi381 and Tsi382 based systems.

## 1.2 Implementation

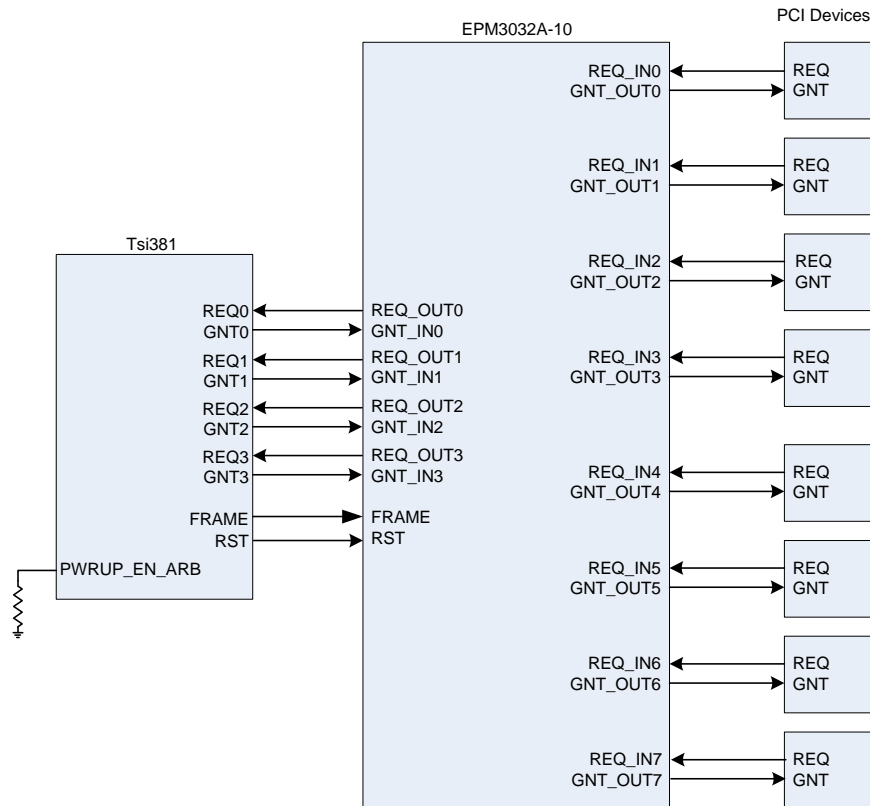
The 8-master arbiter extender provided by IDT is targeted for Altera's EPM3032ATC44-10 CPLD.

Connect all four Tsi381 request and all four Tsi381 grants to the CPLD.

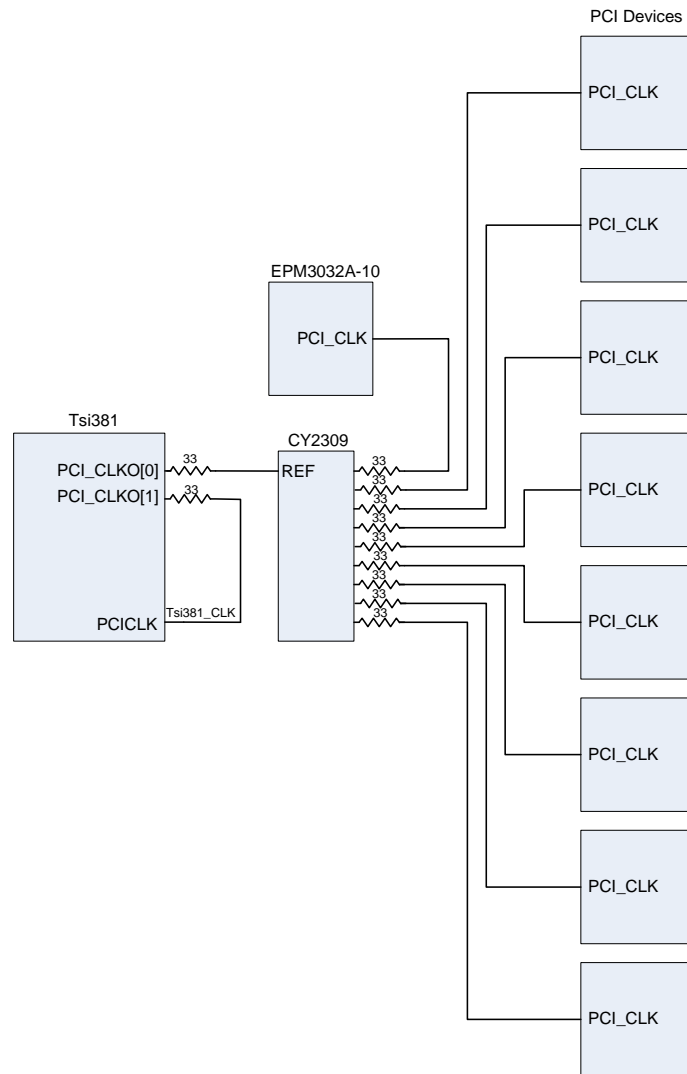
Connect all eight PCI master device's requests and grants to the CPLD.

Provide a copy of the PCI bus clock.

PCI\_FRAME and PCI\_RESET are also required.

**Figure 1: Arbiter Extension CPLD**

The PCI clock must be distributed to all PCI devices, including the CPLD and Tsi381. One of the Tsi381 PCI clock outputs must be distributed with a fanout buffer such as the Cypress' CY2309 to each PCI device, including the CPLD. Use the other PCI clock output of the Tsi381 to loopback the PCI clock its PCI\_CLK input (see [Figure 2](#)).

**Figure 2: PCI Bus Clocking**

## 1.3 CPLD Signal List

The following table provides a signal name list and a connection description. Please contact IDT for a copy of the source code, the pin assignment, and the CPLD programmer object file (.POF)

**Table 1: CPLD Pin List**

CPLD Signal	Direction	Description
clk	input	Connect this input to the PCI bus clock distribution buffer
pci_frame_i	input	Connect this input to PCI_FRAMEn of Tsi381
pci_gnt_i[0]	input	Connect to Tsi381 PCI_GNTn[0] output
pci_gnt_i[1]	input	Connect to Tsi381 PCI_GNTn[1] output
pci_gnt_i[2]	input	Connect to Tsi381 PCI_GNTn[2] output
pci_gnt_i[3]	input	Connect to Tsi381 PCI_GNTn[3] output
pci_req_i[0]	input	Connect PCI device 0 REQ output
pci_req_i[1]	input	Connect PCI device 1 REQ output
pci_req_i[2]	input	Connect PCI device 2 REQ output
pci_req_i[3]	input	Connect PCI device 3 REQ output
pci_req_i[4]	input	Connect PCI device 4 REQ output
pci_req_i[5]	input	Connect PCI device 5 REQ output
pci_req_i[6]	input	Connect PCI device 6 REQ output
pci_req_i[7]	input	Connect PCI device 7 REQ output
rst_n	input	Connect to Tsi381 PCI_RSTn output
pci_gnt_o[0]	output	Connect PCI device 0 GNT input
pci_gnt_o[1]	output	Connect PCI device 1 GNT input
pci_gnt_o[2]	output	Connect PCI device 2 GNT input
pci_gnt_o[3]	output	Connect PCI device 3 GNT input
pci_gnt_o[4]	output	Connect PCI device 4 GNT input
pci_gnt_o[5]	output	Connect PCI device 5 GNT input
pci_gnt_o[6]	output	Connect PCI device 6 GNT input
pci_gnt_o[7]	output	Connect PCI device 7 GNT input
pci_req_o[0]	output	Connect to Tsi381 PCI_REQn[0] input
pci_req_o[1]	output	Connect to Tsi381 PCI_REQn[1] input
pci_req_o[2]	output	Connect to Tsi381 PCI_REQn[2] input
pci_req_o[3]	output	Connect to Tsi381 PCI_REQn[3] input

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## 1.4 Tsi381 Setup

### *PWRUP\_ARB\_EN*

When the arbiter extension CPLD is used, the Tsi381's internal arbiter must be ENABLED. To enable the Tsi381 arbiter, set the PWRUP\_EN\_ARB pin to ground.



**CORPORATE HEADQUARTERS**  
6024 Silver Creek Valley Road  
San Jose, CA 95138

**for SALES:**  
800-345-7015 or 408-284-8200  
fax: 408-284-2775  
[www.idt.com](http://www.idt.com)

**for Tech Support:**  
email: [ssdhelp@idt.com](mailto:ssdhelp@idt.com)  
phone: 408-284-8208  
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