Product Change Notice (PCN)

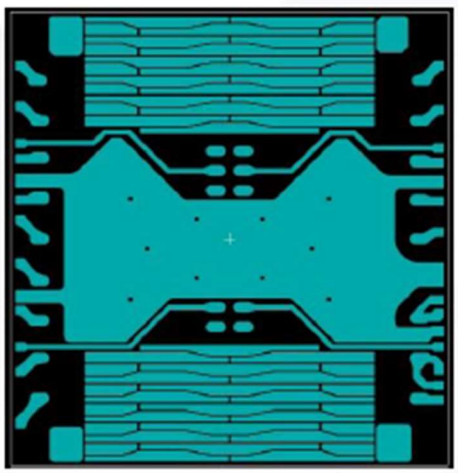
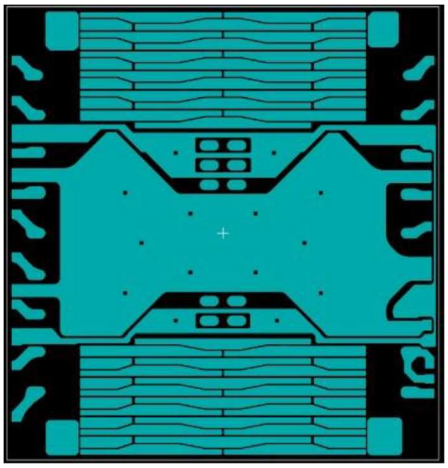
Subject: Metal Spin and Change in RDL Design and PI Materials
Publication Date: 6/16/2023
Effective Date: 9/15/2023

Revision Description:
Initial Release

Description of Change:
Renesas has made a metal spin to fix the ADC stuck and I2C issue. In addition, there are modifications made on the RDL layout and PI materials.

The ordering part number will change.

Refer below table for comparison.

	Current	New
Ordering Part#	P8900-X0Z001FNG P8900-X0Z001FNG8	P8900-X1Z001FNG P8900-X1Z001FNG8
RDL Design		
PI1 & PI2 Material	High temp cure material, HD4100	Low temp cure material, LTC9320

Affected Product List: P8900-X0Z001FNG, P8900-X0Z001FNG8

Reason for Change:
The change is to address the improvements made to ADC stuck and I2C issue.

Impact on Fit, Form, Function, Quality & Reliability:
The change will have no impact on the form, fit, function, quality, reliability and environmental compliance of the products.

Product Identification:
New ordering part number, P8900-X1Z001FNG, P8900-X1Z001FNG8

Qualification Status: Completed. Refer Appendix A
Sample Availability Date: 4 weeks from sample booking date
Device Material Declaration: Available upon request

Note:

1. Acknowledgement must be received by Renesas within 30 days or Renesas will consider the change as approved.

2. If timely acknowledgement is provided by Customer, then Customer shall have 90 days from the date of receipt of this PCN to make any objections to this PCN. If Customer fails to make objections to this PCN within 90 days of the receipt of the PCN then Renesas will consider the PCN changes as approved.

3. If customer cannot accept the PCN then customer must provide Renesas with a last time buy demand and purchase order.

For additional information regarding this notice, please contact idt-pcn@lm.renesas.com

Product Qualification Report

Date: 4/03/2023

Product: P8900-X1 (Highly integrated, highly efficient PMIC for DDR5 Applications)	
Base Product: AW842T006	Process Technology: CV018G BCD gen3, 1P5M
Package Type: FCQFN 5 x 5 mm (36L)	Fab location: TSMC, Taiwan
Qual Plan: Q19-07-001/ Q23-01-004/Q23-01-007/ P23-02-004/P19-03-005	Assembly location: Greatek, Taiwan

Test Description	**Conditions**	**Sample Size**	**Results (rej/SS)**	**Comments**
High Temperature Operating Life	JESD22-A108, Tj=125°C, Vccmax, 1000 hrs	77	0/77, x 3 lots	Pass
ESD: Human Body Model	JS-001 Classification	3	0/3	Pass, Class 1C (2000V)
ESD: Charged Device Model	JS-002 Classification	3	0/3	Pass, Class 1C (750V)
Latch-Up	JESD78, +/-100mA	6	0/6	Pass, Ta = 85°C
Electrical Characterization	Datasheet	10	Results reported in Datasheet	Completed
NVCE	JESD22-A117, 230415, 10K cycles.	78	0/78	Pass, Ta = 85°C
PCHTDR	JESD22-A117, 230415, 72 hours.	78	0/78	Pass, Ta = 250°C
EOS	Per Datasheet, VIN_Mgmt=10V, VIN_Bulk=37V	3	0/3	Pass
Unbiased Temperature Humidity (UHAST)[1]	JESD22-A118, +130°C/85% R.H., Unbiased, 96 hrs	77	0/77, x3 lots	Pass
Highly Accelerated Temperature and Humidity stress (BHAST) [1]	JESD22-A110, +130°C, 85% R.H., Vcc_{max},96 hrs	77	0/77, x 3 lots	Pass
Temperature Cycling [1]	JESD22-A104, -55°C to +125°C, 700 cycles	77	0/77, x3 lots	Pass
High Temperature Storage Life (HTSL)	JESD22-A103, +150°C, 1000 hrs	45	0/45, x 3 lots	Pass
Solderability Test	J-STD-002	5	0/5, x3 lots	Pass
Moisture Classification	J-STD-020	25	0/25, x2 lots	Pass MSL1 / 260°C

Note:

1. With preconditioning per JESD22-A113, MSL 1 (260°C).