

## Product Change Notice (PCN)

**Subject:** 28Gbps VCSEL Driver and TIA+PA Receiver Revision Update

**Publication Date:** 2/9/2026

**Effective Date:** 5/20/2026

**Revision Description:**

Initial Release

**Description of Change:**

HXT8204-DNG and HXT8212-DNG: Fixed the issues reported the errata in PA210013 (R1) of the previous version as below.

- LDIS is not functional in Analog modes.
- GDPD, all DPDx, uLDIS, and LDIS must always be set to zero.
- AUTOLDIS must always be set to zero.
- BAx must always be set to  $\geq 3$ .

HXR8204 and HXR8212: Added alignment marker on the one corner of die.

**Affected Product List:**

HXT8204-DNG	HXR8204-DNG	HXT8212-DNG	HXR8212-DNG
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**Note:** Product Advisory PA210013 (R1) issued on 7/31/2021 is no longer applicable to HXT8204-DNG and HXT8212-DNG, but still valid to HXT8212-DNT.

**Reason for Change:**

To fix the functional restriction mentioned in the errata for HXT8204-DNG and HXT8212-DNG.

To improve the easy of assembly in regards of die orientation for HXR8204-DNG and HXR8212-DNG.

**Impact on Fit, Form, Function, Quality & Reliability:**

The change will have no impact on Fit, quality, reliability and compliance of products except for function and adding alignment mark described in the section of Description of Change.

Please see Appendix A regarding reliability.

**Product Identification:**

Updated the device revision in the Revision Identifier Register (0xE1) from 6 (decimal) to 7 (decimal).

Please see Appendix B regarding physical die ID.

**Qualification Status:** Completed

**Sample Availability Date:** 12/19/2025

**Device Material Declaration:** Available upon request. No change compared to the previous version.

## Note:

1. Acknowledgement must be received by Renesas within 30 days or Renesas will consider the change as approved.
2. If timely acknowledgement is provided by Customer, then Customer shall have 90 days from the date of receipt of this PCN to make any objections to this PCN. If Customer fails to make objections to this PCN within 90 days of the receipt of the PCN then Renesas will consider the PCN changes as approved.
3. If customer cannot accept the PCN then customer must provide Renesas with a last time buy demand and purchase order.

For additional information regarding this notice, please contact [idt-pcn@lm.renesas.com](mailto:idt-pcn@lm.renesas.com)

**Appendix A - Qualification Results**

1.

Product Type: HXT8204-DNG rev E				
Qual Plan		Q25-01-001		
Process Technology: 1P6M/8HP		Fab Location: GFUSA-GF 9		
Test Description	Conditions	Sample Size	Results (rej/SS)	Comments
HIGH TEMPERATURE OPERATING LIFE (HTOL)	JESD22-A108, JESD85 Tj=125°C, 1000 hrs, Vcc=3.63V, VCONF=3.3V Static bias, 100% duty Cycle	77	0/77 1 lot	Passed
LATCH-UP (LU)	JESD78 +/-100mA I/O and 1.5x Vcc OV stress, Class II (Tj=105°C)	6	0/6 1 lot	Passed
ESD: HBM	JS-001 (TA = 25°C)	3	0/3 1 lot	Pass (Note 1)
ELECTRICAL CHARACTERIZATION	JESD86 (TA per Datasheet Conditions)	27	Reported in the datasheet	Completed

**Note 1:**

Pins	ESD Test Point	REJ/SS
RF input / output pins	250V	0/3
DC pins	2000V	0/3

2.

Product Type: HXT8212-DNG rev E				
Qual Plan		Q25-01-001		
Process Technology: 1P6M/8HP		Fab Location: GFUSA-GF 9		
Test Description	Conditions	Sample Size	Results (rej/SS)	Comments
HIGH TEMPERATURE OPERATING LIFE (HTOL)	JESD22-A108, Tj=125°C, 1000 hrs, Vcc=3.63V, VCONF=3.3V Static bias, 100% duty Cycle	77	0/77 1 lot	QBS to HXT8204-DNG rev E qual
LATCH-UP (LU)	JESD78 +/-100mA I/O and 1.5x Vcc OV stress, Class II (Tj=105°C)	6	0/6 1 lot	Pass
ESD: HBM	JS-001 (TA = 25°C)	3	0/3 1 lot	Pass (Note 1)
ELECTRICAL CHARACTERIZATION	JESD86 (TA per Datasheet Conditions)	27	Reported in the datasheet	Completed

**Note 1:**

Pins	ESD Test Point	REJ/SS
RF input / output pins	250V	0/3
DC pins	1000V	0/3

3.

<b>Product Type: HXR8204-DNG rev E</b>				
<b>Qual Plan</b>	Q25-01-001			
<b>Process Technology: 1P6M/8HP</b>			<b>Fab Location: GFUSA-GF 9</b>	
<b>Test Description</b>	<b>Conditions</b>	<b>Sample Size</b>	<b>Results (rej/SS)</b>	<b>Comments</b>
HIGH TEMPERATURE OPERATING LIFE (HTOL)	JESD22-A108, Tj=125°C, 1000 hrs, Vcc=3.63V, Static bias, 100% duty Cycle	77	0/77 1 lot	QBS to HXR8204 rev D qual (Q20-04-012)
LATCH-UP (LU)	JESD78 +/-100mA I/O and 1.5x Vcc OV stress, Class II (Tj=105 °C)	6	0/6 1 lot	Passed
ESD: HBM	JS-001 (TA = 25 °C)	3	0/3 1 lot	Pass (Note 1)
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4.

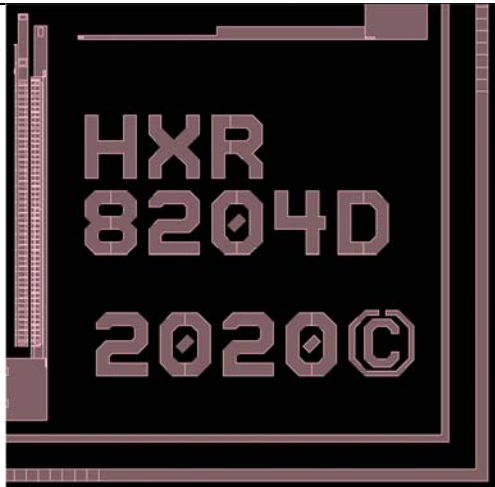



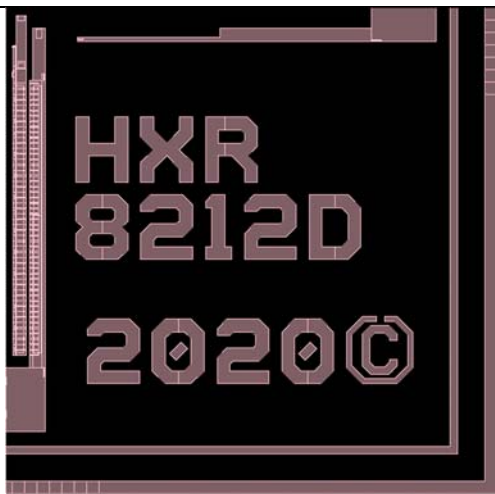

<b>Product Type: HXR8212-DNG rev E</b>				
<b>Qual Plan</b>	Q25-01-001			
<b>Process Technology: 1P6M/8HP</b>			<b>Fab Location: GFUSA-GF 9</b>	
<b>Test Description</b>	<b>Conditions</b>	<b>Sample Size</b>	<b>Results (rej/SS)</b>	<b>Comments</b>
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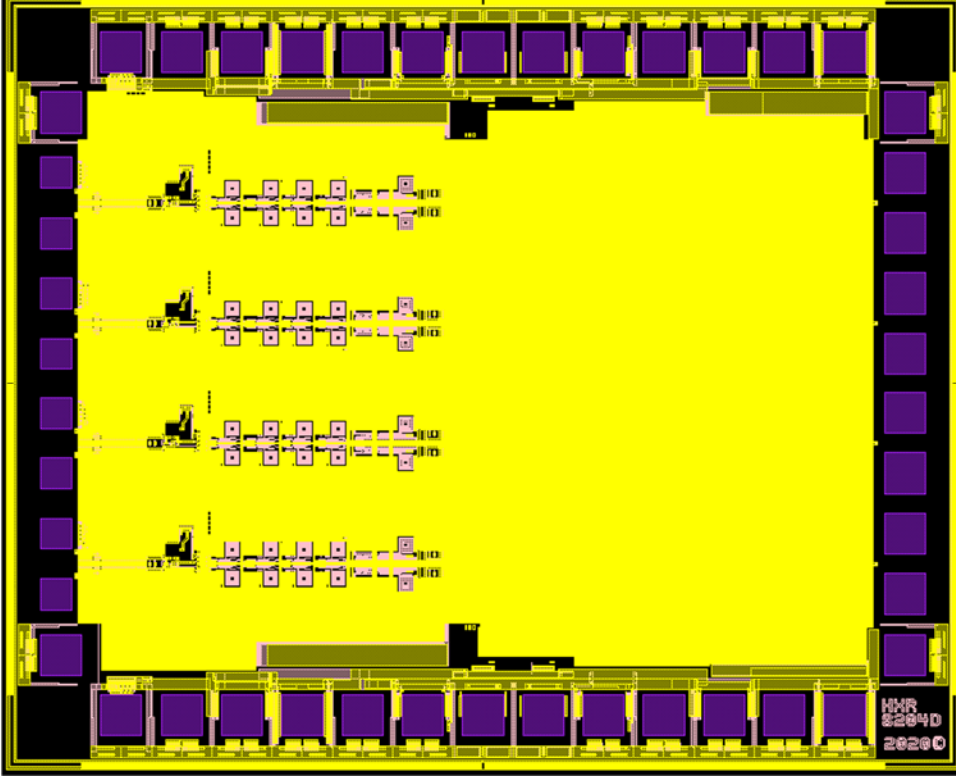
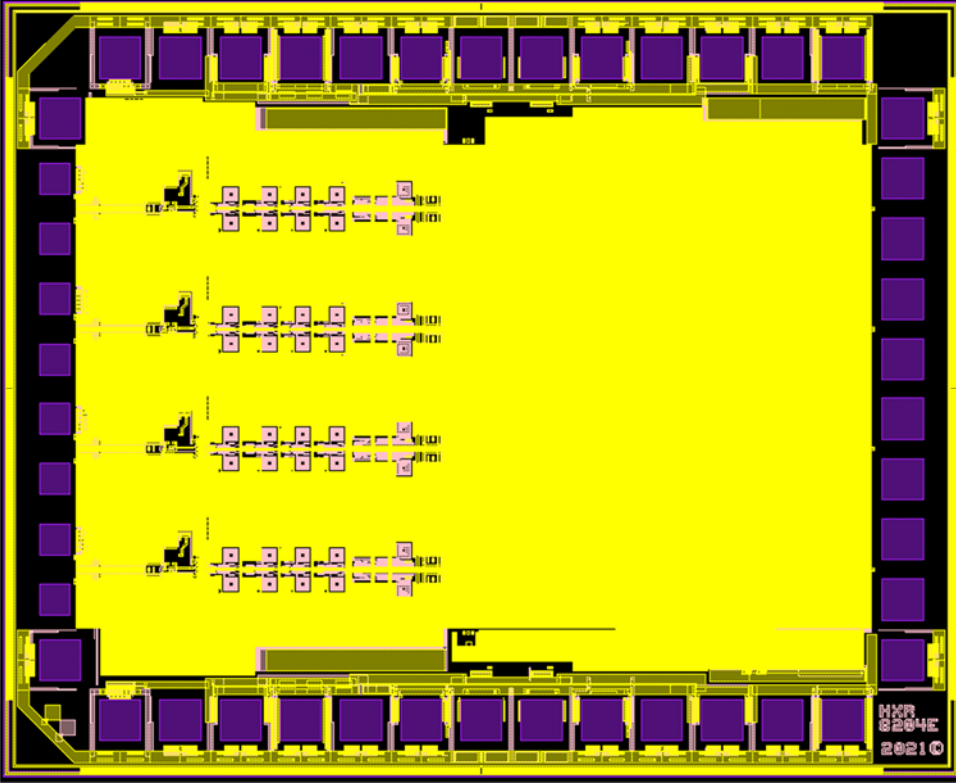
Appendix B – Physical Die ID Label and Alignment Maker Comparison

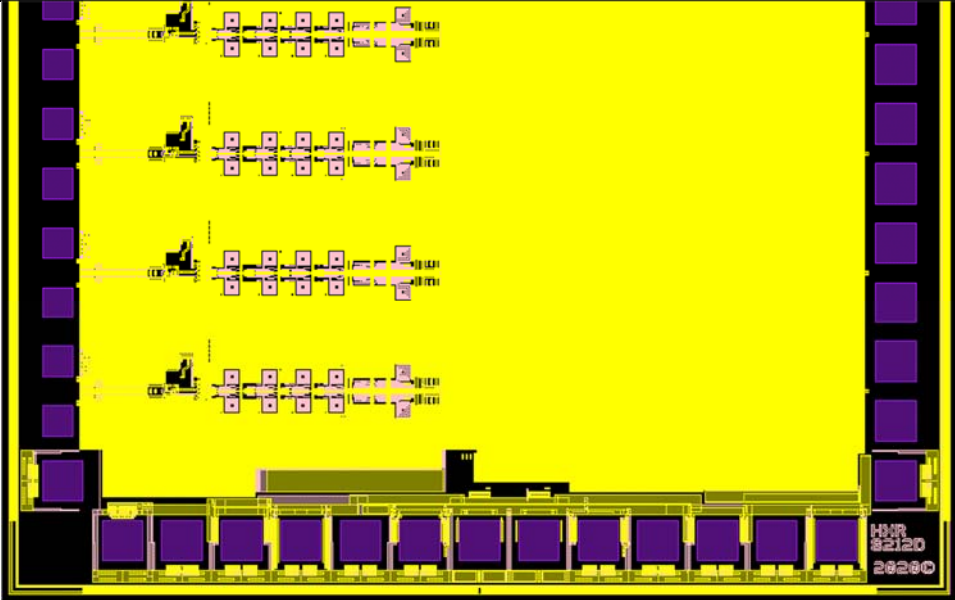

Die ID Label Comparison

	Previous Version (Revision D)	Updated Version (Revision E)
HXR8204-DNG		
HXT8204-DNG		
HXR8212-DNG		



Alignment Maker Comparison

<p>HXR8204D</p>	
<p>HXR8204E</p> <p>Alignment maker in lower left corner</p>	

<p><b>HXR8212D</b></p>	 <p>A top-down micrograph of the HXR8212D chip. The chip is rectangular with a yellow central area and purple peripheral areas. It features a grid of small square components and larger rectangular structures. A label in the bottom right corner reads "HXR 8212D 2020".</p>
<p><b>HXR8212E</b> <b>Alignment maker in lower left corner</b></p>	 <p>A top-down micrograph of the HXR8212E chip, which is similar in layout to the HXR8212D. It features a yellow central area and purple peripheral areas. A small square feature, identified as an alignment maker, is located in the lower left corner. A label in the bottom right corner reads "HXR 8212E 2021".</p>