Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **F-0602-01R1** DATE: **6/27/06**
Product Affected: **IDT72125 Family**

Date Effective: **9/19/06**

MEANS OF DISTINGUISHING CHANGED DEVICES:
- ☐ Product Mark
- ☐ Back Mark
- ■ Date Code Top mark will show "Y4" die revision.
- ☐ Other

Contact: Dennis Lantz
Title: Quality Engineer
Phone #: (408) 284-4597
Fax #: (408) 284-1450
E-mail: Dennis.Lantz@idt.com

Attachment: ■ Yes ☐ No

Samples: Available upon request

DESCRIPTION AND PURPOSE OF CHANGE:
- ☐ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ■ Manufacturing Site
- ☐ Data Sheet
- ☐ Other

This notification is to amend minimum gate length that was inadvertently written as 0.6 m in PCN# F-0602-01, published in 21-Jun-2006.

The correct minimum gate length is 0.6 um.

There is no change in the PCN affectivity date.

RELIABILITY/QUALIFICATION SUMMARY:

Refer to the attached qualification summary.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone # /Fax #: _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

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ATTACHMENT I - PCN #: F-0602-01R1

PCN Type: Fab site change.

Data Sheet Change: None

Detail of Change: Transfer existing qualified products from Salinas, California IDT wafer fab facility (Fab 2) to Hillsboro, Oregon IDT wafer fab facility (Fab 4).

Product	72125Y	72125Y4
Die Revision	Y	Y4
Wafer Fab	Fab 2	Fab 4
Fab Technology	CMOS 8	CMOS 8
# Poly Layers	2	2
# Metal Layers	2	2
Minimum Gate Length	0.6 um	0.6 um
Die Dimensions (k sq. mils)	5.3	5.3

Sample Availability: Now. Contact sales to request samples.

Production Shipments: September 19, 2006

Production Information:

Part Number	Current Die Rev	New Die Rev
IDT72125L25SO	Y	Y4
IDT72125L50SO	Y	Y4
IDT72125L25TP	Y	Y4
IDT72125L50TP	Y	Y4
IDT72125L25SOG	Y	Y4

Notes: For T & R (shipping method) "8" is added to the orderable part number

Qualification Plan #: QSM-0601-01

Qualification Results

Test Description	Test Method (Latest specs in effect)	Sample Size	Test Results SS / Rej
High Temperature Operating Lifetest (Dynamic) (125 °C, 500 hours)	JESD22-A108	3 lots / 116 units each lot	348/0
ESD: Human Body Model	MIL-STD 883 Method 3015	1 lot / 3 units	3/0 2500V
ESD: Charged Device Model	JEDEC 22-101	1 lot / 3 units	3/0 1000V
Latch-up	EIA/JESD78	1 lot / 6 units	6/0