Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **K1101-01** DATE: **14-Jan-2011**
Product Affected: Refer Attachment 1

Date Effective: **14-Apr-2011**

MEANS OF DISTINGUISHING CHANGED DEVICES:
- ■ Product Mark New ordering Part#
- ☐ Back Mark
- ☐ Date Code
- ☐ Other

Contact: Bimla Paul
Title: Product Quality Assurance
Phone #: (408) 574-6419
Fax #: (408) 284-8362
E-mail: Bimla.Paul@idt.com

Attachment: ■ Yes ☐ No

Samples: Contact your local samples representative for sample requests.

DESCRIPTION AND PURPOSE OF CHANGE:

- ☐ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ☐ Data Sheet
- ■ Other - Die revision (New ordering Part#)

IDT is advising our customers that we are introducing the 932SQ420DGLF and 932SQ420DKLF to enhance product performance. IDT requests that customers switch to the new parts due to the performance enhancement.

Refer to Attachment 1 for details & Attachment 2 for characterization data.

RELIABILITY/QUALIFICATION SUMMARY:
There is no expected change to the product quality or reliability performance.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:
IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone # /Fax #: _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT 1 - PCN #: K1101-01

PCN Type: Die revision - New ordering Part#

Data Sheet Change: Yes. New ordering Part#.

Detail Of Change:

IDT is advising our customers that we are introducing the 932SQ420DGLF and 932SQ420DKLF to enhance product performance. IDT requests that customers switch to the new parts due to the performance enhancement.

Please note that there is a change in ordering part# and data sheets for new part #s have been released. Please contact your local IDT sales representative for sample and data sheet. Changes in part# are detailed as below:

Affected Part#

Existing Part#	New Part#
932SQ420BGLF	932SQ420DGLF
932SQ420BGLFT	932SQ420DGLFT
932SQ420BKLF	932SQ420DKLF
932SQ420BKLFT	932SQ420DKLFT
932SQ420CGLF	932SQ420DGLF
932SQ420CGLFT	932SQ420DGLFT
932SQ420CKLF	932SQ420DKLF
932SQ420CKLFT	932SQ420DKLFT

932SQ420DGLF -498 Char Report

Board conditions:

Xtal 25M, X1, X2 loads: 30pF

Perfomance check: 85ohms Dedicated 64 TSSOP, SN 631

RREF = 412ohms, Diff: 2pF, Rs=27 ohms, Rp to GND= 43.2ohms, SE: 39 ohms, 5pF (PCI_2X, 48_2X) and 43 ohms, 5pF (REF 3X)

Electrical Characteristics - Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	MEASURED MIN	MEASURED TYP	MEASURED MAX	NOTES
3.3V Core Supply Voltage	VDDA				4.6	V	1,2	Guaranteed by Design (GBD)			85Ω board unless otherwise noted. 100Ω board is similar.
3.3V Logic Supply Voltage	VDD				4.6	V	1,2				
Input Low Voltage	V_{IL}		GND-0.5			V	1				
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1				
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1				
Storage Temperature	Ts		-65		150	°C	1				
Junction Temperature	Tj				125	°C	1				
Input ESD protection	ESD prot	Human Body Model	2000			V	1	2000			

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics - Input/Supply/Common Parameters

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	MIN	TYP	MAX	
Ambient Operating Temperature	T_{COM}	Commmercial range	0		70	°C	1	-10		85	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V_{DD} + 0.3	V	1	GBD			
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	1				
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	1				
	I_{INP}	Single-ended inputs. V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	1				
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1	0.7		V_{DD}	
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1	0		0.3	
Input Frequency	F_i			25.00		MHz	2		25.00		
Pin Inductance	L_{pin}				7	nH	1	GBD			
Capacitance	C_{IN}	Logic Inputs			5	pF	1				
	C_{OUT}	Output pin capacitance			5	pF	1				
	C_{INX}	X1 & X2 pins			5	pF	1				
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1.8	ms	1,2			1.3	
SS Modulation Frequency	f_{MODIN}	Allowable Frequency (Triangular Modulation)	30	31.300	33	kHz	1	31.12	31.300	31.65	
Tdrive_PD#	t_{DRVPD}	Differential output enable after PD# de-assertion			300	us	1,3			200	
Tfall	t_F	Fall time of control inputs			5	ns	1,2			10	Input spec

932SQ420DGLF -498 Char Report

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Trise	t_R	Rise time of control inputs			5	ns	1,2			10 Input spec
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	1	GBD		
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	1			
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	1			0.3
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	1	5		
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	1	GBD		
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1			
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1			
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			100	kHz	1			400

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

Electrical Characteristics - Current Consumption

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	MEASURED MIN	MEASURED TYP	MEASURED MAX
Operating Supply Current	$I_{DD3.3OP}$	All outputs active @100MHz, C_L = Full load;		385	400	mA	1			385
Powerdown Current	$I_{DD3.3PDZ}$	All differential pairs tri-stated		16	20	mA	1			16

[1]Guaranteed by design and characterization, not 100% tested in production.

DC Electrical Characteristics - Differential Current Mode Outputs

T_A = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	MEASURED MIN	MEASURED TYP	MEASURED MAX
Slew rate	Trf	Scope averaging on	1	2.4	4	V/ns	1, 2, 3	2.1	2.4	2.7
Slew rate matching	ΔTrf	Slew rate matching, Scope averaging on		9	20	%	1, 2, 4	0	9	17
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	772	850	mV	1	731	772	826
Voltage Low	VLow		-150	9	150		1	-31	9	50
Max Voltage	Vmax	Measurement on single ended signal using absolute value.		810	1150	mV	1, 7	771	810	831
Min Voltage	Vmin		-300	-17			1, 7	-39	-17	5
Vswing	Vswing	Scope averaging off	300			mV	1, 2	1446		
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	351	550	mV	1, 5	325	351	390
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		24	140	mV	1, 6	4	24	44

[1]Guaranteed by design and characterization, not 100% tested in production. IREF = VDD/(3xR_R). For R_R = **412Ω (1%)**, I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω **(85Ω differential impedance).**

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage t

Matching applies to rising edge rate for Clock and falling edge rate for Clock#.

932SQ420DGLF -498 Char Report

Board conditions:

Xtal 25M, X1, X2 loads: 30pF

Perfomance check: 85ohms Dedicated 64 TSSOP, SN 631

RREF = 412ohms, Diff: 2pF, Rs=27 ohms, Rp to GND= 43.2ohms, SE: 39 ohms, 5pF (PCI_2X, 48_2X) and 43 ohms, 5pF (REF 3X)

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross absol

[7] Includes overshoot and undershoot.

AC Electrical Characteristics - Differential Current Mode Outputs

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	MEASURED MIN	MEASURED TYP	MEASURED MAX
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	50.1	55	%	1	49.0%	50.1%	51.9%
Skew, Output to Output	t_{sk3SRC}	Across all SRC outputs, V_T = 50%		13.5	50	ps	1	13	13.5	14
Skew, Output to Output	t_{sk3CPU}	Across all CPU outputs, V_T = 50%		43	50	ps	1	38	43	48
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	CPU, SRC, NS_SAS outputs		35	50	ps	1,3	27.3	35.1	47.7
		DOT96 output		75	250	ps	1,3	62	75	88

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] $I_{REF} = V_{DD}/(3xR_R)$. For R_R = **412Ω** (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

[3] Measured from differential waveform

Electrical Characteristics - Phase Jitter Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes	MEASURED MIN	MEASURED TYP	MEASURED MAX	
Phase Jitter	$t_{jphPCIeG1}$	PCIe Gen 1		28	86	ps (p-p)	1,2,3,6	20.2	27.9	36.5	SRC, spread on and off
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.9	3	ps (rms)	1,2,6	0.7	0.9	1.0	SRC, spread on and off
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		1.7	3.1	ps (rms)	1,2,6	1.6	1.7	1.8	SRC, spread on and off
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.4	1	ps (rms)	1,2,4,6	0.32	0.37	0.42	PcieG3, 3.4 and 3.5MSRC outputs
	t_{jphQPI_SMI}	QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.15	0.5	ps (rms)	1,5,7	0.10	0.15	0.24	QPI 6.4GB, 7.8GB, CPU100, SRC and NS outputs
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.13	0.3	ps (rms)	1,5,7	0.09	0.13	0.16	CPU100, SRC and NS outputs
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.11	0.2	ps (rms)	1,5,7	0.07	0.11	0.16	CPU100, SRC and NS outputs
	$t_{jphSAS12G}$	SAS6G (Filtered REFCLK Jitter 20KHz to 20MHz.)		0.34	0.4	ps (rms)	1,8		0.30	0.34	
	$t_{jphSAS12G}$	SAS 6G/12G		0.70	1.3	ps (rms)	1,5	0.56	0.58	0.61	CPU spread off
								0.56	0.70	0.87	CPU Spread on

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] See http://www.pcisig.com for complete specs

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

932SQ420DGLF -498 Char Report

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Perfomance check: 85ohms Dedicated 64 TSSOP, SN 631

RREF = 412ohms, Diff: 2pF, Rs=27 ohms, Rp to GND= 43.2ohms, SE: 39 ohms, 5pF (PCI_2X, 48_2X) and 43 ohms, 5pF (REF 3X)

[4] Subject to final radification by PCI SIG.
[5] Calculated from Intel-supplied Clock Jitter Tool v 1.6.3
[6] Applied to SRC outputs
[7] Applies to CPU outputs
[8] Intel calculation from raw phase noise data

Electrical Characteristics - PCI

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	MEASURED MIN	MEASURED TYP	MEASURED MAX
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1		GBD	
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1	3		
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1			0.4
Output High Current	I_{OH}	MIN @V_{OH} = 1.0 V	-33			mA	1			
		MAX @V_{OH} = 3.135 V			-33	mA	1		GBD	
Output Low Current	I_{OL}	MIN @V_{OL} = 1.95 V	30			mA	1			
		MAX @ V_{OL} = 0.4 V			38	mA	1			
Clock High Time	T_{HIGH}	1.5V	12			ns	1	These parameters are met when duty cycle, PPM and cycle to cycle jitter specs are met.		
Clock Low Time	T_{LOW}	1.5V	12			ns	1			
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1	1.8	4	V/ns	1,2	1.5	1.8	2.1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	50.5	55	%	1	50.5%	50.5%	50.6%
Group Skew	t_{skew}	V_T = 1.5 V		294	500	ps	1	282	294	306
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		108	500	ps	1	86	108	173

See "Single-ended Test Loads Page" for termination circuits
[1]Guaranteed by design and characterization, not 100% tested in production.
[2] Measured between 0.8V and 2.0V

Electrical Characteristics - 48MHz

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	MEASURED MIN	MEASURED TYP	MEASURED MAX
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	20		60	Ω	1		GBD	
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1	3		
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1			0.4
Output High Current	I_{OH}	MIN @V_{OH} = 1.0 V	-29			mA	1			
		MAX @V_{OH} = 3.135 V			-33	mA	1		GBD	
Output Low Current	I_{OL}	MIN @V_{OL} = 1.95 V	29			mA	1			
		MAX @ V_{OL} = 0.4 V			27	mA	1			
Clock High Time	T_{HIGH}	1.5V	8.094		10.036	ns	1	These parameters are met when duty cycle, PPM and cycle to cycle jitter specs are met.		
Clock Low Time	T_{LOW}	1.5V	7.694		9.836	ns	1			
Edge Rate	t_{slewr/f_USB}	Rising/Falling edge rate	1	1.5	2	V/ns	1,2	1.3	1.5	1.7
Duty Cycle	d_{t1}	V_T = 1.5 V	45	51	55	%	1	50.9%	51.0%	51.1%
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		109	350	ps	1	91	109	122

See "Single-ended Test Loads Page" for termination circuits
[1]Guaranteed by design and characterization, not 100% tested in production.
[2] Measured between 0.8V and 2.0V

932SQ420DGLF -498 Char Report

Board conditions:

Xtal 25M, X1, X2 loads: 30pF

Perfomance check: 85ohms Dedicated 64 TSSOP, SN 631

RREF = 412ohms, Diff: 2pF, Rs=27 ohms, Rp to GND= 43.2ohms, SE: 39 ohms, 5pF (PCI_2X, 48_2X) and 43 ohms, 5pF (REF 3X)

Electrical Characteristics - REF

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes	MEASURED MIN	MEASURED TYP	MEASURED MAX
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1	GBD		
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1	3		
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1			0.4
Output High Current	I_{OH}	MIN @V_{OH} = 1.0 V	-33			mA	1	GBD		
		MAX @V_{OH} = 3.135 V			-33	mA	1			
Output Low Current	I_{OL}	MIN @V_{OL} = 1.95 V	30			mA	1			
		MAX @ V_{OL} = 0.4 V			38	mA	1			
Clock High Time	T_{HIGH}	1.5V	27.5			ns	1	These parameters are met when duty cycle, PPM and cycle to cycle jitter specs are met.		
Clock Low Time	T_{LOW}	1.5V	27.5			ns	1			
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1	1.9	4	V/ns	1,2	1.6	1.9	2.2
Duty Cycle	d_{t1}	V_T = 1.5 V	45	50.5	55	%	1	50.5%	50.5%	50.5%
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		75	1000	ps	1	68	75	82

See "Single-ended Test Loads Page" for termination circuits

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured between 0.8V and 2.0V

Revision History

Rev.	Issue Date	Who	Description	Page #
A	9/16/2010	RDW	Initial Release	-
B	9/22/2010	RDW	Updated SAS phase jitter spec and results	Various