Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA - 95054

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: SM-0308-02 DATE: 8/15/2003
Product Affected: 70121 / 70125 2Kx9 Dual-Port RAM

Date Effective: 11/15/2003

MEANS OF DISTINGUISHING CHANGED DEVICES:
- ■ Product Mark — Die revision "R" marked on top
- ☐ Back Mark — of the part near the date code
- ☐ Date Code
- ☐ Other

Contact: Dennis Lantz
Title: Quality/Reliability Manager
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Attachment:: ■ Yes ☐ No

Samples: Available now
Contact your IDT Sales Representative

DESCRIPTION AND PURPOSE OF CHANGE:

- ■ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ■ Manufacturing Site
- ☐ Data Sheet
- ☐ Other

To consolidate Wafer Fab production from Salinas, California (Fab 2) to Hillsboro, Oregon (Fab4). These qualified products will be transferred to IDT's Wafer Fab facility in Hillsoboro, Oregon. These devices will be upgraded from Cmos 7 (.64um) to Cmos 8 (.60um). Cmos 8 is an existing qualifed process at Fab 4.

RELIABILITY/QUALIFICATION SUMMARY:

Qualification testing has been completed and verifies that there is no change to the product reliability. Qualification details are attached

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone# /Fax# : _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

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PCN Type: Fab Site Change

Data Sheet Change None Expected

Detail of Change Transfer existing qualified products from Salinas, California Wafer Fab Facility (Fab 2) to Hillsboro, Oregon Wafer Fab Facility (Fab 4).

	Current Die Revision	Future Die Revision
Die Revision	V	R
Wafer Fab Tech	Cmos 7	Cmos 8
Wafer Size	6 inch	8 inch
# Poly Layers	2	2
# Metal Layers	2	2
Die Dimensions (sq mils)	11.96	10.92

Conversion Schedule (Estimated)

Base Device	Production Shipments and Sample Availability
70121S	Now
70125S	Now

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Qualification Plan: QSM-0304-01

Test Vehicle	**Test Results**
7132S4	Sample Size/ # of Fails
Operating Life Test: Dynamic @+135°C, Vcc=4V for 750 hours	116 / 0
High Temp. Storage Life Test (Unbiased, 1000 hours @+150°C)	77 / 0
Bake & Ballshear Test @ 200°C / 4 ball bonds per device	5 / 0
Temperature Cycling: (-65°C to +150°C, 500 cycles)	45 / 0
HAST: (Biased, 100 Hrs. @+130°C, +85%RH, 3 Atm.)	45 / 0
Autoclave:(Unbiased, 2 Atm Saturated Steam, +121°C, 168 Hrs)	45 / 0
ESD Human Body Model	9 / 0
ESD Charged Device Model	6 / 0
Latch up: (Tested to 2X Vcc)	10 / 0