Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA - 95054

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: SR-0405-02 DATE: 5/6/2004
Product Affected: IDT71256S IDT71256L

Date Effective: 8/6/2004

MEANS OF DISTINGUISHING CHANGED DEVICES:
- ☐ Product Mark
- ☐ Back Mark
- ■ Date Code Top mark will show "L4" die revision.
- ☐ Other

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Attachment:: ■ Yes ☐ No

Samples: Refer to page 2 for sample availability

DESCRIPTION AND PURPOSE OF CHANGE:

- ☐ Die Technology
- ■ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ■ Manufacturing Site
- ☐ Data Sheet
- ☐ Other

This PCN is to document wafer fab production transfer from Salinas, California (Fab 2) to Hillsboro, Oregon (Fab 4). These devices will be upgraded from Cmos 7 to Cmos 8 . Cmos 8 is an existing qualified process at Fab 4.

RELIABILITY/QUALIFICATION SUMMARY:

Device qualification details shown on attachment, verifies that there is no change to the device reliability

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone# /Fax# : _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

ATTACHMENT - PCN #: SR-0405-02

PCN Summary

PCN Type: Fab site change, technology upgrade

Commodity Memory

Forecast or Execute Execute

Planned or Unplanned Planned

Data Sheet Change None

Detail of Change Transfer existing qualified products from Salinas, California wafer fab facility (Fab 2) to Hillsboro, Oregon wafer fab facility (Fab 4).

Product	71256L	71256L4
Wafer Fab Facility	Salinas, CA	Hillsboro, OR
Wafer Fab Technology	CMOS 7	CMOS 8
Wafer Size	6 inch	8 inch
Cell Type	4T	4T
# Poly Layers	1	1
# Metal layers	2	2
Minimum Feature Size	0.64 um	0.60 um
Die Dimension / K sq mils	23.3	23.3

Sample Availability: Now

Production Shipments: Now

Product Information

Base Part Number	Curent Die Rev	New Die Rev	Interface	Vcc	Bus Width	Depth	Density
IDT71256S	L	L4	Asynchronous	5V	x8	32K	256K
IDT71256L	L	L4	Asynchronous	5V	x8	32K	256K

ATTACHMENT - PCN #: SR-0405-02

Qualification Plan #: QS-0403-04
Test Vehicle: 7164L4 / 71256L4 (Same cell type and technology)

Qualification Results

Package Type: SOJ-28

TEST DESCRIPTION	Sample Size / # Fails	Comments
High Temperature Operating Life (Dynamic) JESD22-A108, +125°C @ 1000 hours or equivalent	116/0	
Highly Accelerated Stress Test: JEDEC STD 22, Method A110, Biased, @+130°C, +85%RH, 3 Atm, 100 hours*	43/0	
Autoclave: EIA/JESD22-A102 @ 2 ATM, Saturated Steam @ 121°C, 168 hours*	45/0	
Temperature Cycling: JESD22-A104, Condition C, -65°C to +150°C, 500 cylces*	45/0	
High Temp Storage: JESD22-A103 +150°C, 1000 hours	77/0	
ESD: Human Body Model Mil-Std-883, method 3015	3/0	Rating: 1000V
ESD: Charged device Model JEDEC 22-101	3/0	Rating: 1000V
Latch-up EIA/JESD STD-78	6/0	

* Preconditioning per JESD22-A113B Level 3

Characterization Data:

Characterization available upon request.