Product Change Notice

(PCN tracking number : CST-R2-AJ094 Rev.1.0)

August 5, 2016

To: Valued RENESAS Customer

Renesas Product Summary: Standard SRAM (TSOP) products.

Change Description:
1. Site change of Back-end (assembly and final-test) process, including a change of assembly materials
2. Product integration by EOL of "-5SR, -7SI, -7SR" products and by part name unification to "-5SI" product

Reason for Change:
1. Due to obsolescence of manufacturing equipment, and material change for improvement of board-level package reliability
2. For long-time, stable supply by improvement of mass production efficiency

Identification: Identifiable by the country of origin, laser-marked on the package's surface

Anticipated Impact:
1. Packing specification is changed accompanied with the site change of Back-end process
2. Moisture Sensitivity Level is changed from MSL2 to MSL3 accompanied with a change of lead-frame material (from 42-Alloy to Cu).
3. Electrical characteristics of "-5SI" product is completely upper-compatible with "-5SR, -7SI, -7SR" products

Date of Change: From December, 2016 onward

Schedule:
1. Regarding the site change of Back-end process (excluding EOL products),
   Commercial samples: October, 2016 (November, 2016 for some part names)
   Mass production (post-change products): December, 2016
   End of production (pre-change products): June, 2017

2. Regarding the EOL of "-5SR, -7SI, -7SR" products,
   Last-Time-Buy quantity forecast to RENESAS: June, 2017
   Last Time to Order: December, 2017
   Last Time to Ship: December, 2018

Supplemental Information: Please see the page 3 to 5 and the attachments (Appendix for CST-R2-AJ094).

Contact: General Purpose Analog and Power Solution Department 3,
General Purpose Analog and Power Business Division,
2nd Solution Business Unit

Internal Reference:

Attachments: Appendix for CST-R2-AJ094

In case of any questions, please contact your Renesas sales representative.

Customer Response (to be returned by email or mail)

☐ Acknowledge	Company: _____
☐ Acceptable	Name & Position: _____
☐ Unacceptable (pls. comment)	Email: _____
☐ Not applicable	Phone: _____

Note: Acknowledgement must be received by Renesas within 30 days of delivery of the PCN or Renesas will consider the change as approved. If timely acknowledgement is provided by Customer, then Customer shall have 90 days from the date of receipt of this PCN or commercial samples in which to make any objections to the PCN. If Customer fails to make objections to this PCN within 90 days of the receipt of the PCN or commercial samples then Renesas will consider the PCN changes as approved. If customer cannot accept the PCN then customer must provide Renesas with a last time buy demand and purchase order.

Comments

_____

Signature of customer

1. Background of Change

Renesas announces 2 types of Product Changes on Standard SRAM (TSOP) products.
One is a site change of back-end (assembly and final-test site) process due to obsolescence of manufacturing equipment. It also includes a change of assembly materials for improvement of board-level package reliability.
The other is a product integration by EOL of "-5SR, -7SI, -7SR" products and by part name unification to "-5SI" product. It aims for long-time, stable supply by improvement of mass production efficiency.
We greatly appreciate your kind understanding and early approval for this notification.

2. Details of Change

(1) The site of Back-end process is transferred from "Renesas Semiconductor Beijing (Assembly and Final-test site)" to "Amkor Technology Malaysia (Assembly site)" and to "Powertech Technology Inc. (Final-test site)".

(2) Regarding assembly material change,
  (a) Lead frame material is changed from 42-Alloy to Cu, and moisture sensitivity level is changed from MSL2 to MSL3. (No change of lead frame material and MSL in existing Cu-products.)
  (b) Lead plating material is changed from Sn-Cu to Sn. (No change of lead plating in existing Sn-products.)

(3) Regarding the EOL of "-5SR, -7SI, -7SR" products,
  (a) "Access and Temperature grades" of "-5SR, -7SI, -7SR" in 256Kb to 4Mb Low Power SRAM products are put to EOL, and part name of the products are unified to "-5SI".
  (b) Electrical characteristics (DC/AC) of unified "-5SI" product are completely upper-compatible with "-5SR, -7SI, -7SR" products.
  (c) The unified "-5SI" products are processed under the post-change condition as described in above (1) and (2).

(4) Regarding these changes,
  (a) There are no changes in the site of Front-end (Wafer) process or revision of photomasks.
  (b) Package outline and pin configuration is equivalent to those of pre-change products.
  (c) Reliability and quality level are equivalent to those of pre-change products.
  (d) Electrical characteristics (DC/AC) are equivalent to those of pre-change products, excluding "-5SR, -7SI, -7SR" of pre-change products.
  (e) Packing specification is changed (both in tray and reel shipment.) For more detailed information, see the appendix for CST-R2-AJ094.

Comparison

Item			Pre Change	Post Change
Assembly	Company		Renesas Semiconductor Beijing	Amkor Technology Malaysia
	Country		China	Malaysia
	Material	Lead frame	Cu or 42Alloy (*)	Cu
		Lead plating	Sn or Sn-Cu (*)	Sn
	Package marking specification		Country of origin "CHINA"	Country of origin "MALAYSIA"
Final test	Company		Renesas Semiconductor Beijing	Powertech Technology Inc.
	Country		China	Taiwan
Moisture Sensitivity Level			MSL 3 or 2 (*)	MSL 3
Packing specification	Tray packing		Please see the appendix.	Please see the appendix.
	Tape & Reel packing		Please see the appendix.	Please see the appendix.

(*) Pre-change products have two types of assembly material. Please see the attachments (Appendix for CST-R2-AJ094).

3. Release Support and Milestones

Sample submission	Commercial samples : October, 2016 (November, 2016 for R1RP0416DSB, R1RW0416DSB and R1LV1616HSA)
Renesas report	Reliability report : October, 2016 (November, 2016 for R1RP0416DSB, R1RW0416DSB and R1LV1616HSA)

4. Identification

Identifiable by the country of origin, laser-marked on the package's surface

5. Schedule

(1) Regarding the site change of Back-end process (excluding EOL products),

Commercial samples: October, 2016 (November, 2016 for some part names)

Mass production (post-change products): December, 2016

End of production (pre-change products): June, 2017

(2) Regarding the EOL of "-5SR, -7SI, -7SR" products,

Last-Time-Buy quantity forecast to RENESAS: June, 2017

Last Time to Order: December, 2017

Last Time to Ship: December, 2018

6. Supplemental Information

Please see the attachments (Appendix for CST-R2-AJ094).

7. Product list

Package Type	Product Type (Memory Cap., Supply Voltage)	Orderable part name	
		Pre Change	Post Change
28pin-TSOP(I)	256Kb 5V	R1LP5256ESA-5SI, -5SR, -7SI, -7SR#B0	R1LP5256ESA-5SI#B1
		R1LP5256ESA-5SI, -5SR, -7SI, -7SR#S0	R1LP5256ESA-5SI#S1
	256Kb 3V	R1LV5256ESA-5SI, -5SR, -7SI, -7SR#B0	R1LV5256ESA-5SI#B1
		R1LV5256ESA-5SI, -5SR, -7SI, -7SR#S0	R1LV5256ESA-5SI#S1
32pin-TSOP(I)	1Mb 5V	R1LP0108ESF-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESF-5SI#B1
		R1LP0108ESF-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESF-5SI#S1
	1Mb 3V	R1LV0108ESF-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESF-5SI#B1
		R1LV0108ESF-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESF-5SI#S1
32pin-sTSOP	1Mb 5V	R1LP0108ESA-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESA-5SI#B1
		R1LP0108ESA-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESA-5SI#S1
	1Mb 3V	R1LV0108ESA-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESA-5SI#B1
		R1LV0108ESA-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESA-5SI#S1
	2Mb 3V	R1LV0208BSA-5SI, -7SI#B0	R1LV0208BSA-5SI#B1
		R1LV0208BSA-5SI, -7SI#S0	R1LV0208BSA-5SI#S1
32pin-TSOP(II)	4Mb 5V	R1LP0408DSB-5SI, -5SR, -7SI, -7SR#B0	R1LP0408DSB-5SI#B1
		R1LP0408DSB-5SI, -5SR, -7SI, -7SR#S0	R1LP0408DSB-5SI#S1
44pin-TSOP(II)	2Mb 3V	R1LV0216BSB-5SI, -7SI#B0	R1LV0216BSB-5SI#B1
		R1LV0216BSB-5SI, -7SI#S0	R1LV0216BSB-5SI#S1
	4Mb Fast 5V	R1RP0416DSB-0PI, -0PR, -2LR, -2PI, -2PR, -2SR#D0	R1RP0416DSB-0PI, -0PR, -2LR, -2PI, -2PR, -2SR#D1
		R1RP0416DSB-2LR, -2PR#S0	R1RP0416DSB-2LR, -2PR#S1
	4Mb Fast 3V	R1RW0416DSB-0PI, -0PR, -2LR, -2PI, -2PR, -2SR, -2UR#D0	R1RW0416DSB-0PI, -0PR, -2LR, -2PI, -2PR, -2SR, -2UR#D1
		R1RW0416DSB-0PI, -0PR, -2PI, -2PR#S0	R1RW0416DSB-0PI, -0PR, -2PI, -2PR#S1
48pin-TSOP(I)	16Mb 3V	R1LV1616HSA-4SI, -5SI#B0	R1LV1616HSA-4SI, -5SI#B1
		R1LV1616HSA-4SI, -5SI#S0	R1LV1616HSA-4SI, -5SI#S1
	32Mb 3V	R1LV3216RSA-5SI#B0	R1LV3216RSA-5SI#B1
		R1LV3216RSA-5SI#S0	R1LV3216RSA-5SI#S1

To: Valued RENESAS customer,

General Purpose Analog and Power Solution Department 3
General Purpose Analog and Power Business Division
2nd Solution Business Unit
Renesas Electronics Corporation

August 5, 2016

Appendix for CST-R2-AJ094
(Standard SRAM (TSOP) products)

This appendix states the detailed information of PCN: CST-R2-AJ094 (Site change of Back-end (assembly and final-test) process and product integration by EOL of “-5SR, -7SI, -7SR” products).

Contents

© 2016 Renesas Electronics Corporation. All rights reserved.

1. Product List

(1) 28pin-TSOP(I), 32pin-TSOP(I), 32pin-sTSOP package

Package Type	Product Type (Memory Cap., Supply Voltage)	Organization (bit)	Orderable Part Name		Packing Type	Page No. of Comparison Table
			Pre Change	**Post Change**		
28pin-TSOP(I)	256Kb 5V	x8	R1LP5256ESA-5SI#B0	R1LP5256ESA-5SI#B1	Tray	p.4, p.17, pp.19-20
			R1LP5256ESA-5SR#B0			
			R1LP5256ESA-7SI#B0			
			R1LP5256ESA-7SR#B0			
			R1LP5256ESA-5SI#S0	R1LP5256ESA-5SI#S1	Tape & Reel	
			R1LP5256ESA-5SR#S0			
			R1LP5256ESA-7SI#S0			
			R1LP5256ESA-7SR#S0			
	256Kb 3V	x8	R1LV5256ESA-5SI#B0	R1LV5256ESA-5SI#B1	Tray	p.5, p.17, pp.21-22
			R1LV5256ESA-5SR#B0			
			R1LV5256ESA-7SI#B0			
			R1LV5256ESA-7SR#B0			
			R1LV5256ESA-5SI#S0	R1LV5256ESA-5SI#S1	Tape & Reel	
			R1LV5256ESA-5SR#S0			
			R1LV5256ESA-7SI#S0			
			R1LV5256ESA-7SR#S0			
32pin-TSOP(I)	1Mb 5V	x8	R1LP0108ESF-5SI#B0	R1LP0108ESF-5SI#B1	Tray	p.6, p.17, pp.23-24
			R1LP0108ESF-5SR#B0			
			R1LP0108ESF-7SI#B0			
			R1LP0108ESF-7SR#B0			
			R1LP0108ESF-5SI#S0	R1LP0108ESF-5SI#S1	Tape & Reel	
			R1LP0108ESF-5SR#S0			
			R1LP0108ESF-7SI#S0			
			R1LP0108ESF-7SR#S0			
	1Mb 3V	x8	R1LV0108ESF-5SI#B0	R1LV0108ESF-5SI#B1	Tray	p.7, p.17, pp.25-26
			R1LV0108ESF-5SR#B0			
			R1LV0108ESF-7SI#B0			
			R1LV0108ESF-7SR#B0			
			R1LV0108ESF-5SI#S0	R1LV0108ESF-5SI#S1	Tape & Reel	
			R1LV0108ESF-5SR#S0			
			R1LV0108ESF-7SI#S0			
			R1LV0108ESF-7SR#S0			
32pin-sTSOP	1Mb 5V	x8	R1LP0108ESA-5SI#B0	R1LP0108ESA-5SI#B1	Tray	p.8, p.18, pp.23-24
			R1LP0108ESA-5SR#B0			
			R1LP0108ESA-7SI#B0			
			R1LP0108ESA-7SR#B0			
			R1LP0108ESA-5SI#S0	R1LP0108ESA-5SI#S1	Tape & Reel	
			R1LP0108ESA-5SR#S0			
			R1LP0108ESA-7SI#S0			
			R1LP0108ESA-7SR#S0			
	1Mb 3V	x8	R1LV0108ESA-5SI#B0	R1LV0108ESA-5SI#B1	Tray	p.9, p.18, pp.25-26
			R1LV0108ESA-5SR#B0			
			R1LV0108ESA-7SI#B0			
			R1LV0108ESA-7SR#B0			
			R1LV0108ESA-5SI#S0	R1LV0108ESA-5SI#S1	Tape & Reel	
			R1LV0108ESA-5SR#S0			
			R1LV0108ESA-7SI#S0			
			R1LV0108ESA-7SR#S0			
	2Mb 3V	x8	R1LV0208BSA-5SI#B0	R1LV0208BSA-5SI#B1	Tray	p.10, p.18, pp.27-28
			R1LV0208BSA-7SI#B0			
			R1LV0208BSA-5SI#S0	R1LV0208BSA-5SI#S1	Tape & Reel	
			R1LV0208BSA-7SI#S0			

© 2016 Renesas Electronics Corporation. All rights reserved.

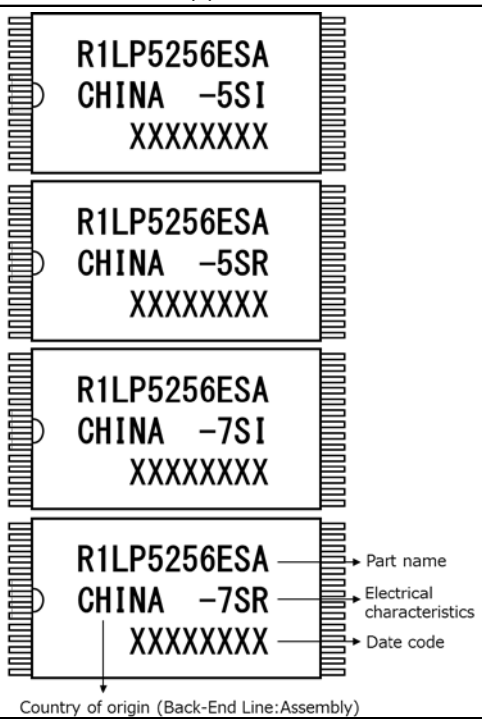
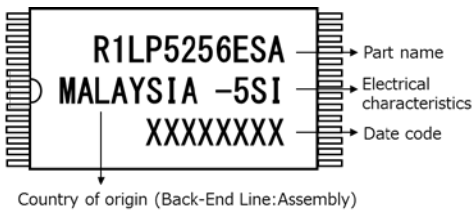
(2) 32pin-TSOP(II), 44pin-TSOP(II), 48pin-TSOP(I) package

Package Type	Product Type (Memory Cap., Supply Voltage)	Organi-zation (bit)	Orderable Part Name		Packing Type	Page No. of Comparison Table
			Pre Change	**Post Change**		
32pin-TSOP(II)	4Mb 5V	x8	R1LP0408DSB-5SI#B0	R1LP0408DSB-5SI#B1	Tray	p.11, p.18, pp.29-30
			R1LP0408DSB-5SR#B0			
			R1LP0408DSB-7SI#B0			
			R1LP0408DSB-7SR#B0			
			R1LP0408DSB-5SI#S0	R1LP0408DSB-5SI#S1	Tape & Reel	
			R1LP0408DSB-5SR#S0			
			R1LP0408DSB-7SI#S0			
			R1LP0408DSB-7SR#S0			
44pin-TSOP(II)	2Mb 3V	x16	R1LV0216BSB-5SI#B0	R1LV0216BSB-5SI#B1	Tray	p.12, p.18, pp.31-32
			R1LV0216BSB-7SI#B0			
			R1LV0216BSB-5SI#S0	R1LV0216BSB-5SI#S1	Tape & Reel	
			R1LV0216BSB-7SI#S0			
	4Mb Fast 5V	x16	R1RP0416DSB-0PI#D0	R1RP0416DSB-0PI#D1	Tray	p.13
			R1RP0416DSB-0PR#D0	R1RP0416DSB-0PR#D1	Tray	
			R1RP0416DSB-2LR#D0	R1RP0416DSB-2LR#D1	Tray	
			R1RP0416DSB-2LR#S0	R1RP0416DSB-2LR#S1	Tape & Reel	
			R1RP0416DSB-2PI#D0	R1RP0416DSB-2PI#D1	Tray	
			R1RP0416DSB-2PR#D0	R1RP0416DSB-2PR#D1	Tray	
			R1RP0416DSB-2PR#S0	R1RP0416DSB-2PR#S1	Tape & Reel	
			R1RP0416DSB-2SR#D0	R1RP0416DSB-2SR#D1	Tray	
	4Mb Fast 3V	x16	R1RW0416DSB-0PI#D0	R1RW0416DSB-0PI#D1	Tray	p.14
			R1RW0416DSB-0PI#S0	R1RW0416DSB-0PI#S1	Tape & Reel	
			R1RW0416DSB-0PR#D0	R1RW0416DSB-0PR#D1	Tray	
			R1RW0416DSB-0PR#S0	R1RW0416DSB-0PR#S1	Tape & Reel	
			R1RW0416DSB-2LR#D0	R1RW0416DSB-2LR#D1	Tray	
			R1RW0416DSB-2PI#D0	R1RW0416DSB-2PI#D1	Tray	
			R1RW0416DSB-2PI#S0	R1RW0416DSB-2PI#S1	Tape & Reel	
			R1RW0416DSB-2PR#D0	R1RW0416DSB-2PR#D1	Tray	
			R1RW0416DSB-2PR#S0	R1RW0416DSB-2PR#S1	Tape & Reel	
			R1RW0416DSB-2SR#D0	R1RW0416DSB-2SR#D1	Tray	
			R1RW0416DSB-2UR#D0	R1RW0416DSB-2UR#D1	Tray	
48pin-TSOP(I)	16Mb 3V	x16	R1LV1616HSA-4SI#B0	R1LV1616HSA-4SI#B1	Tray	p.15
			R1LV1616HSA-4SI#S0	R1LV1616HSA-4SI#S1	Tape & Reel	
			R1LV1616HSA-5SI#B0	R1LV1616HSA-5SI#B1	Tray	
			R1LV1616HSA-5SI#S0	R1LV1616HSA-5SI#S1	Tape & Reel	
	32Mb 3V	x16	R1LV3216RSA-5SI#B0	R1LV3216RSA-5SI#B1	Tray	p.16
			R1LV3216RSA-5SI#S0	R1LV3216RSA-5SI#S1	Tape & Reel	

© 2016 Renesas Electronics Corporation. All rights reserved.

2. Comparison table

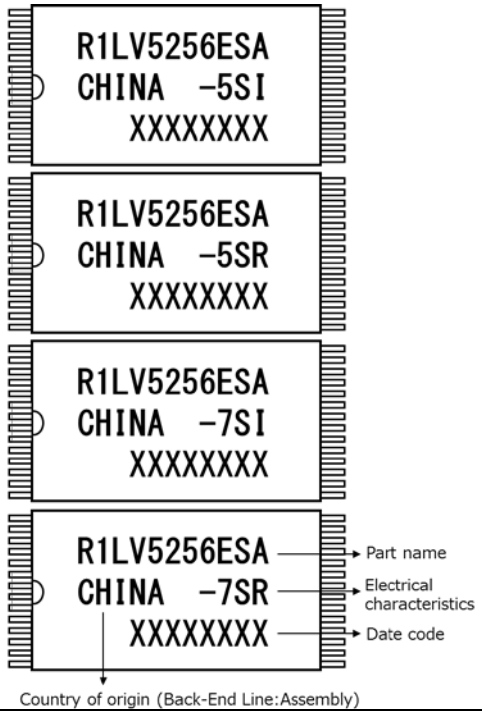
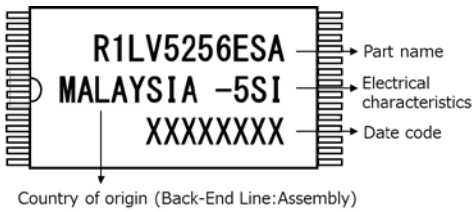
(1) 28pin-TSOP(I) 256Kb(5V) Part name : R1LP5256ESA

Item		Pre Change	Post Change
Orderable part name		R1LP5256ESA-5SI/-5SR/-7SI/-7SR#B0 (Tray packing)	R1LP5256ESA-5SI#B1 (Tray packing)
		R1LP5256ESA-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP5256ESA-5SI#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(1)28-8x11.8-0.55	P-TSOP(1)28-8x11.8-0.55
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 11.8mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 11.8mm)
	Storage number	234pcs/tray	234pcs/tray
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

- Note: Regarding the details of change in the tray and embossed tape, please see pp.33-34.

© 2016 Renesas Electronics Corporation. All rights reserved.

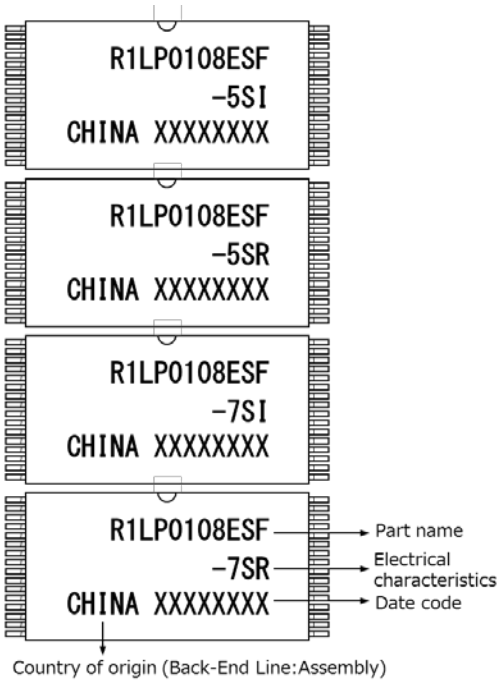
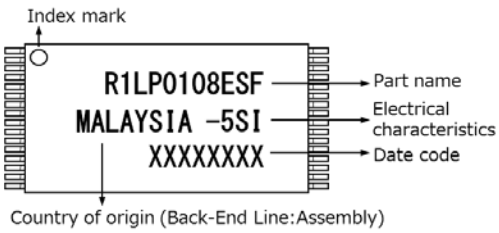
(2) 28pin-TSOP(I) 256Kb(3V) Part name : R1LV5256ESA

Item		Pre Change	Post Change
Orderable part name		R1LV5256ESA-5SI/-5SR/-7SI/-7SR#B0 (Tray packing) R1LV5256ESA-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LV5256ESA-5SI#B1 (Tray packing) R1LV5256ESA-5SI#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(1)28-8x11.8-0.55	P-TSOP(1)28-8x11.8-0.55
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 11.8mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 11.8mm)
	Storage number	234pcs/tray	234pcs/tray
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

- Note: Regarding the details of change in the tray and embossed tape, please see pp.33-34.

© 2016 Renesas Electronics Corporation. All rights reserved.

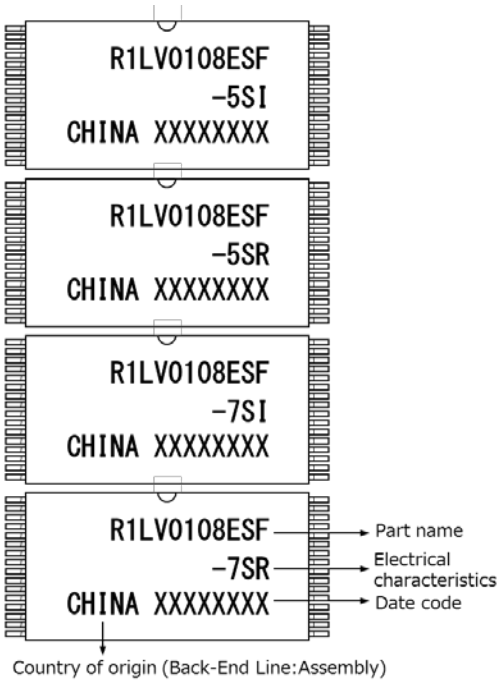
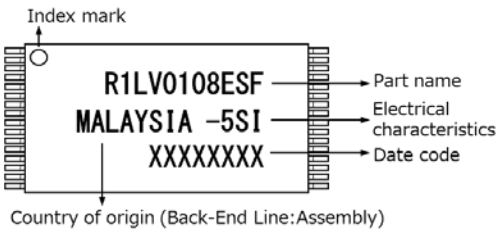
(3) 32pin-TSOP(I) 1Mb(5V) Part name : R1LP0108ESF

Item		Pre Change	Post Change
Orderable part name		R1LP0108ESF-5SI/-5SR/-7SI/-7SR#B0 (Tray packing) R1LP0108ESF-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP0108ESF-5SI#B1 (Tray packing) R1LP0108ESF-5SI#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(1)32-8x18.4-0.50	P-TSOP(1)32-8x18.4-0.50
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 18.4mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 18.4mm)
	Storage number	156pcs/tray	156pcs/tray
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

- Note: Regarding the details of change in the tray and embossed tape, please see pp.33-34.

© 2016 Renesas Electronics Corporation. All rights reserved.

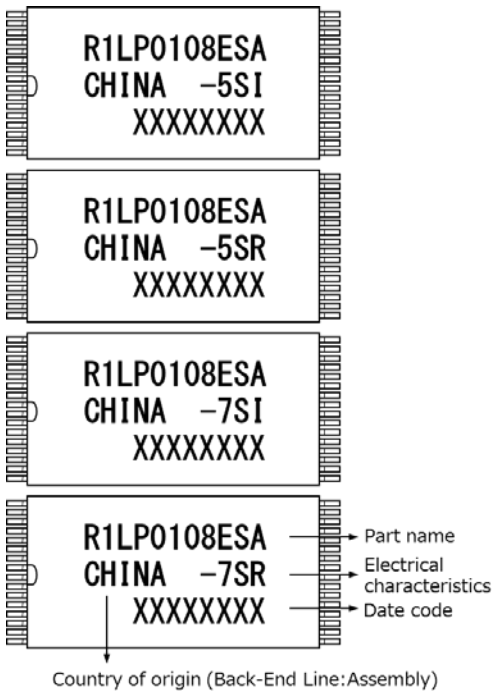
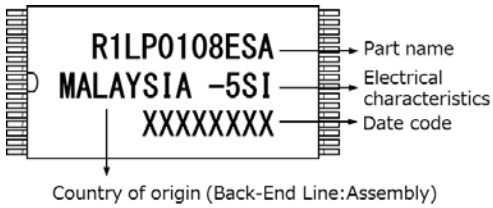
(4) 32pin-TSOP(I) 1Mb(3V) Part name : R1LV0108ESF

Item		Pre Change	Post Change
Orderable part name		R1LV0108ESF-5SI/-5SR/-7SI/-7SR#B0 (Tray packing)	R1LV0108ESF-5SI#B1 (Tray packing)
		R1LV0108ESF-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LV0108ESF-5SI#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(1)32-8x18.4-0.50	P-TSOP(1)32-8x18.4-0.50
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 18.4mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 18.4mm)
	Storage number	156pcs/tray	156pcs/tray
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

- Note: Regarding the details of change in the tray and embossed tape, please see pp.33-34.

© 2016 Renesas Electronics Corporation. All rights reserved.

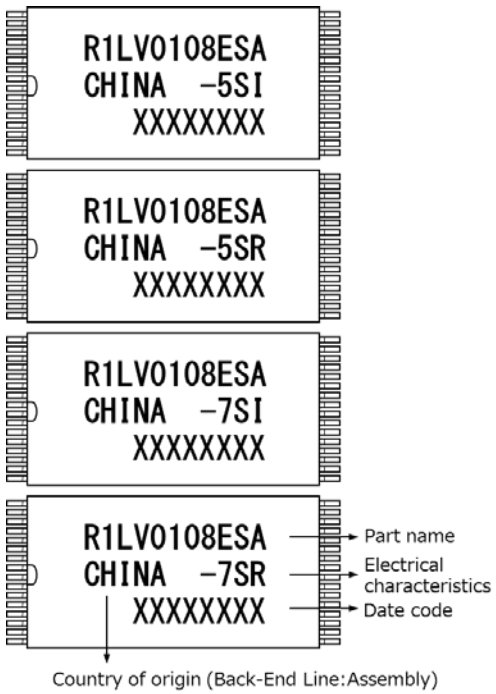
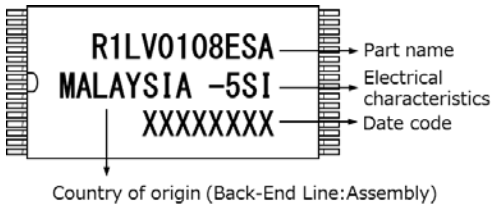
(5) 32pin-sTSOP 1Mb(5V) Part name : R1LP0108ESA

Item		Pre Change	Post Change
Orderable part name		R1LP0108ESA-5SI/-5SR/-7SI/-7SR#B0 (Tray packing)	R1LP0108ESA-5SI#B1 (Tray packing)
		R1LP0108ESA-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP0108ESA-5SI#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(1)32-8x11.8-0.50	P-TSOP(1)32-8x11.8-0.50
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 11.8mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 11.8mm)
	Storage number	234pcs/tray	234pcs/tray
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

- Note: Regarding the details of change in the tray and embossed tape, please see pp.33-34.

© 2016 Renesas Electronics Corporation. All rights reserved.

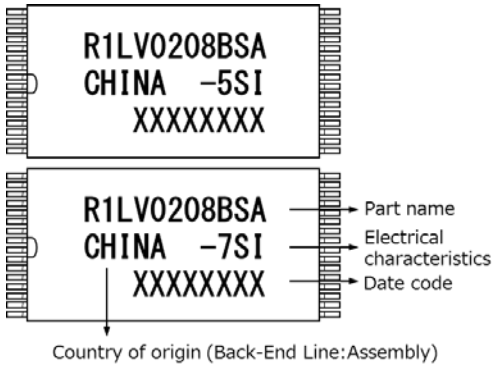
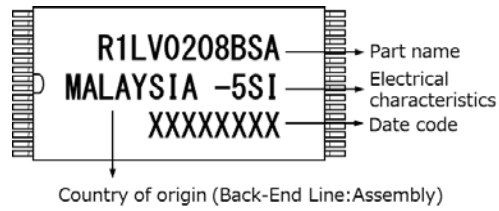
(6) 32pin-sTSOP 1Mb(3V) Part name : R1LV0108ESA

Item		Pre Change	Post Change
Orderable part name		R1LV0108ESA-5SI/-5SR/-7SI/-7SR#B0 (Tray packing) R1LV0108ESA-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LV0108ESA-5SI#B1 (Tray packing) R1LV0108ESA-5SI#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(1)32-8x11.8-0.50	P-TSOP(1)32-8x11.8-0.50
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 11.8mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 11.8mm)
	Storage number	234pcs/tray	234pcs/tray
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

- Note: Regarding the details of change in the tray and embossed tape, please see pp.33-34.

© 2016 Renesas Electronics Corporation. All rights reserved.

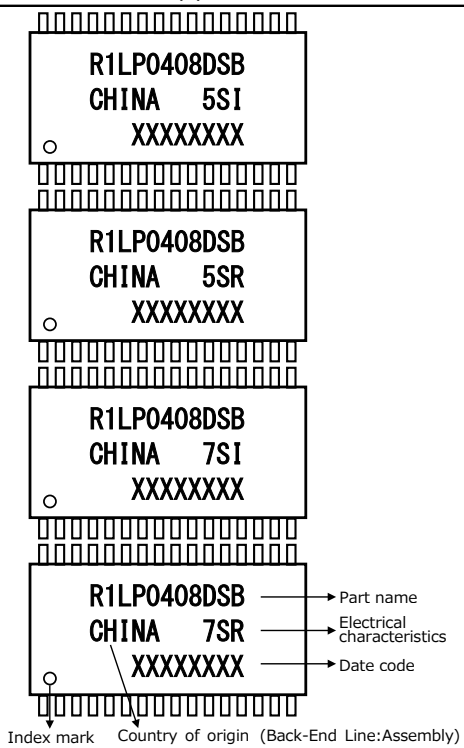
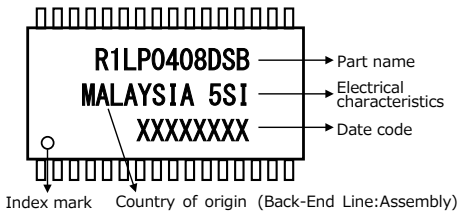
(7) 32pin-sTSOP 2Mb(3V) x8 Part name : R1LV0208BSA

Item		Pre Change	Post Change
Orderable part name		R1LV0208BSA-5SI/-7SI#B0 (Tray packing)	R1LV0208BSA-5SI#B1 (Tray packing)
		R1LV0208BSA-5SI/-7SI#S0 (Tape & Reel packing)	R1LV0208BSA-5SI#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(1)32-8x11.8-0.50	P-TSOP(1)32-8x11.8-0.50
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 11.8mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 11.8mm)
	Storage number	234pcs/tray	234pcs/tray
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

- Note: Regarding the details of change in the tray and embossed tape, please see pp.33-34.

© 2016 Renesas Electronics Corporation. All rights reserved.

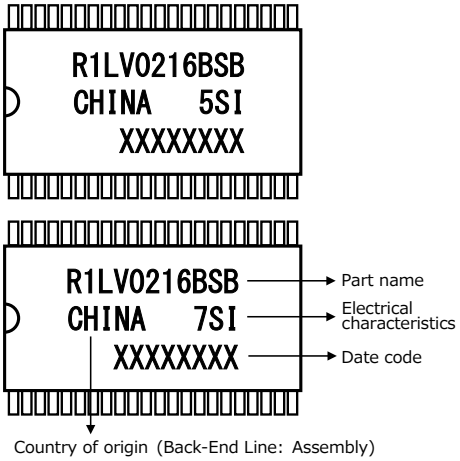
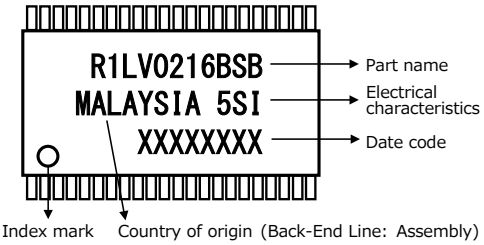
(8) 32pin-TSOP(II) 4Mb(5V) Part name : R1LP0408DSB

Item		Pre Change	Post Change
Orderable part name		R1LP0408DSB-5SI/-5SR/-7SI/-7SR#B0 (Tray packing) R1LP0408DSB-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP0408DSB-5SI#B1 (Tray packing) R1LP0408DSB-5SI#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(2)32-10.16x20.95-1.27	P-TSOP(2)32-10.16x20.95-1.27
Package marking specification			
Assembly Material	Lead frame material	Cu	Cu
	Lead plating	Sn (pure tin)	Sn (pure tin)
	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-free)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP II package size: 10.16mm x 20.95mm)	JEDEC Tray without Renesas Logo (TSOP II package size: 10.16mm x 20.95mm)
	Storage number	117pcs/tray	117pcs/tray
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 3	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin)

- Note: Regarding the details of change in the tray and embossed tape, please see pp.33-34.

© 2016 Renesas Electronics Corporation. All rights reserved.

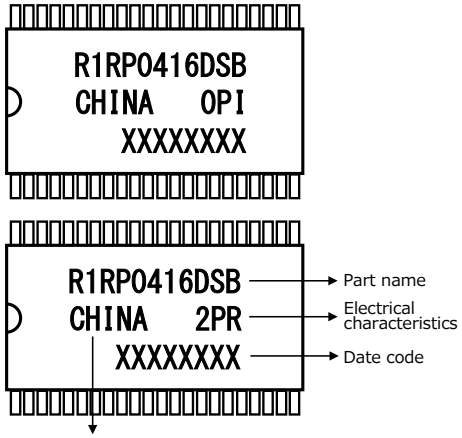
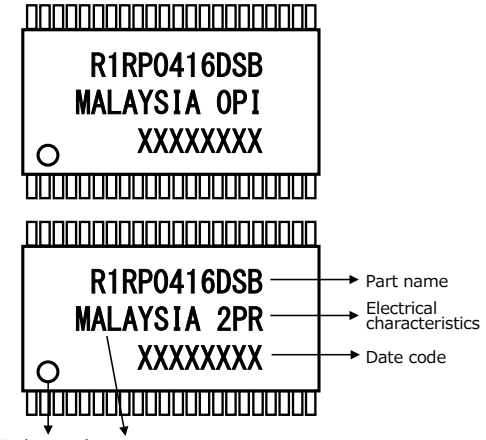
(9) 44pin-TSOP(II) 2Mb(3V) x16 Part name : R1LV0216BSB

Item		Pre Change	Post Change
Orderable part name		R1LV0216BSB-5SI/-7SI#B0 (Tray packing)	R1LV0216BSB-5SI#B1 (Tray packing)
		R1LV0216BSB-5SI/-7SI#S0 (Tape & Reel packing)	R1LV0216BSB-5SI#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(2)44-10.16x18.41-0.80	P-TSOP(2)44-10.16x18.41-0.80
Package marking specification			
Assembly Material	Lead frame material	Cu	Cu
	Lead plating	Sn (pure tin)	Sn (pure tin)
	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-free)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP II package size: 10.16mm x 18.41mm)	JEDEC Tray without Renesas Logo (TSOP II package size: 10.16mm x 18.41mm)
	Storage number	135pcs/tray	135pcs/tray
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 3	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin)

- Note: Regarding the details of change in the tray and embossed tape, please see pp.33-34.

© 2016 Renesas Electronics Corporation. All rights reserved.

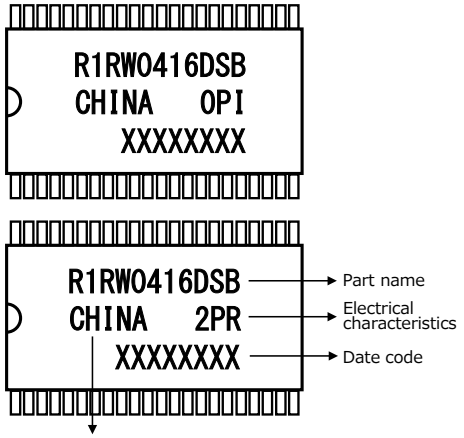
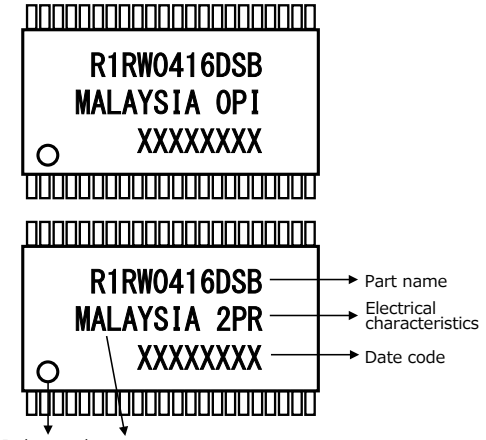
(10) 44pin-TSOP(II) 4Mb Fast 5V Part name : R1RP0416DSB

Item		Pre Change	Post Change
Orderable part name		R1RP0416DSB-0PI/-0PR/-2LR/-2PI/-2PR/-2SR#D0 (Tray packing)	R1RP0416DSB-0PI/-0PR/-2LR/-2PI/-2PR/-2SR#D1 (Tray packing)
		R1RP0416DSB-2LR/-2PR#S0 (Tape & Reel packing)	R1RP0416DSB-2LR/-2PR#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(2)44-10.16x18.41-0.80	P-TSOP(2)44-10.16x18.41-0.80
Package marking specification (No change in display of Electrical characteristics)			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy film	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP II package size: 10.16mm x 18.41mm)	JEDEC Tray without Renesas Logo (TSOP II package size: 10.16mm x 18.41mm)
	Storage number	135pcs/tray	135pcs/tray
	Laying direction of Ics on a tray	Direction from the bottm right position to the up side (when the position of chamfer in tray's corner is bottom left.)	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

- Note: Regarding the details of change in the tray and embossed tape, please see pp.33-34.

© 2016 Renesas Electronics Corporation. All rights reserved.

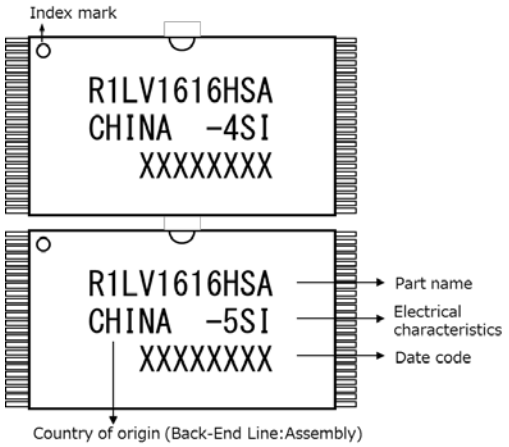
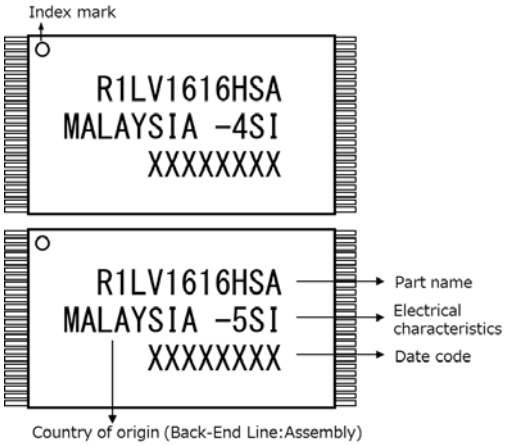
(11) 44pin-TSOP(II) 4Mb Fast 3V Part name : R1RW0416DSB

Item		Pre Change	Post Change
Orderable part name		R1RW0416DSB-0PI/-0PR/-2LR/-2PI/-2PR/-2SR/-2UR#D0 (Tray packing) R1RW0416DSB-0PI/-0PR/-2PI/-2PR#S0 (Tape & Reel packing)	R1RW0416DSB-0PI/-0PR/-2LR/-2PI/-2PR/-2SR/-2UR#D1 (Tray packing) R1RW0416DSB-0PI/-0PR/-2PI/-2PR#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(2)44-10.16x18.41-0.80	P-TSOP(2)44-10.16x18.41-0.80
Package marking specification (No change in display of Electrical characteristics)			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy film	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP II package size: 10.16mm x 18.41mm)	JEDEC Tray without Renesas Logo (TSOP II package size: 10.16mm x 18.41mm)
	Storage number	135pcs/tray	135pcs/tray
	Laying direction of Ics on a tray	Direction from the bottm right position to the up side (when the position of chamfer in tray's corner is bottom left.)	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

- Note: Regarding the details of change in the tray and embossed tape, please see pp.33-34.

© 2016 Renesas Electronics Corporation. All rights reserved.

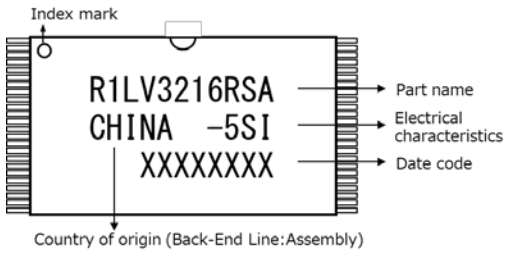
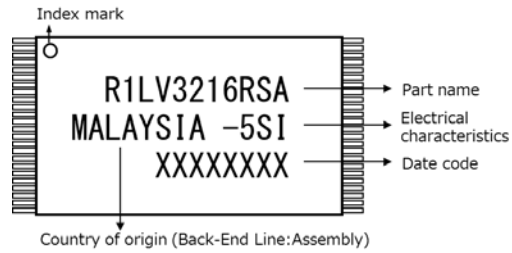
(12) 48pin-TSOP(I) 16Mb 3V Part name : R1LV1616HSA

Item		Pre Change	Post Change
Orderable part name		R1LV1616HSA-4SI/-5SI#B0 (Tray packing)	R1LV1616HSA-4SI/-5SI#B1 (Tray packing)
		R1LV1616HSA-4SI/-5SI#S0 (Tape & Reel packing)	R1LV1616HSA-4SI/-5SI#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(1)48-12x18.4-0.50	P-TSOP(1)48-12x18.4-0.50
Package marking specification (No change in display of Electrical characteristics)			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy film	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 12mm x 18.4mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 12mm x 18.4mm)
	Storage number	96pcs/tray	96pcs/tray
	Laying direction of Ics on a tray	Direction from the bottm right position to the up side (when the position of chamfer in tray's corner is bottom left.)	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

- Note: Regarding the details of change in the tray and embossed tape, please see pp.33-34.

© 2016 Renesas Electronics Corporation. All rights reserved.

(13) 48pin-TSOP(I) 32Mb 3V Part name : R1LV3216RSA

Item		Pre Change	Post Change
Orderable part name		R1LV3216RSA-5SI#B0 (Tray packing)	R1LV3216RSA-5SI#B1 (Tray packing)
		R1LV3216RSA-5SI#S0 (Tape & Reel packing)	R1LV3216RSA-5SI#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(1)48-12x18.4-0.50	P-TSOP(1)48-12x18.4-0.50
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy film	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 12mm x 18.4mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 12mm x 18.4mm)
	Storage number	96pcs/tray	96pcs/tray
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

- Note: Regarding the details of change in the tray and embossed tape, please see pp.33-34.

© 2016 Renesas Electronics Corporation. All rights reserved.

3. Product integration by EOL of “-5SR, -7SI, -7SR” products (for 256Kb ~ 4Mb Low Power SRAM)

■ Regarding the EOL of “-5SR, -7SI, -7SR” products, these "Access and Temperature grades" are unified to "-5SI" (see below).

(1) 28pin-TSOP(I), 32pin-TSOP(I)

Package Type	Memory Cap., Supply Voltage	bit	Pre Change			Post Change		
			Orderable Part Name	Access time	Operation temp.	Orderable Part Name	Access time	Operation temp.
28pin-TSOP(I)	256Kb 5V	x8	R1LP5256ESA-5SI#B0 R1LP5256ESA-5SI#S0	55ns	-40℃ ～85℃	R1LP5256ESA-5SI#B1 R1LP5256ESA-5SI#S1	55ns	-40℃ ～85℃
			R1LP5256ESA-5SR#B0 R1LP5256ESA-5SR#S0		-0℃ ～70℃			
			R1LP5256ESA-7SI#B0 R1LP5256ESA-7SI#S0	70ns	-40℃ ～85℃			
			R1LP5256ESA-7SR#B0 R1LP5256ESA-7SR#S0		0℃ ～70℃			
	256Kb 3V	x8	R1LV5256ESA-5SI#B0 R1LV5256ESA-5SI#S0	55ns	-40℃ ～85℃	R1LV5256ESA-5SI#B1 R1LV5256ESA-5SI#S1	55ns	-40℃ ～85℃
			R1LV5256ESA-5SR#B0 R1LV5256ESA-5SR#S0		-0℃ ～70℃			
			R1LV5256ESA-7SI#B0 R1LV5256ESA-7SI#S0	70ns	-40℃ ～85℃			
			R1LV5256ESA-7SR#B0 R1LV5256ESA-7SR#S0		0℃ ～70℃			
32pin-TSOP(I)	1Mb 5V	x8	R1LP0108ESF-5SI#B0 R1LP0108ESF-5SI#S0	55ns	-40℃ ～85℃	R1LP0108ESF-5SI#B1 R1LP0108ESF-5SI#S1	55ns	-40℃ ～85℃
			R1LP0108ESF-5SR#B0 R1LP0108ESF-5SR#S0		-0℃ ～70℃			
			R1LP0108ESF-7SI#B0 R1LP0108ESF-7SI#S0	70ns	-40℃ ～85℃			
			R1LP0108ESF-7SR#B0 R1LP0108ESF-7SR#S0		0℃ ～70℃			
	1Mb 3V	x8	R1LV0108ESF-5SI#B0 R1LV0108ESF-5SI#S0	55ns	-40℃ ～85℃	R1LV0108ESF-5SI#B1 R1LV0108ESF-5SI#S1	55ns	-40℃ ～85℃
			R1LV0108ESF-5SR#B0 R1LV0108ESF-5SR#S0		-0℃ ～70℃			
			R1LV0108ESF-7SI#B0 R1LV0108ESF-7SI#S0	70ns	-40℃ ～85℃			
			R1LV0108ESF-7SR#B0 R1LV0108ESF-7SR#S0		0℃ ～70℃			

- #B0: Tray packing, #S0: Tape & Reel packing. #B1: Tray packing, #S1: Tape & Reel packing.

© 2016 Renesas Electronics Corporation. All rights reserved.

(2) 32pin-sTSOP, 32pin-TSOP(II), 44pin-TSOP(II)

Package Type	Memory Cap., Supply Voltage	bit	Pre Change			Post Change		
			Orderable Part Name	Access time	Operation temp.	Orderable Part Name	Access time	Operation temp.
32pin-sTSOP	1Mb 5V	x8	R1LP0108ESA-5SI#B0 R1LP0108ESA-5SI#S0	55ns	-40℃ ～85℃	R1LP0108ESA-5SI#B1 R1LP0108ESA-5SI#S1	55ns	-40℃ ～85℃
			R1LP0108ESA-5SR#B0 R1LP0108ESA-5SR#S0		-0℃ ～70℃			
			R1LP0108ESA-7SI#B0 R1LP0108ESA-7SI#S0	70ns	-40℃ ～85℃			
			R1LP0108ESA-7SR#B0 R1LP0108ESA-7SR#S0		0℃ ～70℃			
	1Mb 3V	x8	R1LV0108ESA-5SI#B0 R1LV0108ESA-5SI#S0	55ns	-40℃ ～85℃	R1LV0108ESA-5SI#B1 R1LV0108ESA-5SI#S1	55ns	-40℃ ～85℃
			R1LV0108ESA-5SR#B0 R1LV0108ESA-5SR#S0		-0℃ ～70℃			
			R1LV0108ESA-7SI#B0 R1LV0108ESA-7SI#S0	70ns	-40℃ ～85℃			
			R1LV0108ESA-7SR#B0 R1LV0108ESA-7SR#S0		0℃ ～70℃			
	2Mb 3V	x8	R1LV0208BSA-5SI#B0 R1LV0208BSA-5SI#S0	55ns	-40℃ ～85℃	R1LV0208BSA-5SI#B1 R1LV0208BSA-5SI#S1	55ns	-40℃ ～85℃
			R1LV0208BSA-7SI#B0 R1LV0208BSA-7SI#S0	70ns				
32pin-TSOP(II)	4Mb 5V	x8	R1LP0408DSB-5SI#B0 R1LP0408DSB-5SI#S0	55ns	-40℃ ～85℃	R1LP0408DSB-5SI#B1 R1LP0408DSB-5SI#S1	55ns	-40℃ ～85℃
			R1LP0408DSB-5SR#B0 R1LP0408DSB-5SR#S0		-0℃ ～70℃			
			R1LP0408DSB-7SI#B0 R1LP0408DSB-7SI#S0	70ns	-40℃ ～85℃			
			R1LP0408DSB-7SR#B0 R1LP0408DSB-7SR#S0		0℃ ～70℃			
44pin-TSOP(II)	2Mb 3V	x16	R1LV0216BSB-5SI#B0 R1LV0216BSB-5SI#S0	55ns	-40℃ ～85℃	R1LV0216BSB-5SI#B1 R1LV0216BSB-5SI#S1	55ns	-40℃ ～85℃
			R1LV0216BSB-7SI#B0 R1LV0216BSB-7SI#S0	70ns				

- #B0: Tray packing, #S0: Tape & Reel packing. #B1: Tray packing, #S1: Tape & Reel packing.

© 2016 Renesas Electronics Corporation. All rights reserved.

4. Electrical characteristics (DC/AC) (for 256Kb ~ 4Mb Low Power SRAM)

- Regarding the EOL of "-5SR, -7SI, -7SR" products, electrical characteristics (DC/AC) of unified "-5SI" product is completely upper-compatible with "- "-5SR, -7SI, -7SR" products (see below).

(1)–a. Electrical characteristics (DC) : 256Kb(5V) R1LP5256ESA

Products

Item	**Pre Change**	**Post Change**
Orderable part name	R1LP5256ESA-5SI, -5SR, -7SI, -7SR#B0	R1LP5256ESA-5SI#B1
	R1LP5256ESA-5SI, -5SR, -7SI, -7SR#S0	R1LP5256ESA-5SI#S1

DC conditions

Item	Symbol	**Pre Change**		Symbol	**Post Change**
Supply voltage	Vcc	4.5V～5.5V		Vcc	←
Operating temperature range	Ta	5SR, 7SR	0℃ to 70℃	Ta	-40℃ to 85℃
		5SI, 7SI	-40℃ to 85℃		
Input high voltage	VIH	2.2V(min.) / Vcc+0.3V(max.)		VIH	←
Input low voltage	VIL	-0.3V(min.) / 0.8V(max.)		VIL	←

DC characteristics

Item	Symbol	**Pre Change**		Symbol	**Post Change**	
Operating Current	Icc1(TTL, Min.Cycle)	35mA(max.) / 25mA(typ.)		Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	4mA(max.) / 2mA(typ.)		Icc2(MOS, Cycle=1us)	←	
Standby current	ISB(TTL)	3mA(max.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Output high voltage	VOH	IOH=-1mA	2.4V(min.)	VOH	IOH=-1mA	←
	VOH2	IOH=-0.1mA	Vcc-0.5V(min.)	VOH2	IOH=-0.1mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	**Pre Change**	Symbol	**Post Change**
Input capacitance	C in	6pF(max.)	C in	←
Input/Output capacitance	C I/O	8pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	**Pre Change**		Symbol	**Post Change**	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	～25℃	2uA(max.) / 0.6uA(typ.)	IccDR(Vcc=3.0V)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

© 2016 Renesas Electronics Corporation. All rights reserved.

(1)–b. Electrical characteristics (AC) : 256Kb(5V) R1LP5256ESA

Products

Item	Pre Change	Post Change
Orderable part name	R1LP5256ESA-5SI, -5SR, -7SI, -7SR#B0	R1LP5256ESA-5SI#B1
	R1LP5256ESA-5SI, -5SR, -7SI, -7SR#S0	R1LP5256ESA-5SI#S1

AC characteristics

Read Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SI, 5SR	55ns(min.)	tRC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)
		7SI, 7SR	70ns(max.)		
Chip select access time	tACS	5SI, 5SR	55ns(max.)	tACS	55ns(max.)
		7SI, 7SR	70ns(max.)		
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)
		7SI, 7SR	35ns(max.)		
Output hold from address change	tOH	5SI, 5SR	10ns(min.)	tOH	←
		7SI, 7SR	10ns(min.)		
Chip select to output in low-Z	tCLZ	5SI, 5SR	5ns(min.)	tCLZ	←
		7SI, 7SR	5ns(min.)		
Output enable to output in low-Z	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←
		7SI, 7SR	5ns(min.)		
Chip deselect to output in high-Z	tCHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tCHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	50ns(min.)
		7SI, 7SR	65ns(min.)		
Chip select to end of write	tCW	5SI, 5SR	50ns(min.)	tCW	50ns(min.)
		7SI, 7SR	65ns(min.)		
Write pulse width	tWP	5SI, 5SR	40ns(min.)	tWP	40ns(min.)
		7SI, 7SR	50ns(min.)		
Address setup time	tAS	5SI, 5SR	0ns(min.)	tAS	←
		7SI, 7SR	0ns(min.)		
Write recovery time	tWR	5SI, 5SR	0ns(min.)	tWR	←
		7SI, 7SR	0ns(min.)		
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)
		7SI, 7SR	30ns(min.)		
Data hold from write time	tDH	5SI, 5SR	0ns(min.)	tDH	←
		7SI, 7SR	0ns(min.)		
Output enable from end of write	tOW	5SI, 5SR	5ns(min.)	tOW	←
		7SI, 7SR	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Write to output in high-Z	tWHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

© 2016 Renesas Electronics Corporation. All rights reserved.

(2)–a. Electrical characteristics (DC) : 256Kb(3V) R1LV5256ESA

Products

Item	Pre Change	Post Change
Orderable part name	R1LV5256ESA-5SI, -5SR, -7SI, -7SR#B0	R1LV5256ESA-5SI#B1
	R1LV5256ESA-5SI, -5SR, -7SI, -7SR#S0	R1LV5256ESA-5SI#S1

DC conditions

Item	Symbol	Pre Change		Symbol	Post Change
Supply voltage	Vcc	2.7V～3.6V		Vcc	←
Operating temperature range	Ta	5SR, 7SR	0°C to 70°C	Ta	-40°C to 85°C
		5SI, 7SI	-40°C to 85°C		
Input high voltage	VIH	2.0V(min.) / Vcc+0.3V(max.)		VIH	←
Input low voltage	VIL	-0.3V(min.) / 0.6V(max.)		VIL	←

DC characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Operating Current	Icc1(TTL, Min.Cycle)	25mA(max.) / 14mA(typ.)		Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	5mA(max.) / 2mA(typ.)		Icc2(MOS, Cycle=1us)	←	
Standby current	ISB(TTL)	0.33mA(max.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Output high voltage	VOH	IOH=-0.5mA	2.4V(min.)	VOH	IOH=-0.5mA	←
	VOH2	IOH=-0.05mA	Vcc-0.5V(min.)	VOH2	IOH=-0.05mA	←
Output low voltage	VOL	IOL=1mA	0.4V(max.)	VOL	IOL=1mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	6pF(max.)	C in	←
Input/Output capacitance	C I/O	8pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	～25℃	2uA(max.) / 0.6uA(typ.)	IccDR(Vcc=3.0V)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

© 2016 Renesas Electronics Corporation. All rights reserved.

(2)–b. Electrical characteristics (AC) : 256Kb(3V) R1LV5256ESA

Products

Item	Pre Change	Post Change
Orderable part name	R1LV5256ESA-5SI, -5SR, -7SI, -7SR#B0	R1LV5256ESA-5SI#B1
	R1LV5256ESA-5SI, -5SR, -7SI, -7SR#S0	R1LV5256ESA-5SI#S1

AC characteristics
Read Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SI, 5SR	55ns(min.)	tRC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)
		7SI, 7SR	70ns(max.)		
Chip select access time	tACS	5SI, 5SR	55ns(max.)	tACS	55ns(max.)
		7SI, 7SR	70ns(max.)		
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)
		7SI, 7SR	35ns(max.)		
Output hold from address change	tOH	5SI, 5SR	10ns(min.)	tOH	←
		7SI, 7SR	10ns(min.)		
Chip select to output in low-Z	tCLZ	5SI, 5SR	5ns(min.)	tCLZ	←
		7SI, 7SR	5ns(min.)		
Output enable to output in low-Z	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←
		7SI, 7SR	5ns(min.)		
Chip deselect to output in high-Z	tCHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tCHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	50ns(min.)
		7SI, 7SR	65ns(min.)		
Chip select to end of write	tCW	5SI, 5SR	50ns(min.)	tCW	50ns(min.)
		7SI, 7SR	65ns(min.)		
Write pulse width	tWP	5SI, 5SR	40ns(min.)	tWP	40ns(min.)
		7SI, 7SR	50ns(min.)		
Address setup time	tAS	5SI, 5SR	0ns(min.)	tAS	←
		7SI, 7SR	0ns(min.)		
Write recovery time	tWR	5SI, 5SR	0ns(min.)	tWR	←
		7SI, 7SR	0ns(min.)		
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)
		7SI, 7SR	30ns(min.)		
Data hold from write time	tDH	5SI, 5SR	0ns(min.)	tDH	←
		7SI, 7SR	0ns(min.)		
Output enable from end of write	tOW	5SI, 5SR	5ns(min.)	tOW	←
		7SI, 7SR	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Write to output in high-Z	tWHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

© 2016 Renesas Electronics Corporation. All rights reserved.

(3)–a. Electrical characteristics (DC) : 1Mb(5V) R1LP0108ESF, R1LP0108ESA

Products

Item	Pre Change	Post Change
Orderable part name	R1LP0108ESF-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESF-5SI#B1
	R1LP0108ESF-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESF-5SI#S1
	R1LP0108ESA-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESA-5SI#B1
	R1LP0108ESA-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESA-5SI#S1

DC conditions

Item	Symbol	Pre Change		Symbol	Post Change
Supply voltage	Vcc	4.5V～5.5V		Vcc	←
Operating temperature range	Ta	5SR, 7SR	0°C to 70°C	Ta	-40°C to 85°C
		5SI, 7SI	-40°C to 85°C		
Input high voltage	VIH	2.2V(min.) / Vcc+0.3V(max.)		VIH	←
Input low voltage	VIL	-0.3V(min.) / 0.8V(max.)		VIL	←

DC characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Operating Current	Icc1(TTL, Min.Cycle)	35mA(max.) / 25mA(typ.)		Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	5mA(max.) / 2mA(typ.)		Icc2(MOS, Cycle=1us)	←	
Standby current	ISB(TTL)	3mA(max.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Output high voltage	VOH	IOH=-1mA	2.4V(min.)	VOH	IOH=-1mA	←
	VOH2	IOH=-0.1mA	Vcc-0.5V(min.)	VOH2	IOH=-0.1mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	～25℃	2uA(max.) / 0.6uA(typ.)	IccDR(Vcc=3.0V)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

© 2016 Renesas Electronics Corporation. All rights reserved.

(3)–b. Electrical characteristics (AC) : 1Mb(5V) R1LP0108ESF, R1LP0108ESA

Products

Item	Pre Change	Post Change
Orderable part name	R1LP0108ESF-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESF-5SI#B1
	R1LP0108ESF-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESF-5SI#S1
	R1LP0108ESA-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESA-5SI#B1
	R1LP0108ESA-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESA-5SI#S1

AC characteristics
Read Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SI, 5SR	55ns(min.)	tRC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)
		7SI, 7SR	70ns(max.)		
Chip select access time	tACS1 / tACS2	5SI, 5SR	55ns(max.)	tACS1 / tACS2	55ns(max.)
		7SI, 7SR	70ns(max.)		
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)
		7SI, 7SR	35ns(max.)		
Output hold from address change	tOH	5SI, 5SR	5ns(min.)	tOH	5ns(min.)
		7SI, 7SR	10ns(min.)		
Chip select to output in low-Z	tCLZ1 / tCLZ2	5SI, 5SR	5ns(min.)	tCLZ1 / tCLZ2	5ns(min.)
		7SI, 7SR	10ns(min.)		
Output enable to output in low-Z	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←
		7SI, 7SR	5ns(min.)		
Chip deselect to output in high-Z	tCHZ1 / tCHZ2	5SI, 5SR	0ns(min.) / 20ns(max.)	tCHZ1 / tCHZ2	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	50ns(min.)
		7SI, 7SR	55ns(min.)		
Chip select to end of write	tCW	5SI, 5SR	50ns(min.)	tCW	50ns(min.)
		7SI, 7SR	55ns(min.)		
Write pulse width	tWP	5SI, 5SR	45ns(min.)	tWP	45ns(min.)
		7SI, 7SR	50ns(min.)		
Address setup time	tAS	5SI, 5SR	0ns(min.)	tAS	←
		7SI, 7SR	0ns(min.)		
Write recovery time	tWR	5SI, 5SR	0ns(min.)	tWR	←
		7SI, 7SR	0ns(min.)		
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)
		7SI, 7SR	30ns(min.)		
Data hold from write time	tDH	5SI, 5SR	0ns(min.)	tDH	←
		7SI, 7SR	0ns(min.)		
Output enable from end of write	tOW	5SI, 5SR	5ns(min.)	tOW	←
		7SI, 7SR	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Write to output in high-Z	tWHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

© 2016 Renesas Electronics Corporation. All rights reserved.

(4)–a. Electrical characteristics (DC) : 1Mb(3V) R1LV0108ESF, R1LV0108ESA

Products

Item	Pre Change	Post Change
Orderable part name	R1LV0108ESF-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESF-5SI#B1
	R1LV0108ESF-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESF-5SI#S1
	R1LV0108ESA-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESA-5SI#B1
	R1LV0108ESA-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESA-5SI#S1

DC conditions

Item	Symbol	Pre Change		Symbol	Post Change
Supply voltage	Vcc	2.7V～3.6V		Vcc	←
Operating temperature range	Ta	5SR, 7SR	0°C to 70°C	Ta	-40°C to 85°C
		5SI, 7SI	-40°C to 85°C		
Input high voltage	VIH	2.0V(min.) / Vcc+0.3V(max.)		VIH	←
Input low voltage	VIL	-0.3V(min.) / 0.6V(max.)		VIL	←

DC characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Operating Current	Icc1(TTL, Min.Cycle)	25mA(max.) / 15mA(typ.)		Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	5mA(max.) / 2mA(typ.)		Icc2(MOS, Cycle=1us)	←	
Standby current	ISB(TTL)	0.33mA(max.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Output high voltage	VOH	IOH=-0.5mA	2.4V(min.)	VOH	IOH=-0.5mA	←
	VOH2	IOH=-0.05mA	Vcc-0.5V(min.)	VOH2	IOH=-0.05mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	～25℃	2uA(max.) / 0.6uA(typ.)	IccDR(Vcc=3.0V)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

© 2016 Renesas Electronics Corporation. All rights reserved.

(4)–b. Electrical characteristics (AC) : 1Mb(3V) R1LV0108ESF, R1LV0108ESA

Products

Item	Pre Change	Post Change
Orderable part name	R1LV0108ESF-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESF-5SI#B1
	R1LV0108ESF-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESF-5SI#S1
	R1LV0108ESA-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESA-5SI#B1
	R1LV0108ESA-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESA-5SI#S1

AC characteristics
Read Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SI, 5SR	55ns(min.)	tRC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)
		7SI, 7SR	70ns(max.)		
Chip select access time	tACS1 / tACS2	5SI, 5SR	55ns(max.)	tACS1 / tACS2	55ns(max.)
		7SI, 7SR	70ns(max.)		
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)
		7SI, 7SR	35ns(max.)		
Output hold from address change	tOH	5SI, 5SR	5ns(min.)	tOH	5ns(min.)
		7SI, 7SR	10ns(min.)		
Chip select to output in low-Z	tCLZ1 / tCLZ2	5SI, 5SR	5ns(min.)	tCLZ1 / tCLZ2	5ns(min.)
		7SI, 7SR	10ns(min.)		
Output enable to output in low-Z	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←
		7SI, 7SR	5ns(min.)		
Chip deselect to output in high-Z	tCHZ1 / tCHZ2	5SI, 5SR	0ns(min.) / 20ns(max.)	tCHZ1 / tCHZ2	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	50ns(min.)
		7SI, 7SR	55ns(min.)		
Chip select to end of write	tCW	5SI, 5SR	50ns(min.)	tCW	50ns(min.)
		7SI, 7SR	55ns(min.)		
Write pulse width	tWP	5SI, 5SR	45ns(min.)	tWP	45ns(min.)
		7SI, 7SR	50ns(min.)		
Address setup time	tAS	5SI, 5SR	0ns(min.)	tAS	←
		7SI, 7SR	0ns(min.)		
Write recovery time	tWR	5SI, 5SR	0ns(min.)	tWR	←
		7SI, 7SR	0ns(min.)		
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)
		7SI, 7SR	30ns(min.)		
Data hold from write time	tDH	5SI, 5SR	0ns(min.)	tDH	←
		7SI, 7SR	0ns(min.)		
Output enable from end of write	tOW	5SI, 5SR	5ns(min.)	tOW	←
		7SI, 7SR	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Write to output in high-Z	tWHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

© 2016 Renesas Electronics Corporation. All rights reserved.

(5)–a. Electrical characteristics (DC) : 2Mb(3V) x8 R1LV0208BSA

Products

Item	Pre Change	Post Change
Orderable part name	R1LV0208BSA-5SI, -7SI#B0	R1LV0208BSA-5SI#B1
	R1LV0208BSA-5SI, -7SI#S0	R1LV0208BSA-5SI#S1

DC conditions

Item	Symbol	Pre Change	Symbol	Post Change
Supply voltage	Vcc	2.7V～3.6V	Vcc	←
Operating temperature range	Ta	-40°C to 85°C	Ta	←
Input high voltage	VIH	2.0V(min.) / Vcc+0.3V(max.)	VIH	←
Input low voltage	VIL	-0.3V(min.) / 0.6V(max.)	VIL	←

DC characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Operating Current	Icc1(TTL, Min.Cycle)	25mA(max.) / 15mA(typ.)		Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	5mA(max.) / 2mA(typ.)		Icc2(MOS, Cycle=1us)	←	
Standby current	ISB(TTL)	0.33mA(max.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	2uA(max.) / 1uA(typ.)	ISB1(MOS)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃	10uA(max.)		～85℃	←
Output high voltage	VOH	IOH=-0.5mA	2.4V(min.)	VOH	IOH=-0.5mA	←
	VOH2	IOH=-0.05mA	Vcc-0.5V(min.)	VOH2	IOH=-0.05mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	～25℃	2uA(max.) / 1uA(typ.)	IccDR(Vcc=3.0V)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃	10uA(max.)		～85℃	←
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

© 2016 Renesas Electronics Corporation. All rights reserved.

(5)–b. Electrical characteristics (AC) : 2Mb(3V) x8 R1LV0208BSA

Products

Item	Pre Change	Post Change
Orderable part name	R1LV0208BSA-5SI, -7SI#B0	R1LV0208BSA-5SI#B1
	R1LV0208BSA-5SI, -7SI#S0	R1LV0208BSA-5SI#S1

AC characteristics

Read Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SI	55ns(min.)	tRC	55ns(min.)
		7SI	70ns(min.)		
Address access time	tAA	5SI	55ns(max.)	tAA	55ns(max.)
		7SI	70ns(max.)		
Chip select access time	tACS1 / tACS2	5SI	55ns(max.)	tACS1 / tACS2	55ns(max.)
		7SI	70ns(max.)		
Output enable to output valid	tOE	5SI	30ns(max.)	tOE	30ns(max.)
		7SI	35ns(max.)		
Output hold from address change	tOH	5SI	10ns(min.)	tOH	←
		7SI	10ns(min.)		
Chip select to output in low-Z	tCLZ1 / tCLZ2	5SI	10ns(min.)	tCLZ1 / tCLZ2	←
		7SI	10ns(min.)		
Output enable to output in low-Z	tOLZ	5SI	5ns(min.)	tOLZ	←
		7SI	5ns(min.)		
Chip deselect to output in high-Z	tCHZ1 / tCHZ2	5SI	0ns(min.) / 20ns(max.)	tCHZ1 / tCHZ2	0ns(min.) / 20ns(max.)
		7SI	0ns(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SI	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI	0ns(min.) / 25ns(max.)		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Write cycle time	tWC	5SI	55ns(min.)	tWC	55ns(min.)
		7SI	70ns(min.)		
Address valid to end of write	tAW	5SI	50ns(min.)	tAW	50ns(min.)
		7SI	55ns(min.)		
Chip select to end of write	tCW	5SI	50ns(min.)	tCW	50ns(min.)
		7SI	55ns(min.)		
Write pulse width	tWP	5SI	45ns(min.)	tWP	45ns(min.)
		7SI	50ns(min.)		
Address setup time	tAS	5SI	0ns(min.)	tAS	←
		7SI	0ns(min.)		
Write recovery time	tWR	5SI	0ns(min.)	tWR	←
		7SI	0ns(min.)		
Data to write time overlap	tDW	5SI	25ns(min.)	tDW	25ns(min.)
		7SI	30ns(min.)		
Data hold from write time	tDH	5SI	0ns(min.)	tDH	←
		7SI	0ns(min.)		
Output enable from end of write	tOW	5SI	5ns(min.)	tOW	←
		7SI	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SI	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI	0ns(min.) / 25ns(max.)		
Write to output in high-Z	tWHZ	5SI	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)
		7SI	0ns(min.) / 25ns(max.)		

© 2016 Renesas Electronics Corporation. All rights reserved.

(6)–a. Electrical characteristics (DC) : 4Mb(5V) x8 R1LP0408DSB

Products

Item	Pre Change	Post Change
Orderable part name	R1LP0408DSB-5SI, -5SR, -7SI, -7SR#B0	R1LP0408DSB-5SI#B1
	R1LP0408DSB-5SI, -5SR, -7SI, -7SR#S0	R1LP0408DSB-5SI#S1

DC conditions

Item	Symbol	Pre Change		Symbol	Post Change
Supply voltage	Vcc	4.5V～5.5V		Vcc	←
Operating temperature range	Ta	5SR, 7SR	0°C to 70°C	Ta	-40°C to 85°C
		5SI, 7SI	-40°C to 85°C		
Input high voltage	VIH	2.2V(min.) / Vcc+0.3V(max.)		VIH	←
Input low voltage	VIL	-0.3V(min.) / 0.8V(max.)		VIL	←

DC characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Operating Current	Icc(TTL)	10mA(max.) / 5mA(typ.)		Icc(TTL)	←	
	Icc1(TTL, Min.Cycle)	25mA(max.) / 15mA(typ.)		Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	5mA(max.) / 3mA(typ.)		Icc2(MOS, Cycle=1us)	←	
Standby current	ISB(TTL)	0.5mA(max.) / 0.1mA(typ.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	2.5uA(max.) / 0.8uA(typ.)	ISB1(MOS)	～25℃	←
		～40℃	3uA(max.) / 1uA(typ.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Output high voltage	VOH	IOH=-1mA	2.4V(min.)	VOH	IOH=-1mA	←
	VOH2	IOH=-0.1mA	Vcc-0.5V(min.)	VOH2	IOH=-0.1mA	←
Output low voltage	VOL	IOL=2.1mA	0.4V(max.)	VOL	IOL=2.1mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	～25℃	2.5uA(max.) / 0.8uA(typ.)	IccDR(Vcc=3.0V)	～25℃	←
		～40℃	3uA(max.) / 1uA(typ.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

© 2016 Renesas Electronics Corporation. All rights reserved.

(6)–b. Electrical characteristics (AC) : 4Mb(5V) x8 R1LP0408DSB

Products

Item	Pre Change	Post Change
Orderable part name	R1LP0408DSB-5SI, -5SR, -7SI, -7SR#B0	R1LP0408DSB-5SI#B1
	R1LP0408DSB-5SI, -5SR, -7SI, -7SR#S0	R1LP0408DSB-5SI#S1

AC characteristics
Read Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SI, 5SR	55ns(min.)	tRC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)
		7SI, 7SR	70ns(max.)		
Chip select access time	tACS	5SI, 5SR	55ns(max.)	tACS	55ns(max.)
		7SI, 7SR	70ns(max.)		
Output enable to output valid	tOE	5SI, 5SR	25ns(max.)	tOE	25ns(max.)
		7SI, 7SR	35ns(max.)		
Chip select to output in low-Z	tCLZ	5SI, 5SR	10ns(min.)	tCLZ	←
		7SI, 7SR	10ns(min.)		
Output enable to output in low-Z	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←
		7SI, 7SR	5ns(min.)		
Chip deselect to output in high-Z	tCHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tCHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Output hold from address change	tOH	5SI, 5SR	10ns(min.)	tOH	←
		7SI, 7SR	10ns(min.)		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Chip select to end of write	tCW	5SI, 5SR	50ns(min.)	tCW	50ns(min.)
		7SI, 7SR	60ns(min.)		
Address setup time	tAS	5SI, 5SR	0ns(min.)	tAS	←
		7SI, 7SR	0ns(min.)		
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	50ns(min.)
		7SI, 7SR	60ns(min.)		
Write pulse width	tWP	5SI, 5SR	40ns(min.)	tWP	40ns(min.)
		7SI, 7SR	50ns(min.)		
Write recovery time	tWR	5SI, 5SR	0ns(min.)	tWR	←
		7SI, 7SR	0ns(min.)		
Write to output in high-Z	tWHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)
		7SI, 7SR	30ns(min.)		
Data hold from write time	tDH	5SI, 5SR	0ns(min.)	tDH	←
		7SI, 7SR	0ns(min.)		
Output enable from end of write	tOW	5SI, 5SR	5ns(min.)	tOW	←
		7SI, 7SR	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

© 2016 Renesas Electronics Corporation. All rights reserved.

(7)–a. Electrical characteristics (DC) : 2Mb(3V) x16 R1LV0216BSB

Products

Item	Pre Change	Post Change
Orderable part name	R1LV0216BSB-5SI, -7SI#B0	R1LV0216BSB-5SI#B1
	R1LV0216BSB-5SI, -7SI#S0	R1LV0216BSB-5SI#S1

DC conditions

Item	Symbol	Pre Change	Symbol	Post Change
Supply voltage	Vcc	2.7V～3.6V	Vcc	←
Operating temperature range	Ta	-40°C to 85°C	Ta	←
Input high voltage	VIH	2.2V(min.) / Vcc+0.3V(max.)	VIH	←
Input low voltage	VIL	-0.3V(min.) / 0.6V(max.)	VIL	←

DC characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Operating Current	Icc1(TTL, Min.Cycle)	25mA(max.) / 15mA(typ.)		Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	5mA(max.) / 2mA(typ.)		Icc2(MOS, Cycle=1us)	←	
Standby current	ISB(TTL)	0.5mA(max.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	2uA(max.) / 1uA(typ.)	ISB1(MOS)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃	10uA(max.)		～85℃	←
Output high voltage	VOH	IOH=-0.5mA	2.4V(min.)	VOH	IOH=-0.5mA	←
	VOH2	IOH=-0.05mA	Vcc-0.5V(min.)	VOH2	IOH=-0.05mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	～25℃	2uA(max.) / 1uA(typ.)	IccDR(Vcc=3.0V)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃	10uA(max.)		～85℃	←
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

© 2016 Renesas Electronics Corporation. All rights reserved.

(7)–b. Electrical characteristics (AC) : 2Mb(3V) x16 R1LV0216BSB

Products

Item	Pre Change	Post Change
Orderable part name	R1LV0216BSB-5SI, -7SI#B0	R1LV0216BSB-5SI#B1
	R1LV0216BSB-5SI, -7SI#S0	R1LV0216BSB-5SI#S1

AC characteristics

Read Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SI	55ns(min.)	tRC	55ns(min.)
		7SI	70ns(min.)		
Address access time	tAA	5SI	55ns(max.)	tAA	55ns(max.)
		7SI	70ns(max.)		
Chip select access time	tACS	5SI	55ns(max.)	tACS	55ns(max.)
		7SI	70ns(max.)		
Output enable to output valid	tOE	5SI	30ns(max.)	tOE	30ns(max.)
		7SI	35ns(max.)		
Output hold from address change	tOH	5SI	10ns(min.)	tOH	←
		7SI	10ns(min.)		
LB#,UB# access time	tBA	5SI	55ns(max.)	tBA	55ns(max.)
		7SI	70ns(max.)		
Chip select to output in low-Z	tCLZ	5SI	10ns(min.)	tCLZ	←
		7SI	10ns(min.)		
LB#,UB# enable to low-Z	tBLZ	5SI	10ns(min.)	tBLZ	←
		7SI	10ns(min.)		
Output enable to output in low-Z	tOLZ	5SI	5ns(min.)	tOLZ	←
		7SI	5ns(min.)		
Chip deselect to output in high-Z	tCHZ	5SI	0ns(min.) / 20ns(max.)	tCHZ	0ns(min.) / 20ns(max.)
		7SI	0ns(min.) / 25ns(max.)		
LB#,UB# disable to high-Z	tBHZ	5SI	0ns(min.) / 20ns(max.)	tBHZ	0ns(min.) / 20ns(max.)
		7SI	0ns(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SI	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI	0ns(min.) / 25ns(max.)		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Write cycle time	tWC	5SI	55ns(min.)	tWC	55ns(min.)
		7SI	70ns(min.)		
Address valid to end of write	tAW	5SI	50ns(min.)	tAW	50ns(min.)
		7SI	55ns(min.)		
Chip select to end of write	tCW	5SI	50ns(min.)	tCW	50ns(min.)
		7SI	55ns(min.)		
Write pulse width	tWP	5SI	45ns(min.)	tWP	45ns(min.)
		7SI	50ns(min.)		
LB#,UB# valid to end of write	tBW	5SI	50ns(min.)	tBW	50ns(min.)
		7SI	55ns(min.)		
Address setup time	tAS	5SI	0ns(min.)	tAS	←
		7SI	0ns(min.)		
Write recovery time	tWR	5SI	0ns(min.)	tWR	←
		7SI	0ns(min.)		
Data to write time overlap	tDW	5SI	25ns(min.)	tDW	25ns(min.)
		7SI	30ns(min.)		
Data hold from write time	tDH	5SI	0ns(min.)	tDH	←
		7SI	0ns(min.)		
Output enable from end of write	tOW	5SI	5ns(min.)	tOW	←
		7SI	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SI	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI	0ns(min.) / 25ns(max.)		
Write to output in high-Z	tWHZ	5SI	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)
		7SI	0ns(min.) / 25ns(max.)		

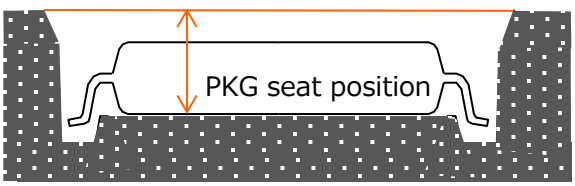
© 2016 Renesas Electronics Corporation. All rights reserved.

5. Packing specification

(1) Change the specification of the JEDEC tray

- The package seat position in tray pocket is to be changed (see below).
- No change in outline dimensions and pocket pitch for JEDEC tray.

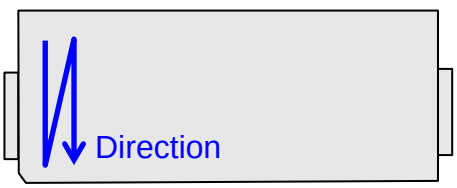
	Package type	Pre Change		Post Change	
		Tray type name	PKG seat position (mm)	Tray type name	PKG seat position (mm)
JEDEC tray	28pin-TSOP(I), 32pin-sTSOP	L196-10	2.0	EA50813	1.85
	32pin-TSOP(I)	L196-20	2.1	EA50820	1.5
	32pin-TSOP(II)	L196-93	2.0	EA80817	2.0
	44pin-TSOP(II)	L196-92	2.0	EA80815	2.0
	48pin-TSOP(I)	L196-126	2.0	EA51220	1.5



Cross section of tray pocket

(2) Laying direction of ICs on a tray

- Regarding R1RP0416DSB, R1RW0416DSB and R1LV1616HSA, laying direction of ICs on a tray is to be changed (see below).
- No change in other products, because the direction is already same as the "Post Change“ as shown below.

	Pre Change	Post Change
Laying direction of ICs on a tray		
Orderable part name	R1RP0416DSB-xxx #D0 R1RW0416DSB-xxx #D0 R1LV1616HSA-xxx #B0	R1RP0416DSB-xxx #D1 R1RW0416DSB-xxx #D1 R1LV1616HSA-xxx #B1

© 2016 Renesas Electronics Corporation. All rights reserved.

(3) Change the specification of the Tape & Reel

- The package seat position in taping pocket is to be changed (see below).
- No change in width and pitch of embossed carrier tape.
- No change in reel diameter.

	Package type	Pre Change		Post Change	
		Emboss type name	PKG seat position (mm)	Emboss type name	PKG seat position (mm)
Embossed carrier tape	28pin-TSOP(I), 32pin-sTSOP	MTE2412H-28P2C-A	1.3	TSOP28	1.4
	32pin-TSOP(I)	MTE3212H-32P3H-A	1.25	TSOP32-1	1.4
	32pin-TSOP(II)	MTE3216H-50P3W	1.2	TSOP32-6	1.3
	44pin-TSOP(II)	MTE3216H-28P3Y	1.2	TSOP44-3	1.3
	48pin-TSOP(I)	TE3216-16P	1.2	TSOP48-3	1.2

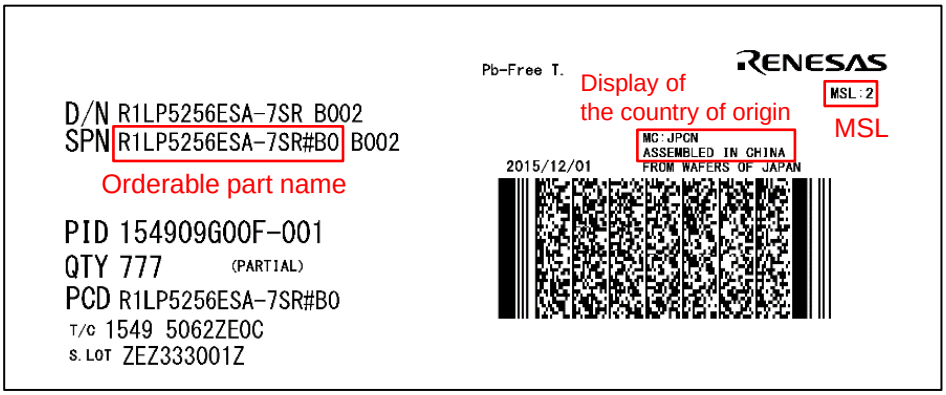
Cross section of taping pocket

© 2016 Renesas Electronics Corporation. All rights reserved.

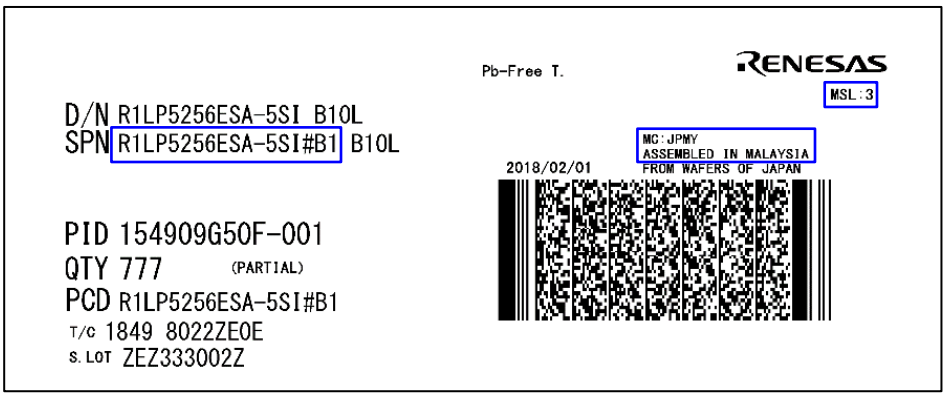
6. Shipping label

- Label format itself is not changed.
- Written specifications: "Orderable part name", "the country of origin" and MSL are changed.
  See below for example.
  (Note: Regarding R1LV0216BSB and R1LP0408DSB, no change in MSL.)

Pre Change



Post Change



7. Site information

Item	Assembly Site	Final Test Site
Company name	Amkor Technology Malaysia Sdn,Bhd.	Powertech Technology Inc.
Country name	Malaysia	Taiwan
Company address	15km, Jalan Klang-Banting, 42507 Telok Panglima Garang, Kuala Langat, Selangor Darul Ehsan, Malaysia	No.10, Datong Rd., Hsinchu Industrial Park, Hukou, Hsinchu 30352, Taiwan

© 2016 Renesas Electronics Corporation. All rights reserved.