RENESAS

PCN# : [EPPO3-EX-26-0002]

Product Change Notice (PCN)

Subject: Wafer-fabrication factory addition for RL78/F25 products
Publication Date: 2/2/2026
Effective Date: 8/13/2026

Revision Description: Initial release

Description of Change: Wafer-process, Wafer-test, and BG (back-grind) fabs are added (parallel production)

	After Fab addition		Current MP
WP	Kawashiri	PSMC	Kawashiri
WT	Kawashiri	Ardentec	Kawashiri
BG	Kawashiri	KL	Kawashiri
Assembly	KL		KL
Sort	KL		KL

"Kawashiri" means Kawashiri Factory, Renesas Semiconductor Manufacturing Co., Ltd.
"KL" means Renesas Semiconductor KL Sdn. Bhd.
"Ardentec" means Ardentec Corporation
"PSMC" means Powerchip Semiconductor Manufacturing Corporation

Affected Product List:

R7F125FPL3AFB-C#BA0	R7F125FML3AFB-C#BA0	R7F125FLL3AFB-C#BA0	R7F125FGL3AFB-C#BA0
R7F125FPL3AFB-C#UA0	R7F125FML3AFB-C#UA0	R7F125FLL3AFB-C#UA0	R7F125FGL3AFB-C#UA0
R7F125FPL3AFB-C#HA0	R7F125FML3AFB-C#HA0	R7F125FLL3AFB-C#HA0	R7F125FGL3AFB-C#HA0
R7F125FPL4AFB-C#BA0	R7F125FML4AFB-C#BA0	R7F125FLL4AFB-C#BA0	R7F125FGL4AFB-C#BA0
R7F125FPL4AFB-C#UA0	R7F125FML4AFB-C#UA0	R7F125FLL4AFB-C#UA0	R7F125FGL4AFB-C#UA0
R7F125FPL4AFB-C#HA0	R7F125FML4AFB-C#HA0	R7F125FLL4AFB-C#HA0	R7F125FGL4AFB-C#HA0

Reason for Change:
Stable production supply for RL78/F25

Impact on Fit, Form, Function, Quality & Reliability:
No impact.

Product Identification:
Enable via the production history data through the packing label or of the trace code.

Qualification Status: Appendix-3 shows "Q100 Qualification Test Results"

Sample Availability Date: 3/31/2026
Sample shipment will begin subsequentially on 3/31/2026

Device Material Declaration: Available upon request.

Note:

1. Acknowledgement must be received by Renesas within 30 days or Renesas will consider the change as approved.

2. If timely acknowledgement is provided by Customer, then Customer shall have 90 days from the date of receipt of this PCN to make any objections to this PCN. If Customer fails to make objections to this PCN within 90 days of the receipt of the PCN then Renesas will consider the PCN changes as approved.

3. If customer cannot accept the PCN then customer must provide Renesas with a last time buy demand and purchase order.

For additional information regarding this notice, please contact your Renesas sales representative.

Appendix-1

■4M changing points

Full chip-design compatible wafer-fabrication-process was ported from Kawashiri factory.

Item	Check Result	Judgement
Machine	Sufficiently compatible to produce the equivalent wafer-level structure and electrical characteristics	**No risk**
Method	Sufficiently compatible to produce the equivalent wafer-level structure and electrical characteristics	**No risk**
Man	Using operator certification system. Only certificated operator can work for the production.	**No risk**
Material	Sufficiently compatible to produce the equivalent wafer-level structure and electrical characteristics	**No risk**

Appendix-2

Q100 Qualification Test Results

Report No. MCR-25-0467
Date: Dec./ 24/ 2025

RENESAS SEMICONDUCTOR

RELIABILITY REPORT

SERIES : RL78/F25

DEVICE : Please see [Device list]

APPLICATION : Automobile

Quality Assurance Div.
Renesas Electronics Corporation

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(Rev.5.0-2 October 2020)

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Q100 Qualification Test Results

[Note : Basically qualification tests were performed using a representative product with the same wafer process and the same package structure .]

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results (Fail of Total)	Comments: (N/A =Not Applicable)
TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS								
PC	A1	JESD22 A113 J-STD-020	Preconditioning: (Test @ Rm) SMD only; Moisture Preconditioning for THB/HAST, AC/UHST, TC ; Peak Reflow Temp=260°C	Min.MSL=3			MSL=3	-
~~THB~~ ~~or~~ HAST	A2	JESD22 A101	Temperature Humidity Bias: (Test @ Rm/Hot) Ta=110°C, RH=85%, t=264hrs	3	77	231	0 of 231	-
~~AC or~~ UHST ~~or TH~~	A3	JESD22 A118	Unbiased Highly Accelerated Stress Test: (Test @ Rm) Ta=110°C, RH=85%, t=264hrs	3	77	231	0 of 231	-
TC	A4	JESD22 A104	Temperature Cycle: (Test@Hot) Ta=-55°C to 150°C, t=1000cyc Wire Bond Pull: (0 Fails after TC)	3	77	231	0 of 231	-
PTC	A5	JESD22 A105	Power Temperature Cycle: (Test @ Rm/Hot) -	-	-	-	-	N/A
HTSL	A6	JESD22 A103	High Temp Storage Life: (Test@Rm/Hot) Ta=175°C, t=500hrs	1	45	45	0 of 45	-
TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS								
HTOL	B1	JESD22 A108	High Temp Operating Life: (Test @ Rm/Hot/Cold) Ta=125°C, t=1000h	3	77	231	0 of 231	-
ELFR	B2	AEC-Q100-008	Early Life Failure Rate: (Test@Rm/Hot) Ta=125°C, t=48hrs	3	800	2400	0 of 2400	-
EDR	B3	AEC-Q100-005	NVM Endurance & Data Retention Test: (Test @ Rm/Hot) — For HTOL	3	77	231	0 of 231	-
			For HTSL	1	45	45	0 of 45	-

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Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results (Fail of Total)	Comments: (N/A =Not Applicable)
TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS								
WBS	C1	AEC-Q100-001 AEC-Q003	Wire Bond Shear Test: (Cpk > 1.67)	30 bonds	5 parts Min.	30 bonds	0 of 30 bonds	Ppk>1.67
WBP	C2	Mil-STD-883 Method 2011 AEC-Q003	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30 bonds	5 parts Min.	30 bonds	0 of 30 bonds	Ppk>1.67
SD	C3	JESD22 B102 JSTD-002D	Solderability: (>95% coverage) 8 hr steam aging prior to testing	1	15	15	0 of 15	-
PD	C4	JESD22 B100 JESD22 B108 AEC-Q003	Physical Dimensions: (Cpk > 1.67)	3	10	30	0 of 30	Ppk>1.67
SBS	C5	AEC-Q100-010 AEC-Q003	Solder Ball Shear: (Cpk > 1.67); 5 balls from min. of 10 devices	-	-	-	-	N/A
LI	C6	JESD22 B105	Lead Integrity: (No lead cracking or breaking); Through-hole only; 10 leads from each of 5 devices	-	-	-	-	N/A
TEST GROUP D – DIE FABRICATION RELIABILITY TESTS								
EM	D1	JESD61	Electromigration:	-	-	-	Pass	Confirmed by process TEG
TDDB	D2	JESD35	Time Dependent Dielectric Breakdown:	-	-	-	Pass	Confirmed by process TEG
HCI	D3	JESD60 & 28	Hot Carrier Injection:	-	-	-	Pass	Confirmed by process TEG
NBTI	D4	JESD90	Negative Bias Temperature Instability:	-	-	-	Pass	Confirmed by process TEG
SM	D5	JESD61,87 & 202	Stress Migration:	-	-	-	Pass	Confirmed by process TEG

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Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results (Fail of Total)	Comments: (N/A =Not Applicable)
TEST GROUP E- ELECTRICAL VERIFICATION								
TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test:	All	All	All	0 of All	-
HBM	E2	AEC-Q100-002	Electrostatic Discharge, Human Body Model: (Test @ Rm/Hot); (2KV HBM / Class 2 or better)	1	3	3	0 of 3 ESD Level=2	HBM>2KV
CDM	E3	AEC-Q100-011	Electrostatic Discharge, Charged Device Model: (Test @ Rm/Hot); (750V corner pins, 500V all other pins / Class C2A or better)	1	3	3	0 of 3 ESD Level=C2A	Corner pins: 750V Pass All other pins:500V Pass
LU	E4	AEC-Q100-004	Latch-Up: (Test @ Rm/Hot)	1	6	6	0 of 6	-
ED	E5	AEC-Q100-009 AEC-Q003	Electrical Distributions: (Test @ Rm/Hot/Cold) (CPk > 1.33, Ppk >1.67)	3	30	90	0 of 90	Ppk>1.67
FG	E6	AEC-Q100-007	Fault Grading:	-	-	-	98.00%	-
CHAR	E7	AEC-Q003	Characterization: (Test @ Rm/Hot/Cold)	-	-	-	Pass	According to Renesas standard procedure
EMC	E9	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	1	1	1	0 of 1	
SC	E10	AEC Q100-012	Short Circuit Characterization	-	-	-	-	N/A
SER	E11	JESD89-1 JESD89-2 JESD89-3	Soft Error Rate	-	-	-	-	N/A
LF	E12	AEC-Q005	Lead (Pb) Free: (see AEC-Q005)	-	-	-	Pass	Solderability: See SD (C3) result. Solder heat resistance: N/A (Wave Solder is Not recommended.) Whisker: Performed on product TEG with test method based on JESD201.

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Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results (Fail of Total)	Comments: (N/A =Not Applicable)
TEST GROUP F – DEFECT SCREENING TESTS								
PAT	F1	AEC-Q001	Process Average Testing: (see AEC-Q001)	All	All	All	Reject units outside PAT limits	Apply to mass production according to Renesas standard procedure
SBA	F2	AEC-Q002	Statistical Bin/Yield Analysis: (see AEC-Q002)	All	All	All	Reject units outside criteria	Apply to mass production according to Renesas standard procedure
TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS (for Ceramic Package testing only)								
MS	G1	JESD22 B104	Mechanical Shock: (Test @ Rm)	-	-	-	-	N/A
VFV	G2	JESD22 B103	Variable Frequency Vibration: (Test @ Rm)	-	-	-	-	N/A
CA	G3	MIL-STD-883 Method 2001	Constant Acceleration: (Test @ Rm)	-	-	-	-	N/A
GFL	G4	MIL-STD-883 Method 1014	Gross and Fine Leak:	-	-	-	-	N/A
DROP	G5	-----------------	Drop Test: (Test @ Rm) MEMS cavity parts only. Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface.	-	-	-	-	N/A
LT	G6	MIL-STD-883 Method 2004	Lid Torque:	-	-	-	-	N/A
DS	G7	MIL-STD-883 Method 2019	Die Shear:	-	-	-	-	N/A
IWV	G8	MIL-STD-883 Method 1018	Internal Water Vapor:	-	-	-	-	N/A

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Device List

[RL78/F25 series]

R7F125FPL4AFB-C		
R7F125FPL3AFB-C		
R7F125FML4AFB-C		
R7F125FML3AFB-C		
R7F125FLL4AFB-C		
R7F125FLL3AFB-C		
R7F125FGL4AFB-C		
R7F125FGL3AFB-C		

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