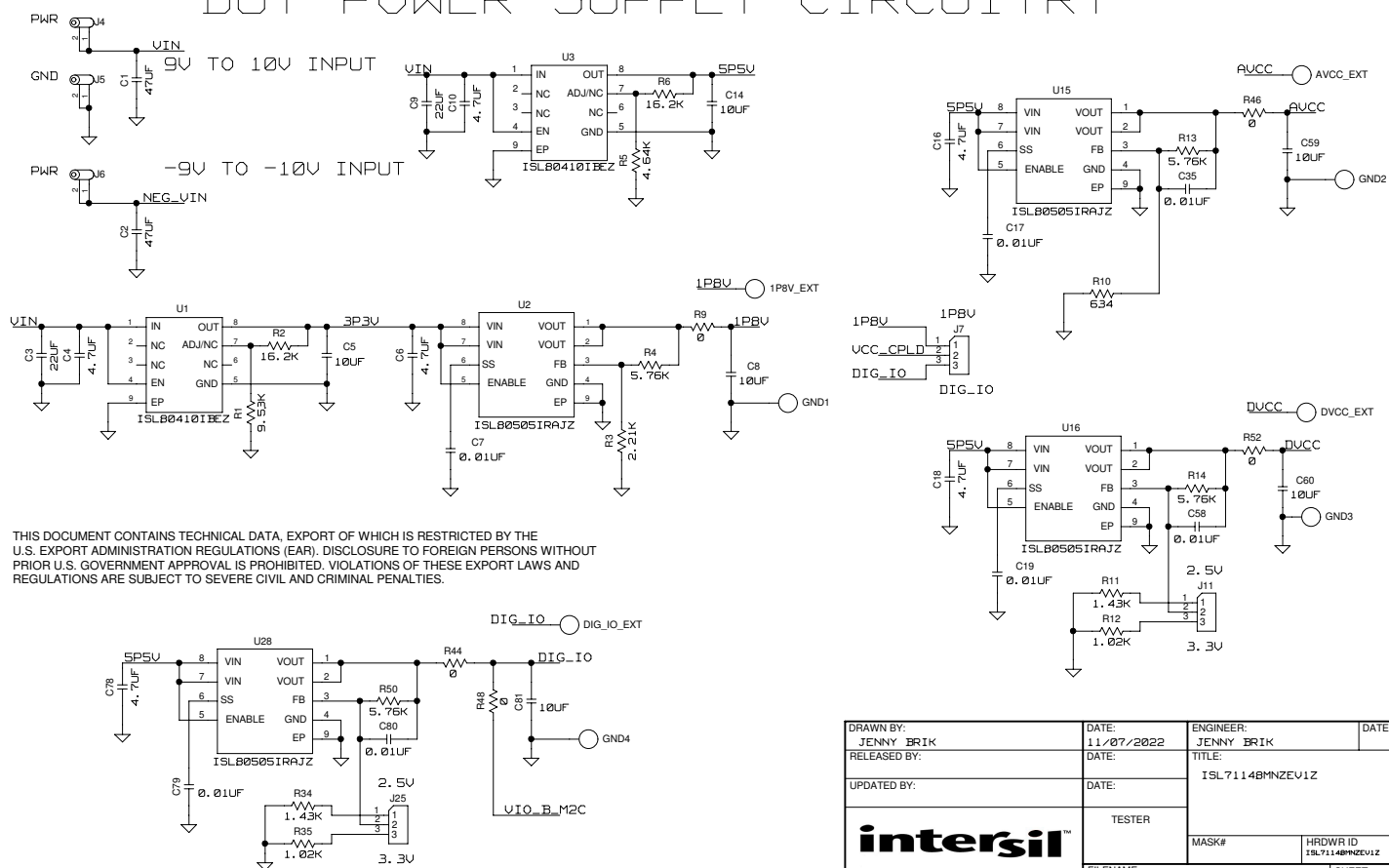



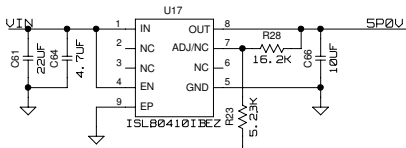
# DUT POWER SUPPLY CIRCUITRY



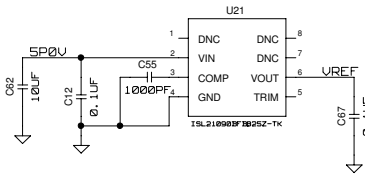
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DRAWN BY: JENNY BRIK		DATE: 11/07/2022		ENGINEER: JENNY BRIK		DATE:	
RELEASED BY:		DATE:		TITLE: ISL7114BMNZEUVZ			
UPDATED BY:		DATE:					
		TESTER		MASK#		HRDW ID ISL7114BMNZEUVZ	REV C
FILENAME: ISL7114BMNZEUVZC.ZIP						SHEET 1 OF 8	

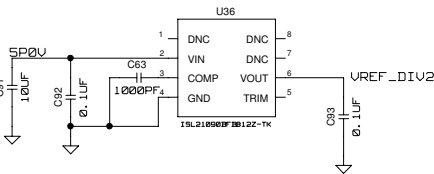
# AMP POWER SUPPLY AND VREF CIRCUITRY



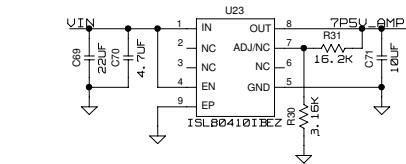
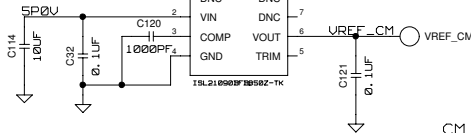
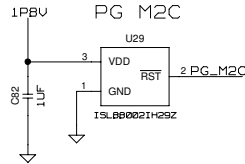
5.0V SUPPLY FOR REFERENCES



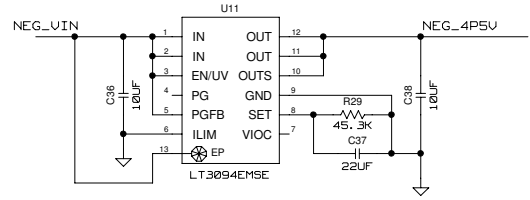
2.5V REFERENCE



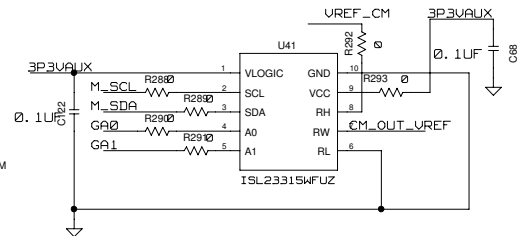
1.25V COMMON MODE



+7.5V/-4.5V SUPPLIES FOR AMPLIFIER CIRCUIT

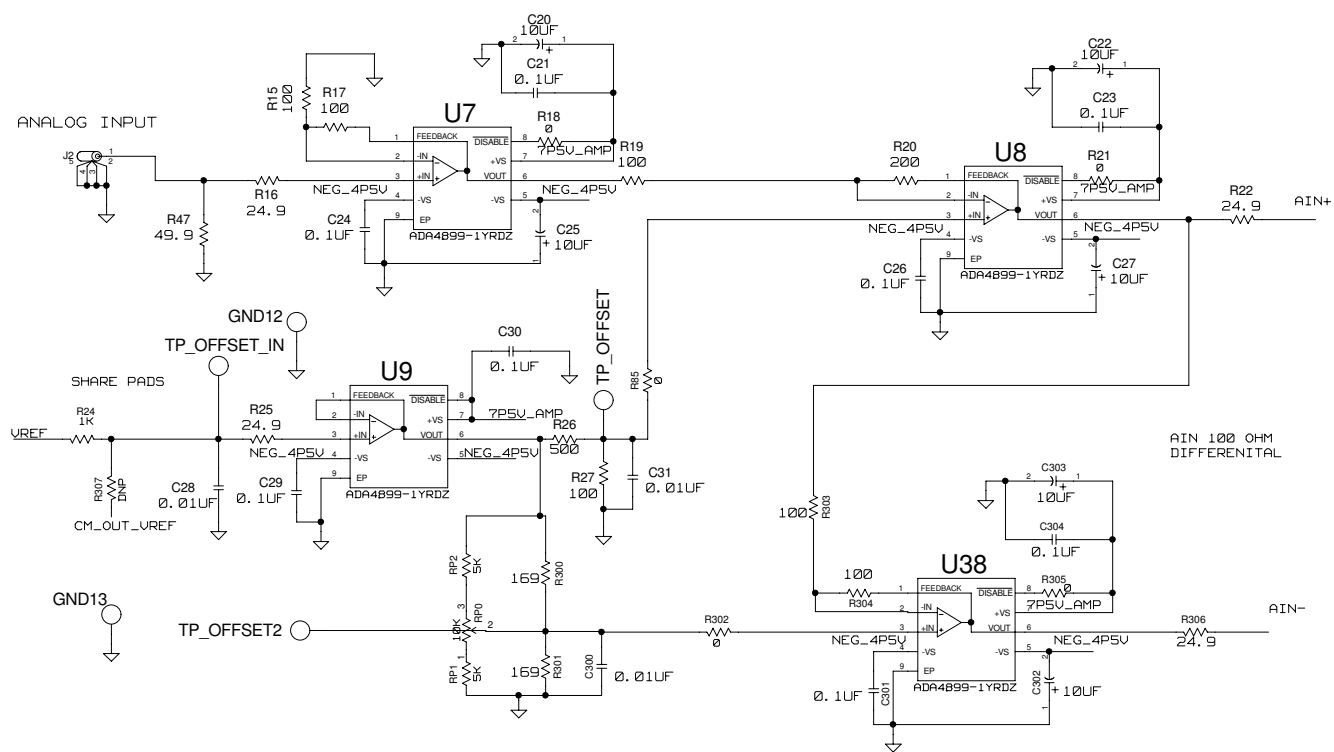


CM ADJUSTMENT



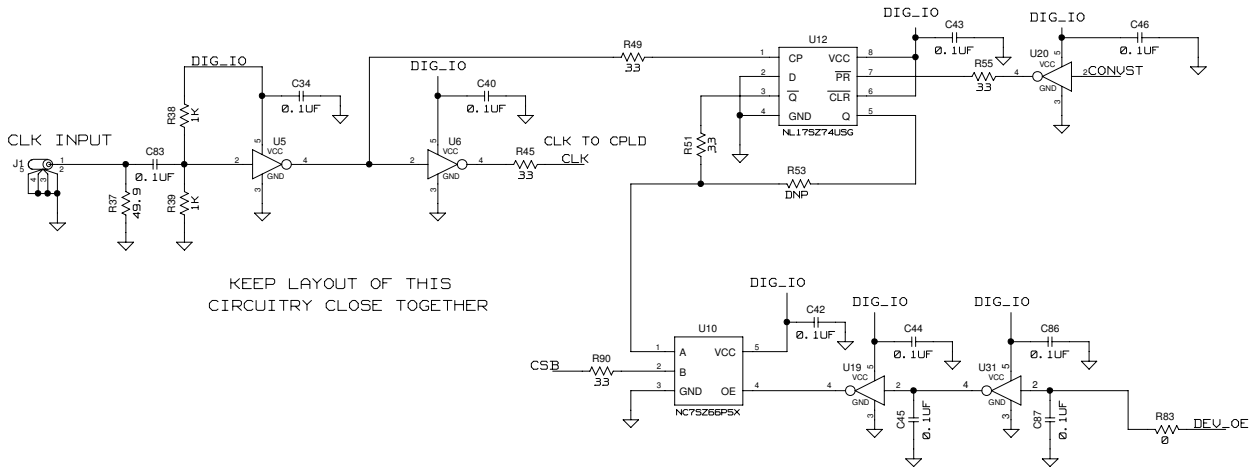
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# ANALOG INPUT AMPLIFIER CIRCUITRY



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# CLOCK CIRCUITRY



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# ADC INPUT CIRCUITRY

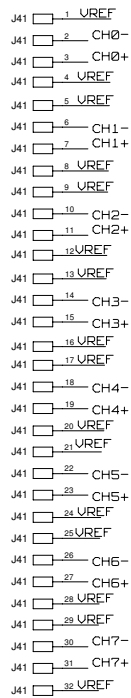
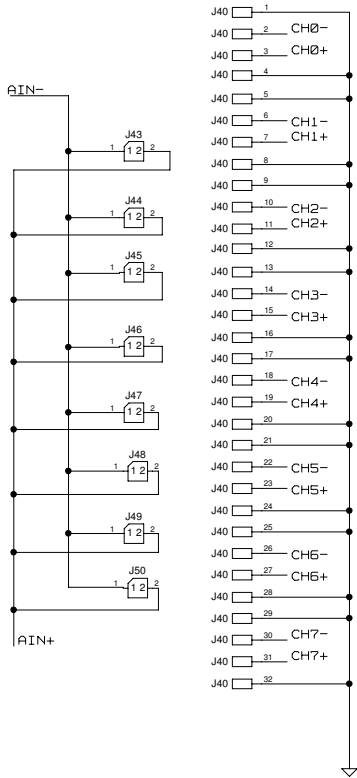
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PLACE HEADERS J40-J50 TOGETHER IN A BANK

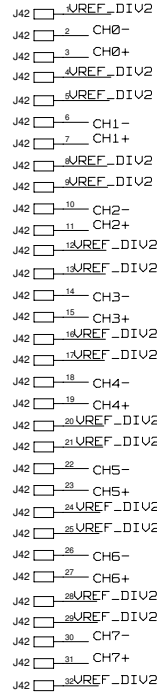
$V_{REF\_VREF}/2$

PLACE HEADER NEAR J40 AND  
CONNECT TO LARGE PLANES FOR  
GND,  $V_{REF}/2$  AND  $V_{REF}$

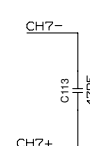
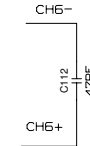
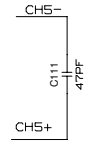
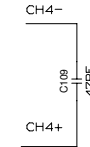
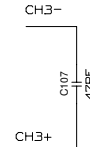
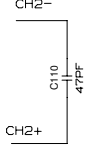
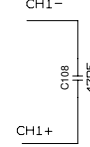
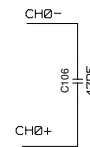
GND



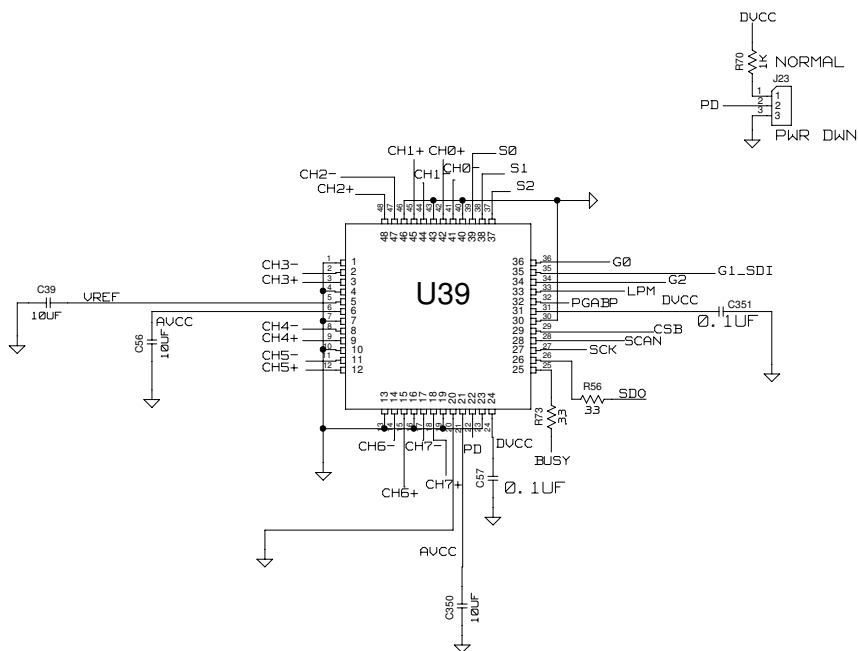
VREF  
BANK



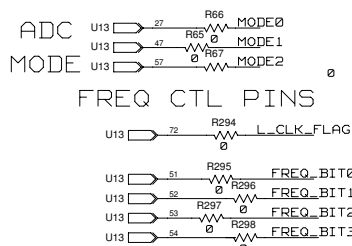
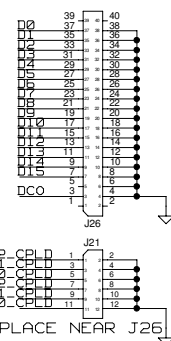
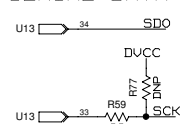
VREF/2  
BANK



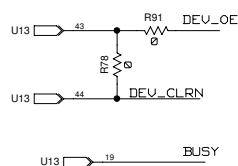
# ADC



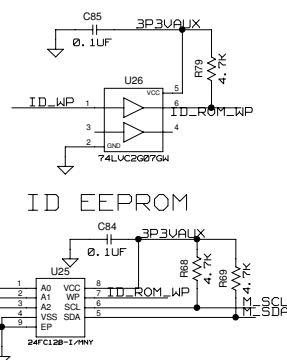
VERTICAL MOUNT  
PARALLEL CONNECTOR



## GPIO PINS



## ID EEPROM



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