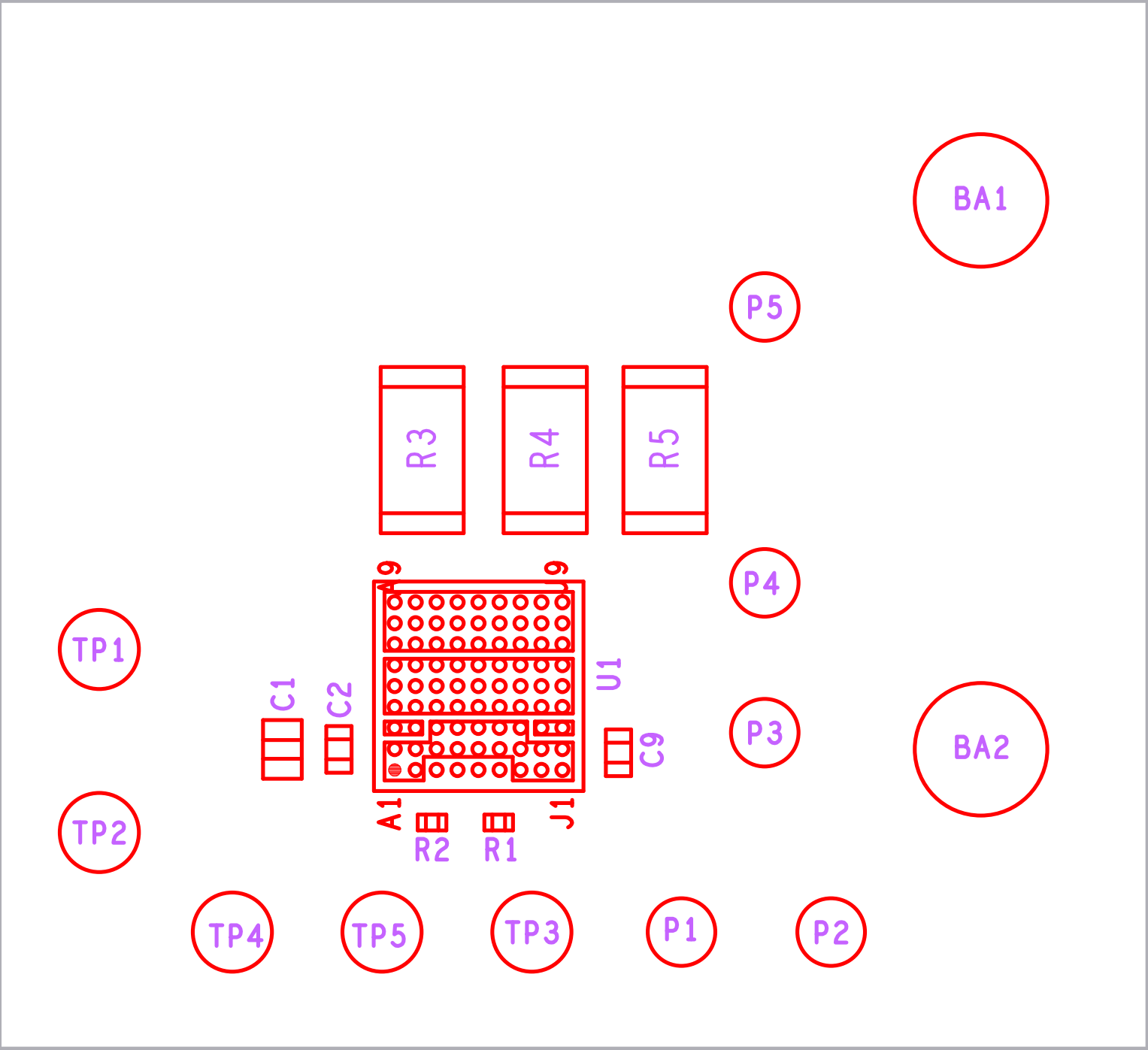


ISL73033SLHEV1Z REV.A

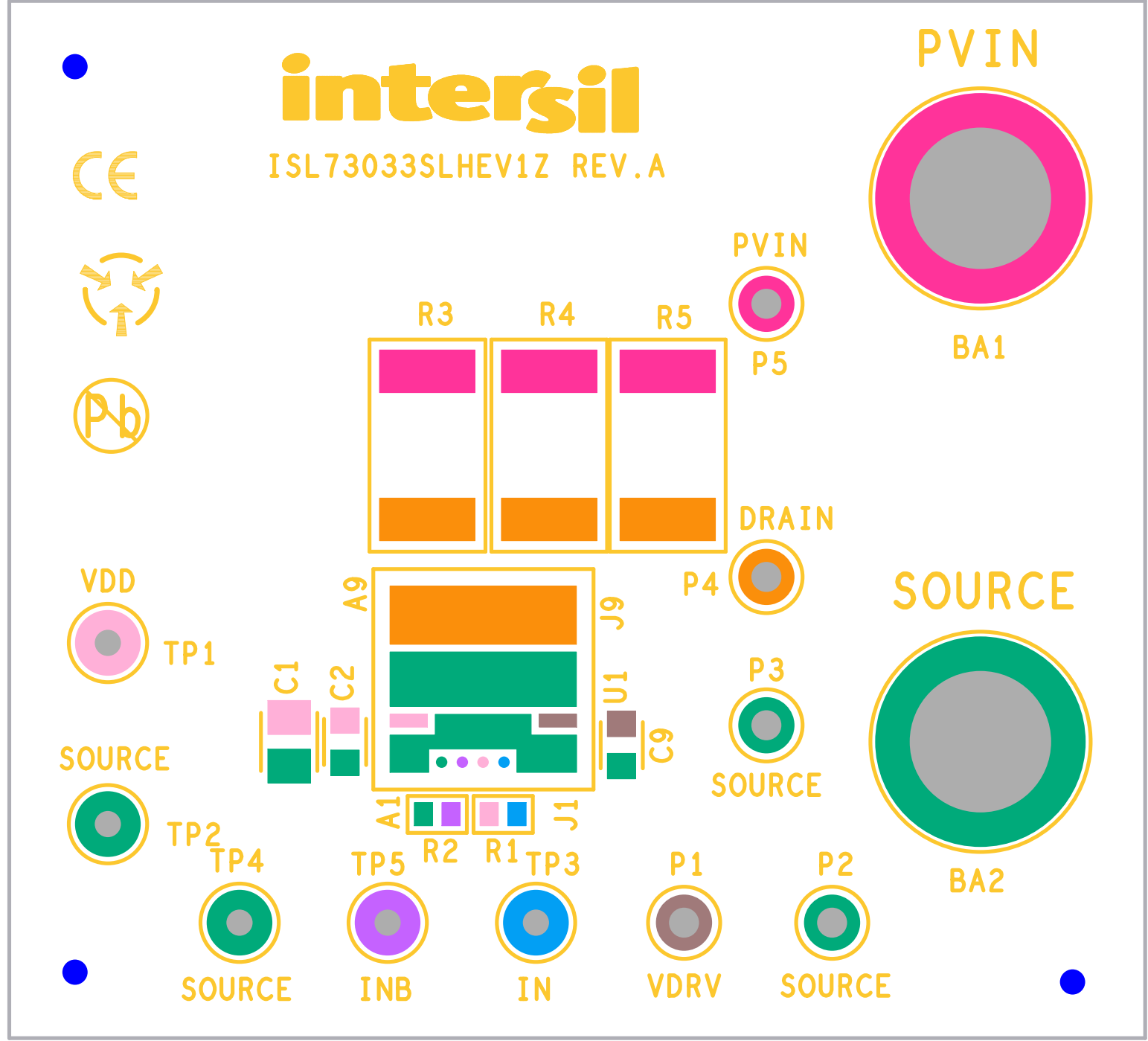


ASSEMBLY TOP

INTERSIL

08-26-2020

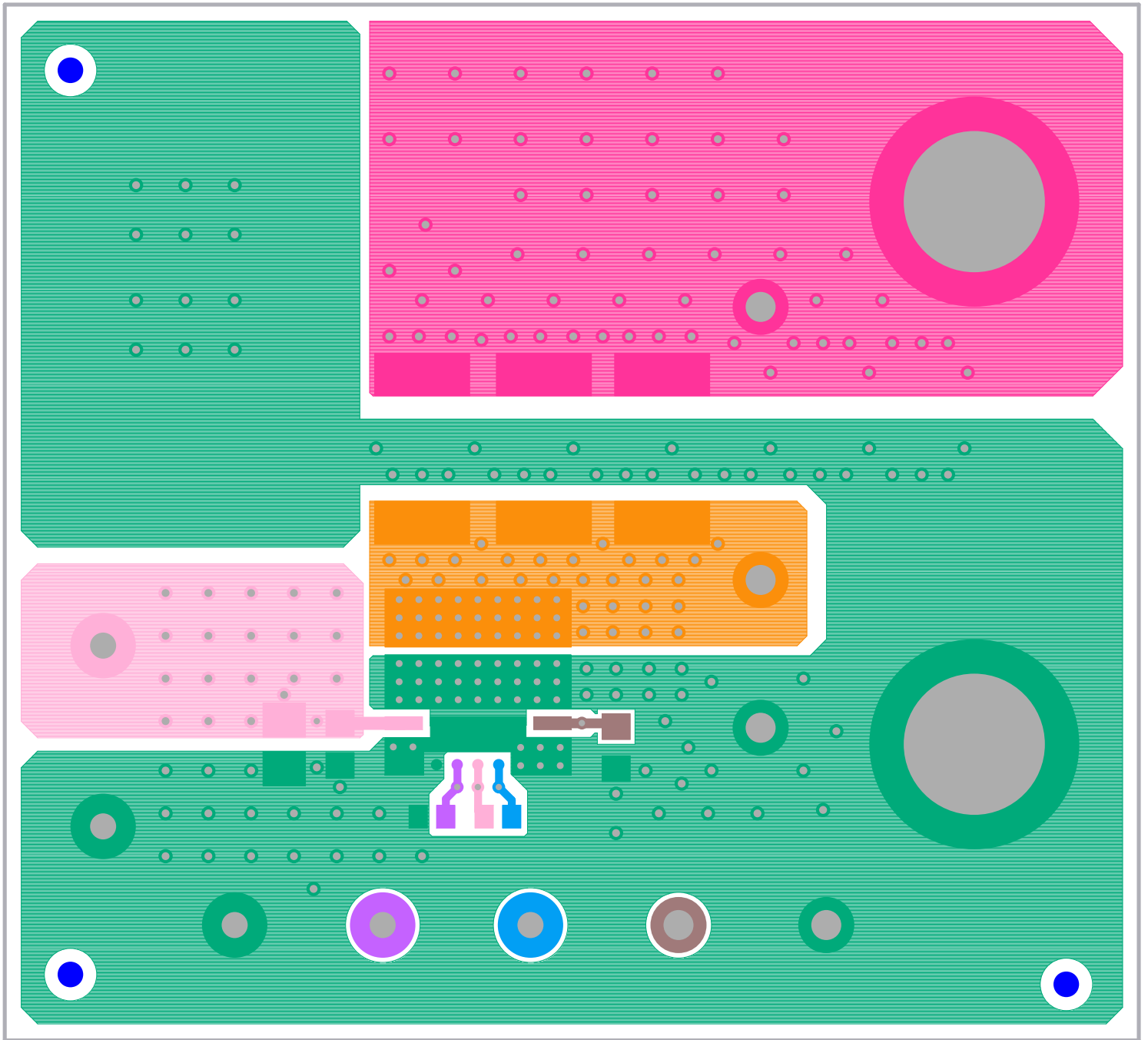
ISL73033SLHEV1Z REV.A



SILK SCREEN TOP

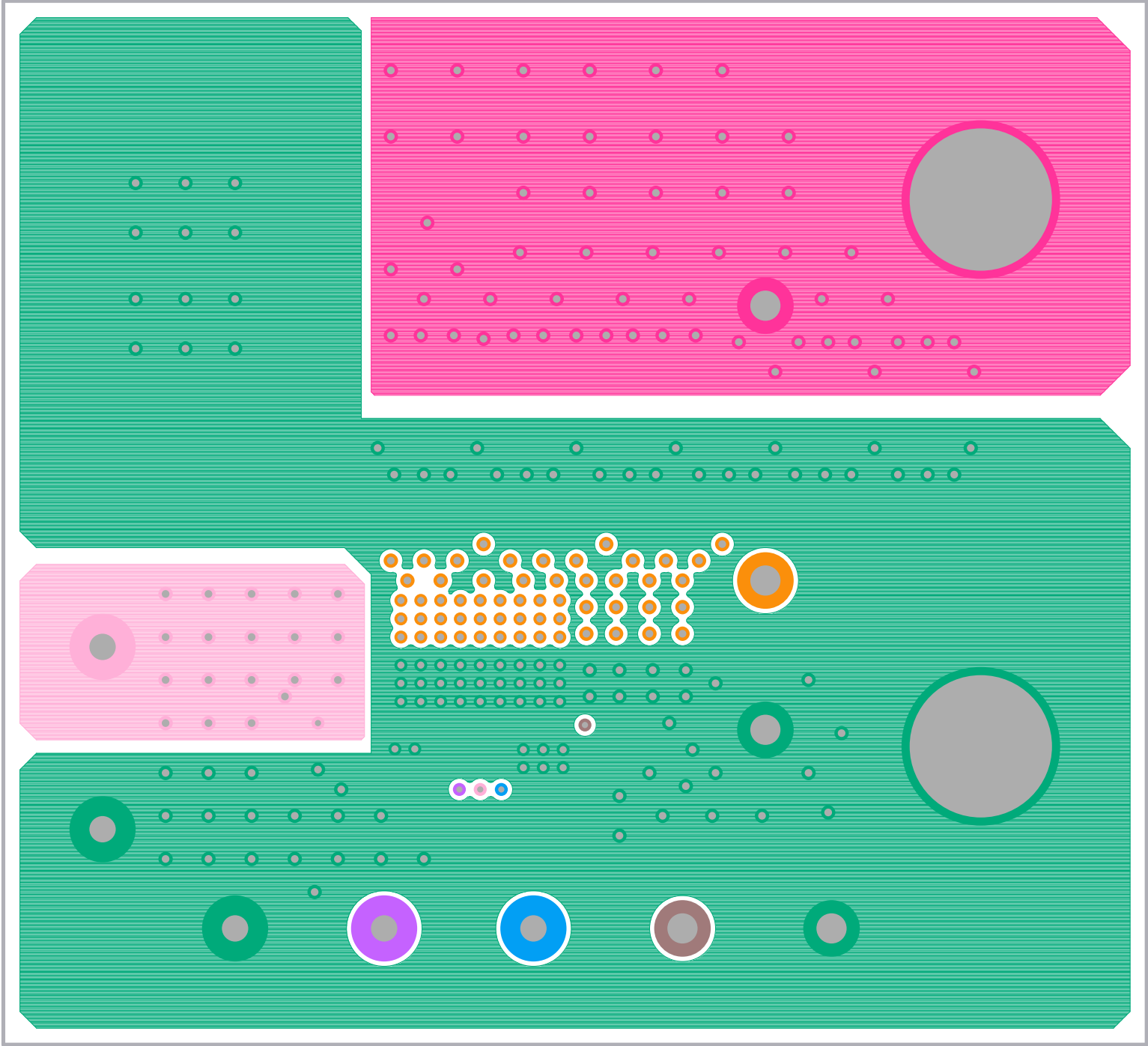
INTERSIL
08-26-2020

ISL73033SLHEV1Z REV.A



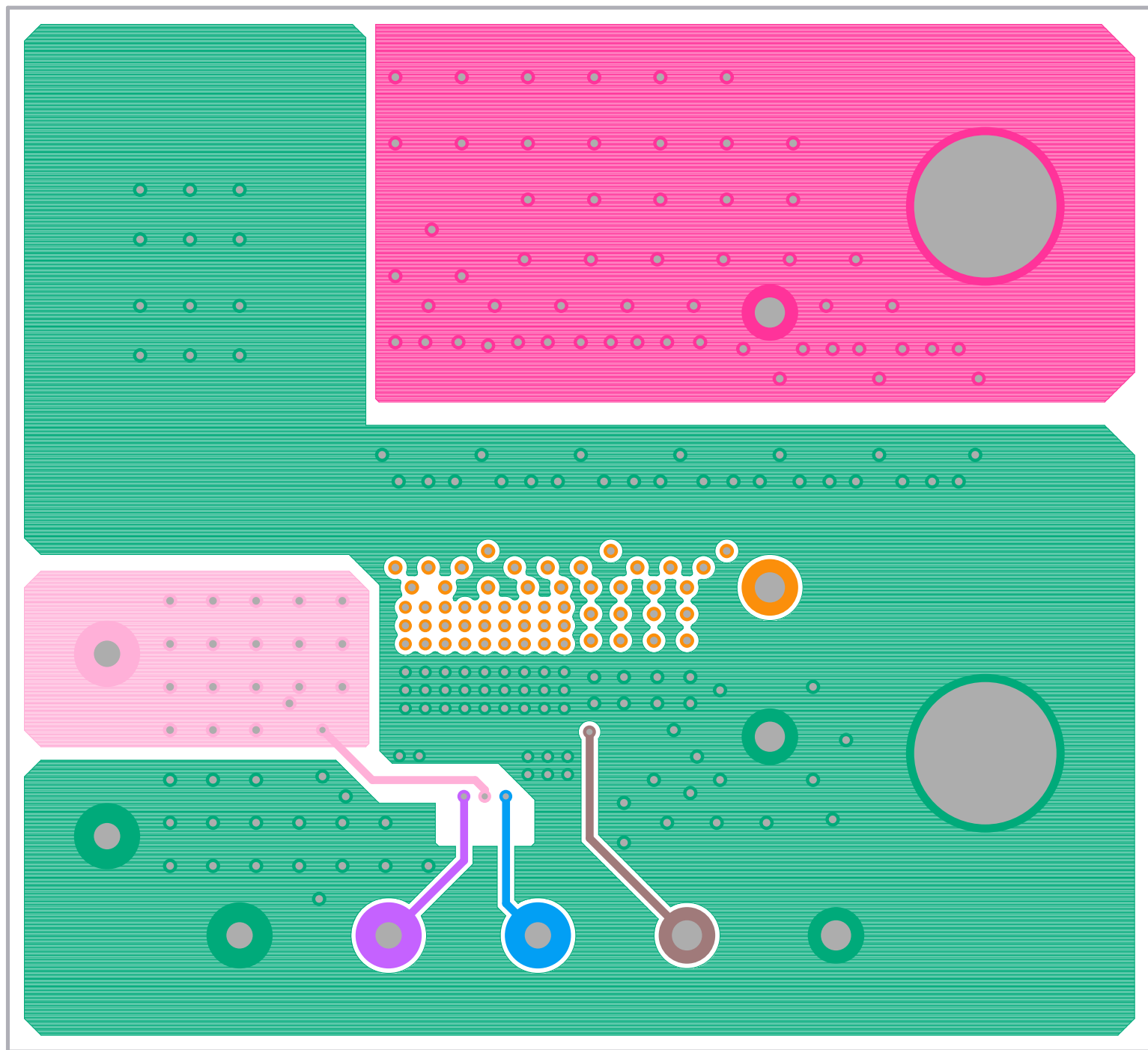
TOP LAYER COMPONENT SIDE
INTERSIL
08-26-2020

ISL73033SLHEV1Z REV.A



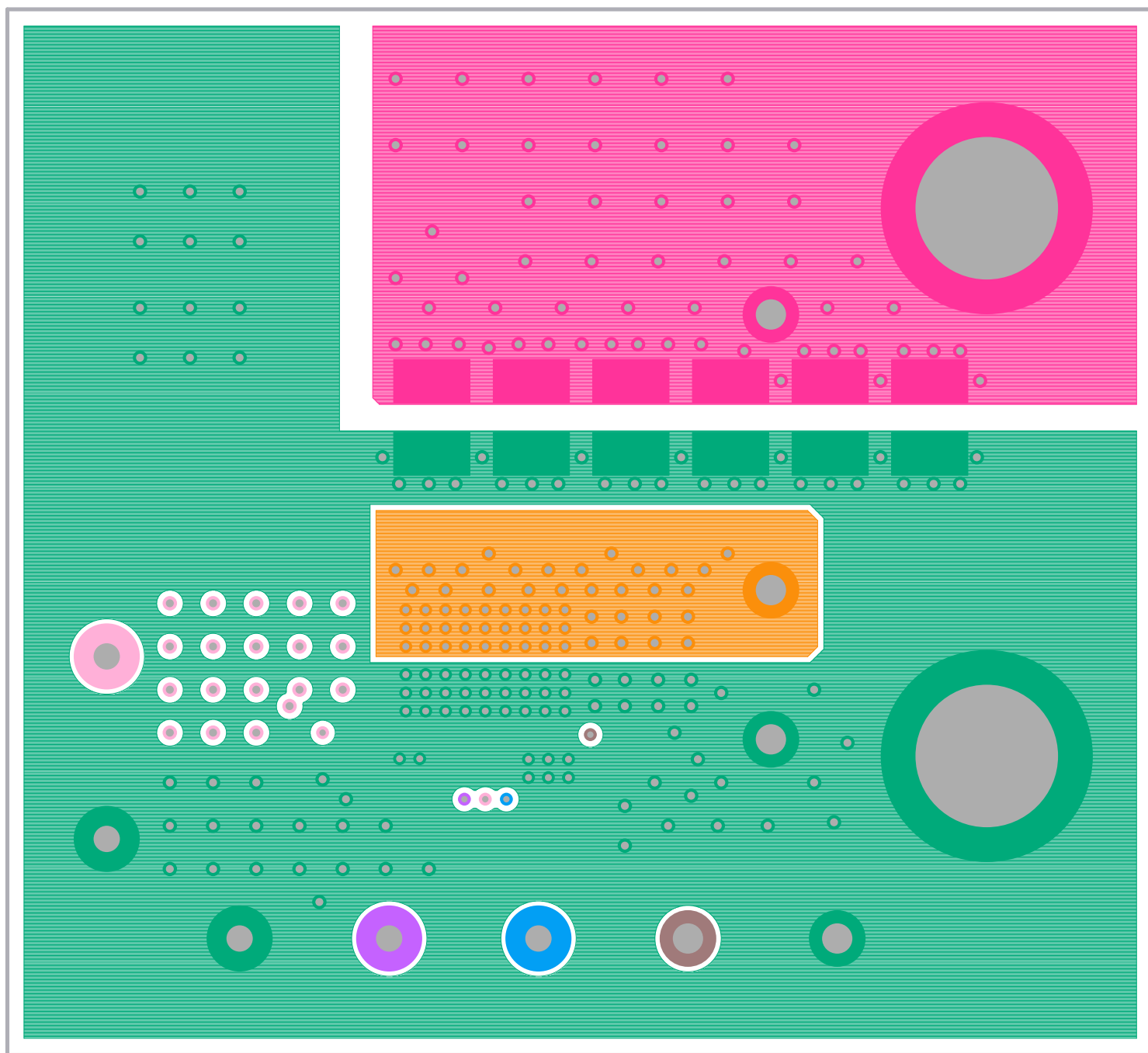
LAYER 2
INTERSIL
08-26-2020

ISL73033SLHEV1Z REV.A



LAYER 3
INTERSIL
08-26-2020

ISL73033SLHEV1Z REV.A

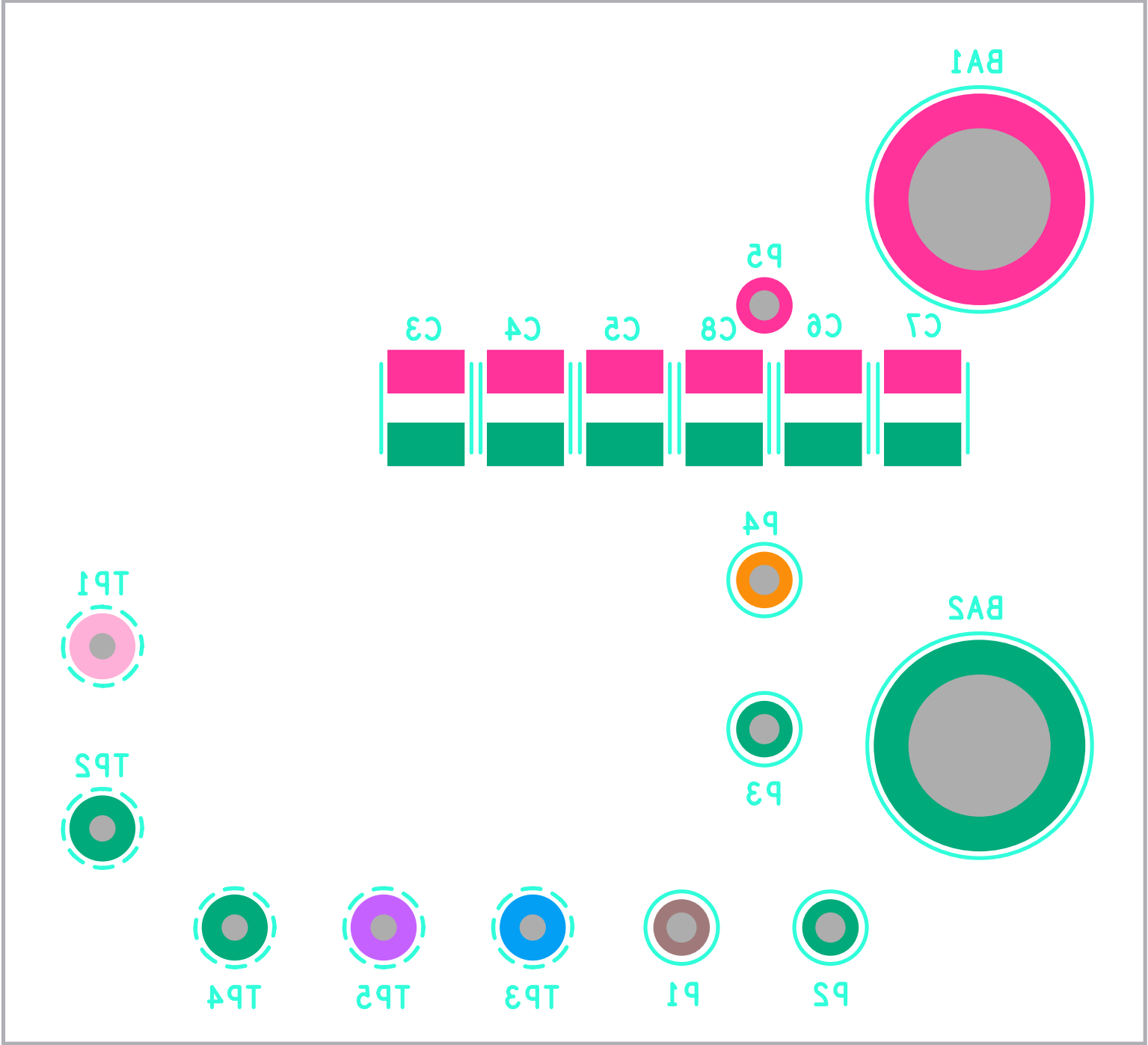


BOTTOM LAYER SOLDER SIDE

INTERSIL

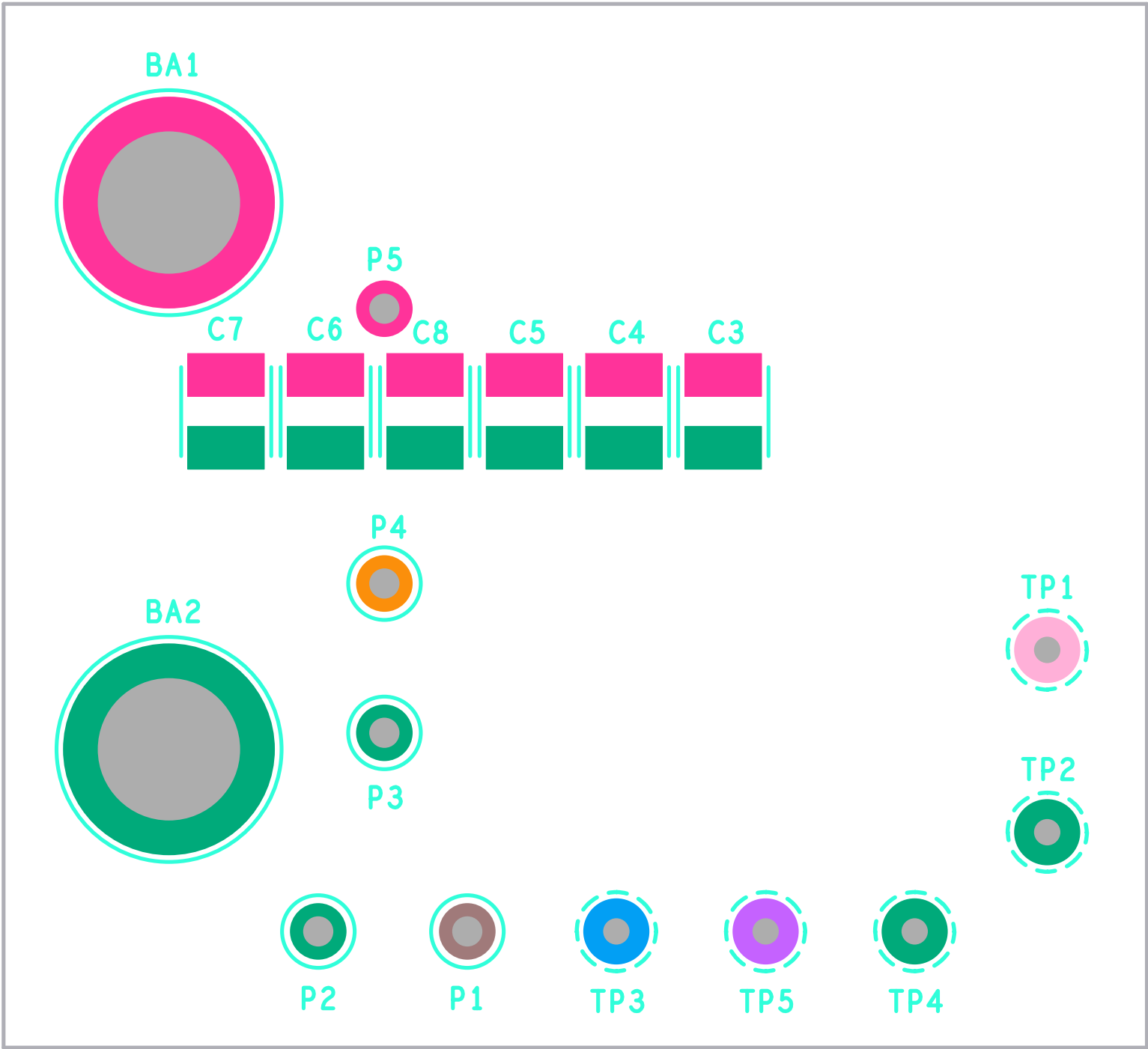
08-26-2020

ISL73033SLHEV1Z REV.A



SILK SCREEN BOTTOM
INTERSIL
08-26-2020

I2L730332LHEV1Z REV.A



SILK SCREEN BOTTOM

INTER2IL

08-56-5050

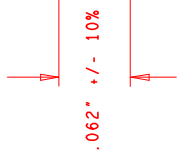
I 2 L 7 3 0 3 3 2 L H E V 1 2 R E V . A



A 2 S E M B L Y B O T T O M

I N T E R S I L
0 8 - 5 6 - 5 0 5 0

PHYSICAL BOARD DIMENSIONS
& LAYER STRUCTURE

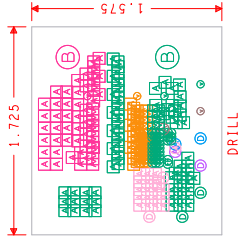


SILK TOP	silkt.art
MASK TOP	smaskt.art
(TOP)COMPONENT	layer1.art
LAYER 2	layer2.art
LAYER 3	layer3.art
(BOTTOM) SOLDER	layer4.art
MASK BOTTOM	maskb.art
SILK BOTTOM	silkb.art

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	PLATED	QTY	
Ⓐ	10.0	PLATED	5	
Ⓑ	11.0	PLATED	62	
Ⓐ	12.0	PLATED	182	
Ⓒ	40.0	PLATED	5	
Ⓒ	46.0	PLATED	5	
Ⓑ	215.0	PLATED	2	

NOTES:

1. THIS BOARD IS RoHS COMPLIANT.
2. PRINTED WIRING BOARD DESIGN AND ACCEPTANCE CRITERIA SHALL BE IAW WITH THE REQUIREMENTS OF IPC-D-275 AND IPC-A-600.
3. MATERIAL: FR4 (RoHS COMPLIANT), 2 OZ COPPER LAYERS 1 & 4, 1 OZ LAYERS 2 & 3..
4. APPLY SOLDER MASK, BOTH SIDES OVER BARE COPPER IAW IPC-SM-840. CLASS 2 (LPI) (BLUE MASK).
5. ALL PATTERNS ARE VIEWED FROM THE PRIMARY SIDE LOOKING THROUGH THE BOARD.
6. UNLESS OTHERWISE SPECIFIED ALL HOLE DIAMETERS ARE AFTER PLATING.
7. APPLY SILKSCREEN USING WHITE NON-CONDUCTIVE EPOXY BASED INK.
8. PWB MUST BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY. USE NETLIST PROVIDED ISL73033SLHEV1ZA_IPC356.IPC IAW IPC-D-356.
9. MARK DATE CODE AND MANUFACTURES IDENTIFICATION ON SOLDER SIDE PER IPC-6011 AND IPC-6012.
10. TOLERANCE ON ALL DRILL HOLES SHALL BE IAW IPC-D-2221 & 2222 UNLESS OTHERWISE SPECIFIED.
11. ALL 11 MIL VIAS ARE TO BE NON-CONDUCTIVE EPOXY FILLED AND CAPPED.



Drawn By:	Date Drawn:	Engineer:
Tim Klemann	09/02/2020	Kiran Bernard
Released By:	Date Released:	ISL73033SLH EVALUATION BOARD LAYOUT
Updated By:	Date Updated:	
		MASK#
		ISL73033SLHEV1Z
		REV.
		A
interSil		
FILENAME: \\\ISL73033SLH\ISL73033SLHEV1ZA		
1 of 1		