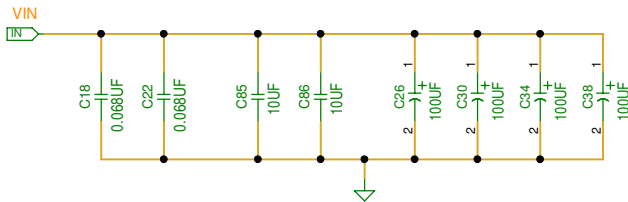


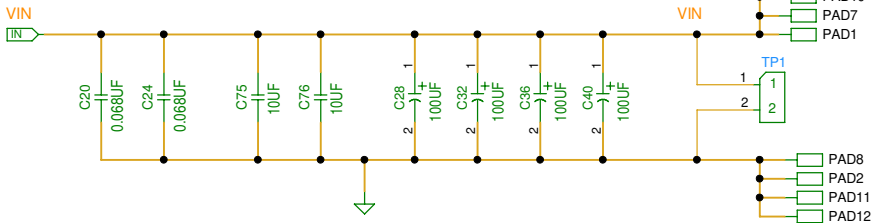
DRAWN BY: TIM KLEMANN	DATE: 12/12/2023	ENGINEER: JUAN GARCIA	DATE:
RELEASED BY:	DATE:	TITLE: ISL73847SEH DEMO6 BOARD SCHEMATIC	
UPDATED BY: TIM KLEMANN	DATE: 05/29/2024	TESTER	
intersil		FILENAME: ~ISL73847SEH\ISL73847SEHDEMO6ZA	SHEET 1 OF 5
		MASK#	HRDWR ID REV. A

**intersil™**

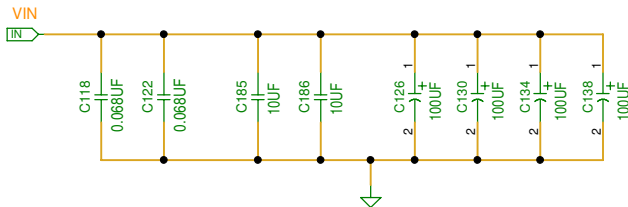
FROM INPUT CAPS
PHASE 1



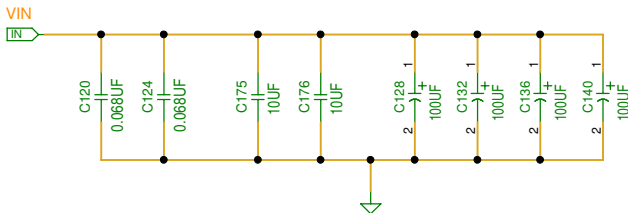
FROM INPUT CAPS
PHASE 2



FROM INPUT CAPS
PHASE 3

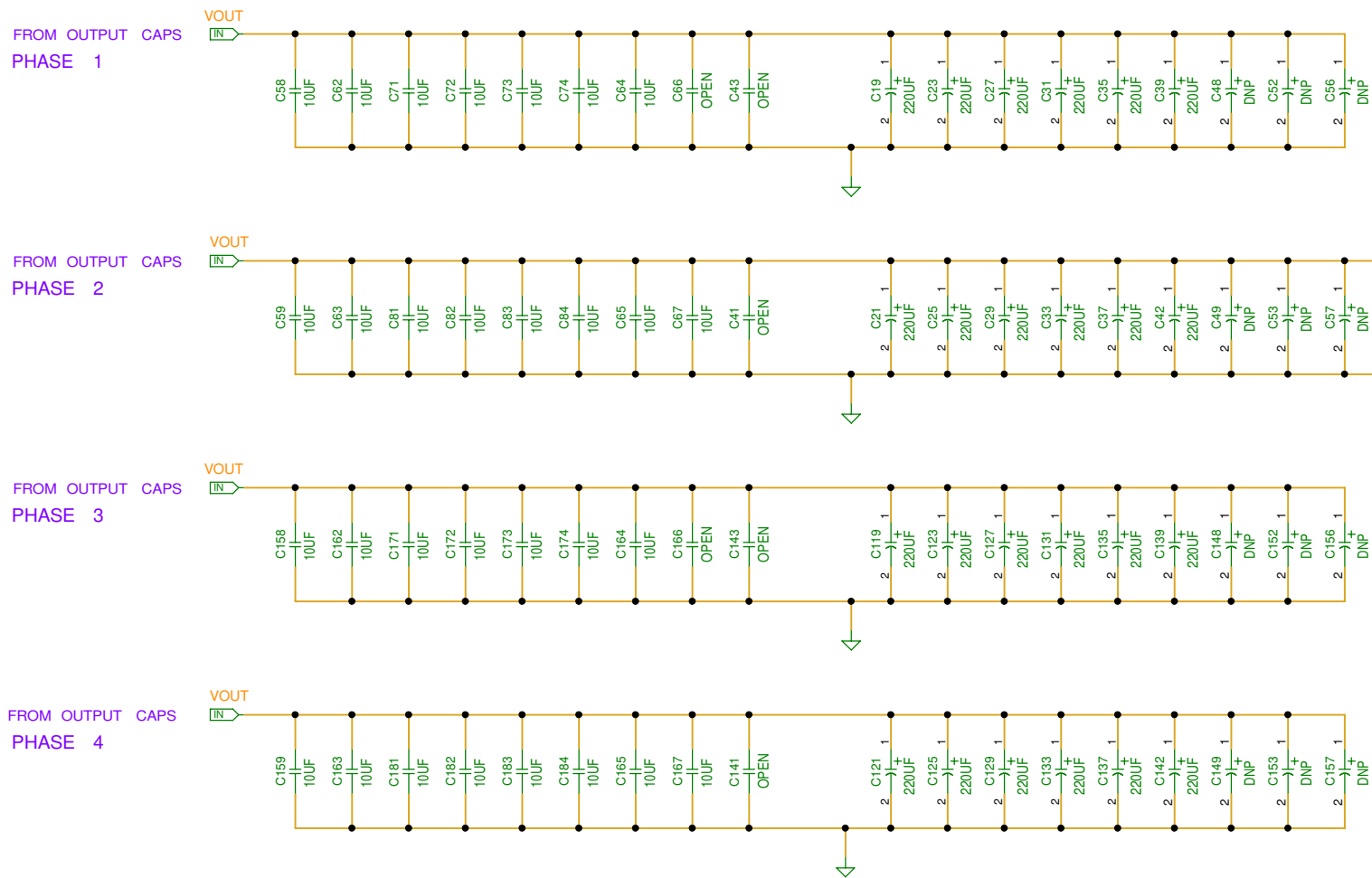


FROM INPUT CAPS
PHASE 4




INPUT PHASES 1 TO 4

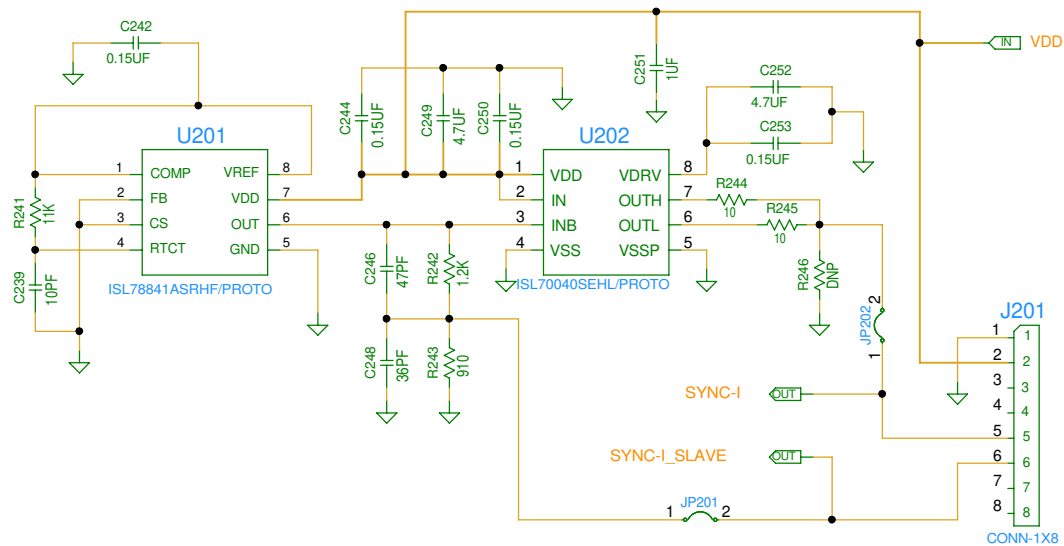
DRAWN BY: TIM KLEMANN	DATE: 11/03/2023	ENGINEER: JUAN GARCIA	DATE:
RELEASED BY:	DATE:	TITLE: ISL73847SEH DEMO6 BOARD SCHEMATIC	
UPDATED BY: TIM KLEMANN	DATE: 05/29/2024		
	TESTER	MASK#	HRDWR ID
	FILENAME: ~\ISL73847SEH\ISL73847SEHDEMO6ZA	REV. A	SHEET 3 OF 5



OUTPUT PHASES 1 TO 4

DRAWN BY: TIM KLEMMANN		DATE: 12/07/2023	ENGINEER: JUAN GARCIA		DATE:
RELEASED BY:		DATE:	ISL73847SEH DEMO6 BOARD SCHEMATIC		
UPDATED BY: TIM KLEMMANN		DATE: 05/29/2024			
		TESTER	MASK#	HRDWR ID	REV. A
		FILENAME: ~\ISL73847SEH\ISL73847SEHDEMO6ZA	SHEET 4 OF 5		

CLOCK SYNCHRONIZATION CIRCUIT



DRAWN BY:	TIM KLEMMANN	DATE:	11/03/2023	ENGINEER:	JUAN GARCIA	DATE:	
RELEASED BY:		DATE:		TITLE:	ISL73847SEH DEMO6 BOARD SCHEMATIC		
UPDATED BY:	TIM KLEMMANN	DATE:	05/29/2024	TESTER			
		FILENAME:	-ISL73847SEH\ISL73847SEHDEMO6ZA		MASK#	HRDWR ID	REV. A
				SHEET 5 OF 5			