
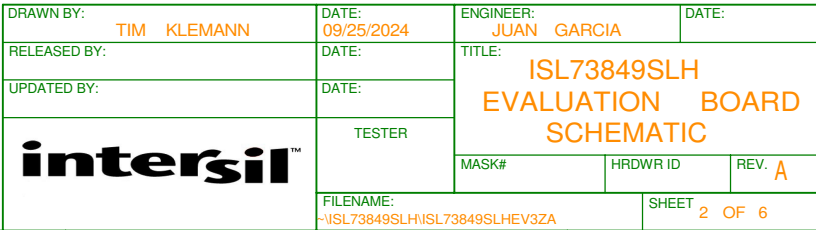
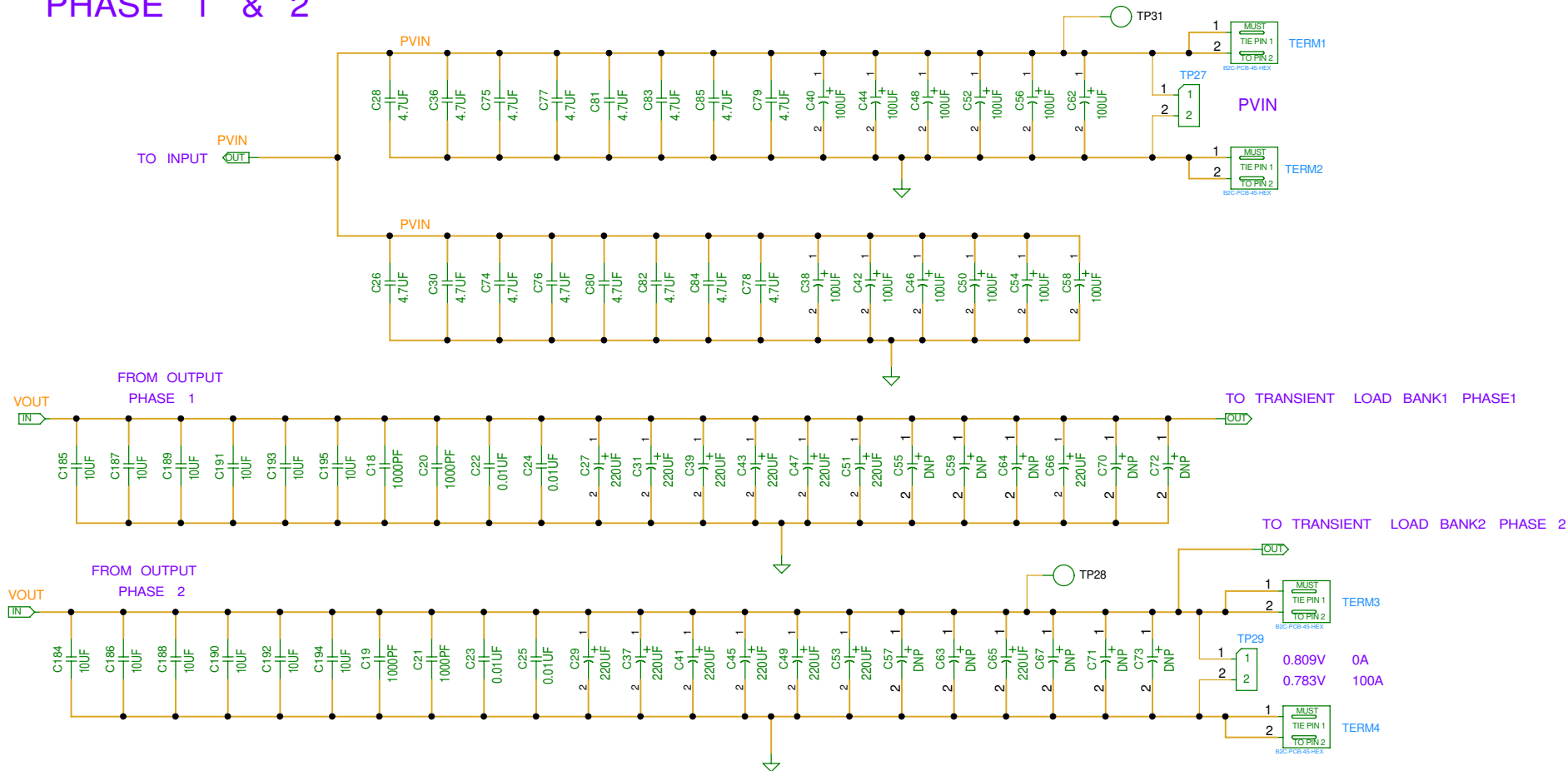


DRAWN BY: TIM KLEMMANN		DATE: 09/30/2024		ENGINEER: JUAN GARCIA		DATE:	
RELEASED BY:		DATE:		TITLE: ISL73849SLH EVALUATION BOARD SCHEMATIC			
UPDATED BY:		DATE:					
		TESTER		MASK#		HRDWR ID	REV. A
				FILENAME: ~\ISL73849SLH\ISL73849SLHEV3ZA		SHEET 1 OF 6	

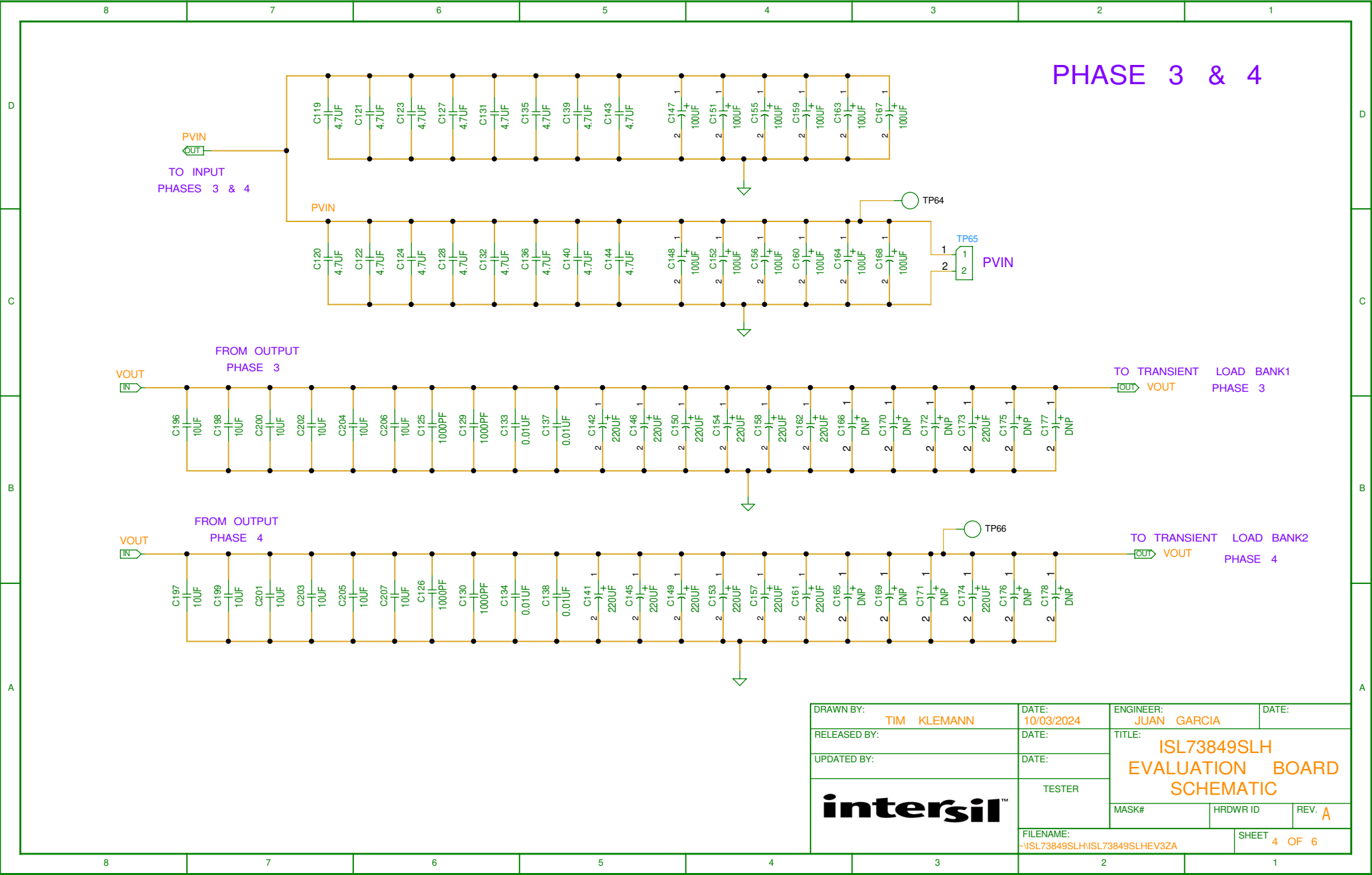
FROM INPUT CAPS
PHASE 3 & 4



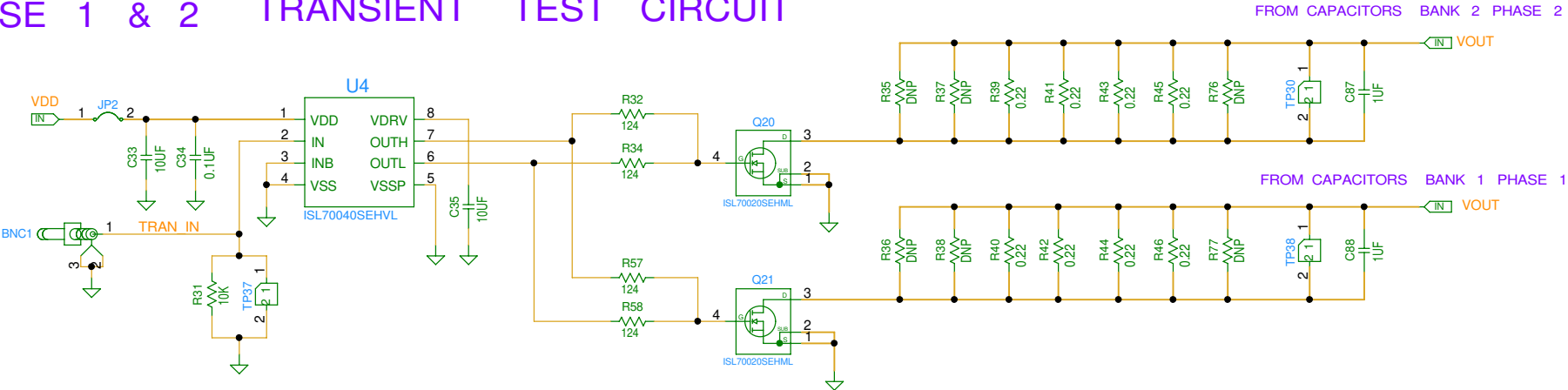
PHASE 1 & 2



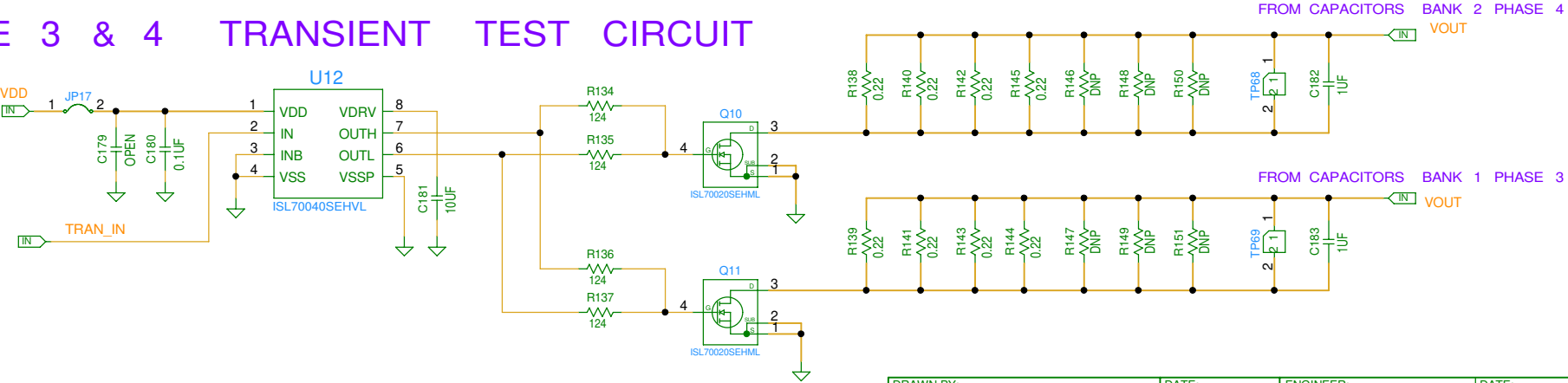
DRAWN BY: TIM KLEMMANN	DATE: 10/03/2024	ENGINEER: JUAN GARCIA	DATE:
RELEASED BY:	DATE:	TITLE: ISL73849SLH EVALUATION BOARD SCHEMATIC	
UPDATED BY:	DATE:	TESTER	
		MASK#	HRDWR ID
FILENAME: ~\ISL73849SLH\ISL73849SLHEV3ZA		REV. A	
		SHEET 3 OF 6	



PHASE 1 & 2 TRANSIENT TEST CIRCUIT



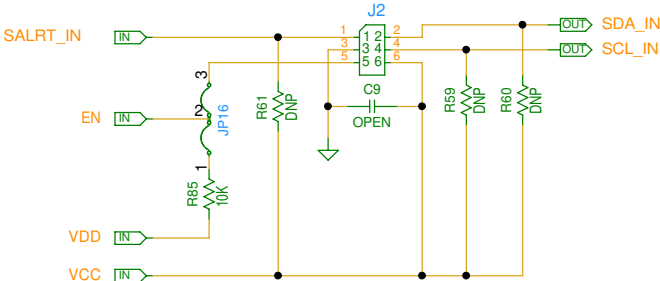
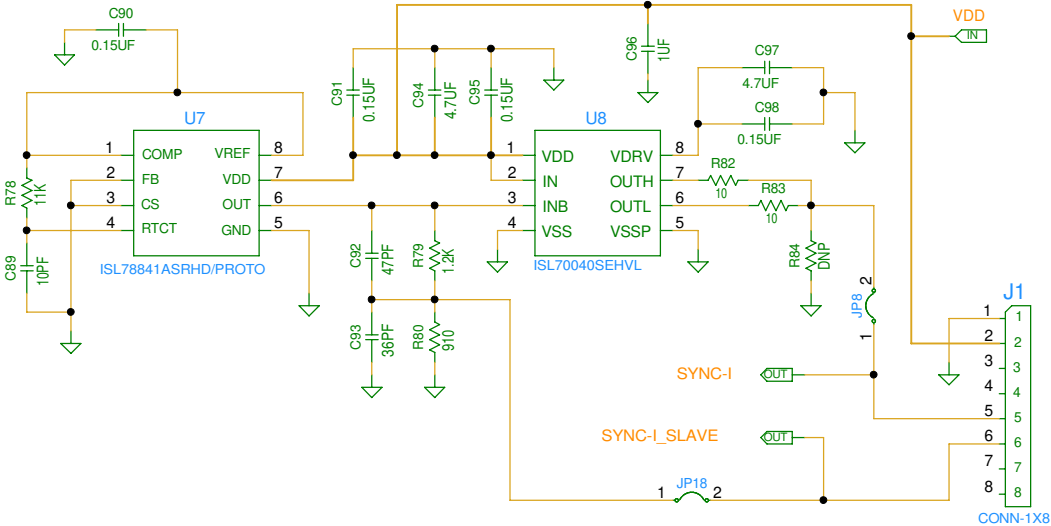
PHASE 3 & 4 TRANSIENT TEST CIRCUIT



DRAWN BY: TIM KLEMMANN	DATE: 09/25/2024	ENGINEER: JUAN GARCIA	DATE:
RELEASED BY:	DATE:	TITLE: ISL73849SLH EVALUATION BOARD SCHEMATIC	
UPDATED BY:	DATE:	TESTER	
FILENAME: ~\ISL73849SLH\ISL73849SLHEV3ZA		MASK#	HRDWR ID
		REV. A	SHEET 5 OF 6

CLOCK SYNCHRONIZATION CIRCUIT

PMBUS INTERFACE



DRAWN BY:	TIM KLEMANN	DATE:	09/25/2024	ENGINEER:	JUAN GARCIA	DATE:	
RELEASED BY:		DATE:		TITLE:	ISL73849SLH EVALUATION BOARD SCHEMATIC		
UPDATED BY:		DATE:		TESTER			
		MASK#		HRDWR ID		REV. A	
		FILENAME:		SHEET		6 OF 6	
		~ISL73849SLH\ISL73849SLHEV3ZA					