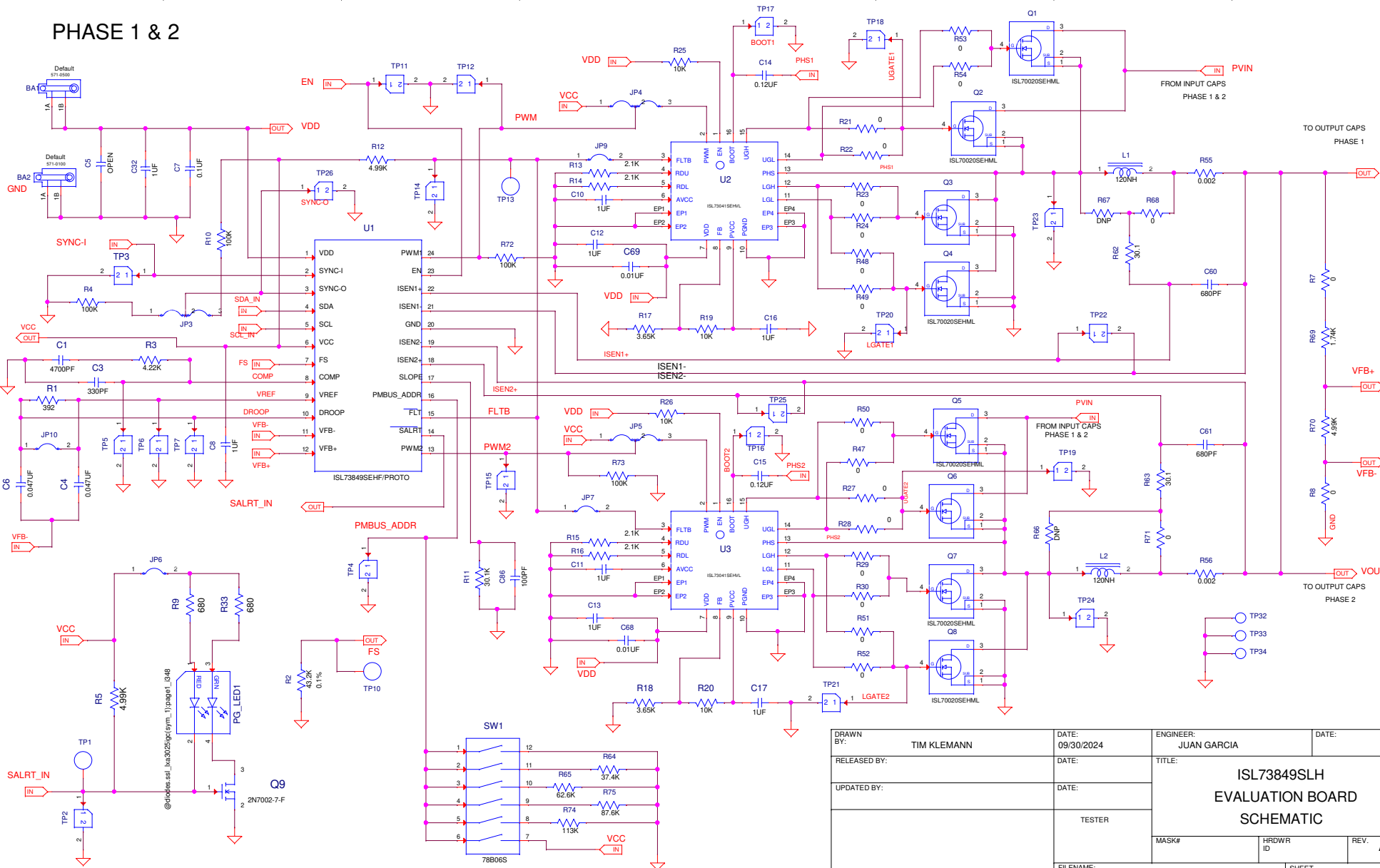


# PHASE 1 & 2



DRAWN BY: TIM KLEMMANN	DATE: 09/30/2024	ENGINEER: JUAN GARCIA	DATE:
RELEASED BY:	DATE:	TITLE: <b>ISL73849SLH EVALUATION BOARD SCHEMATIC</b>	
UPDATED BY:	DATE:	MASK#	REV. <b>A</b>
TESTER		FILENAME: -ISL73849SLH\ISL73849SLHEV3ZA	SHEET 1 OF 6

# PHASE 3 & 4

FROM INPUT CAPS  
PHASE 3 & 4

SYNC-I\_SLAVE

VCC\_SLAVE

FS\_SLAVE

VREF2

DROOP

VFB-

TP41

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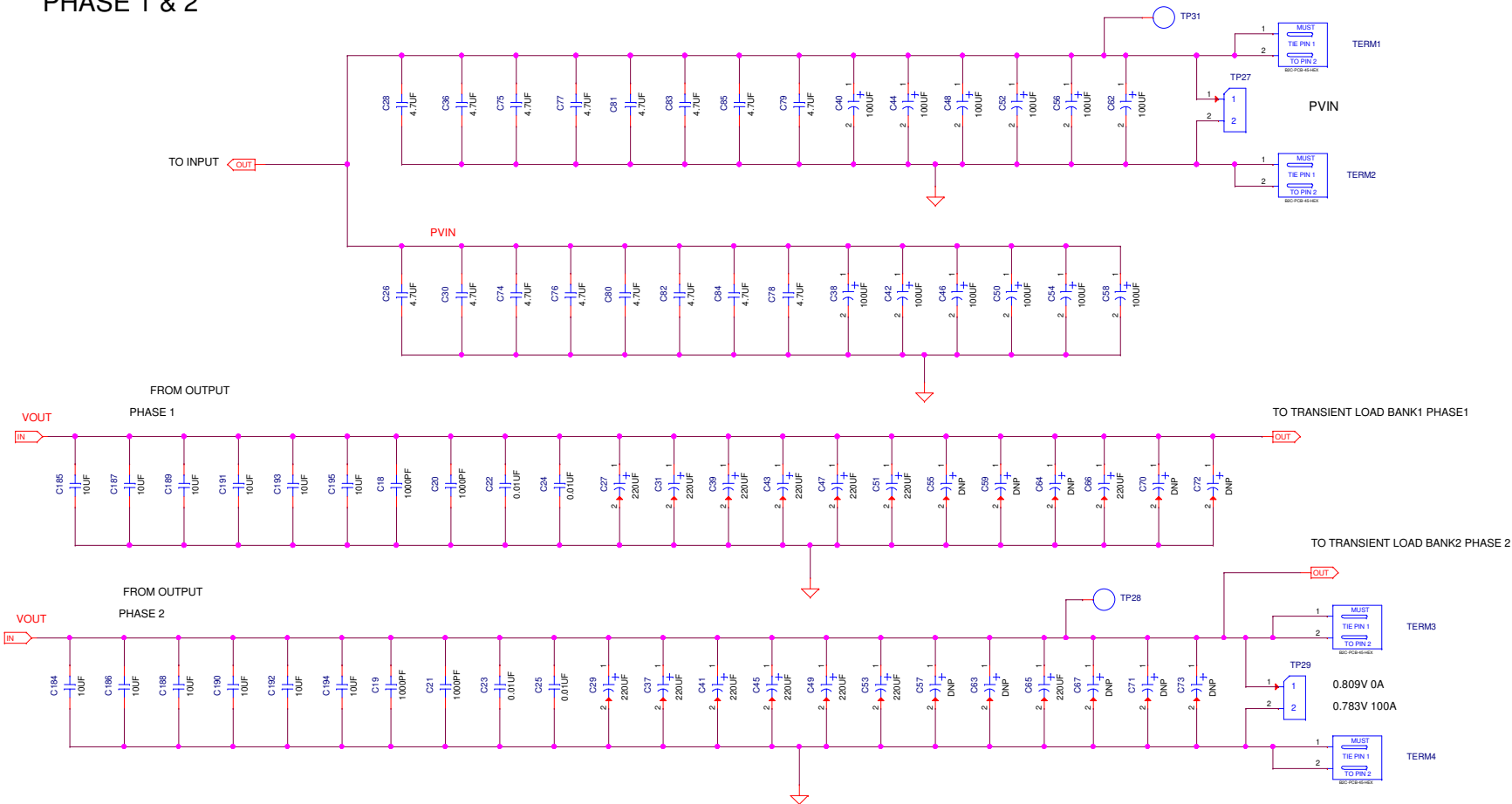
TP334

TP335

TP336

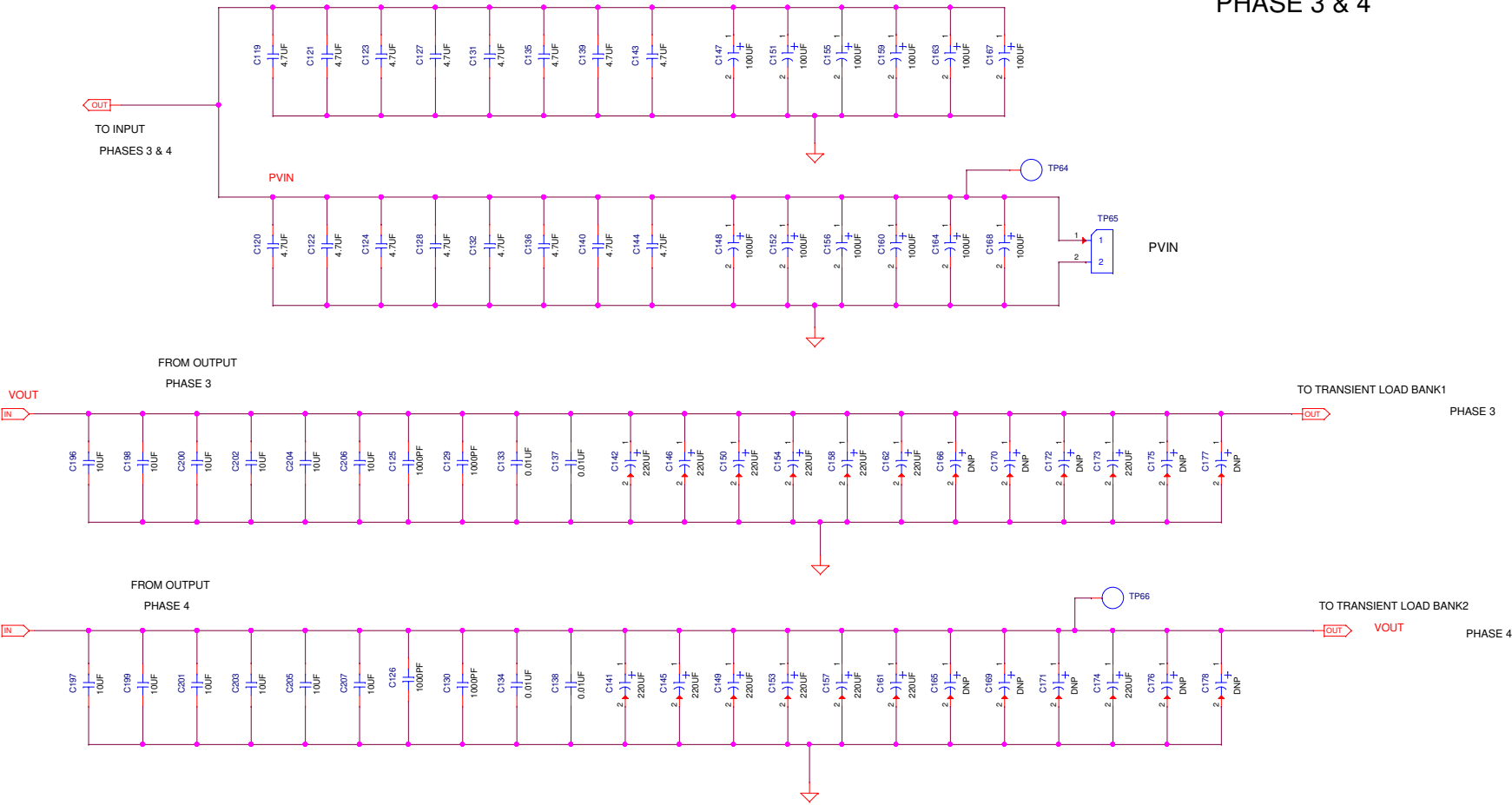
TP337

PHASE 1 & 2



DRAWN BY:	TIM KLEMMANN	DATE:	10/03/2024	ENGINEER:	JUAN GARCIA	DATE:	
RELEASED BY:		DATE:		TITLE:	ISL73849SLH EVALUATION BOARD SCHEMATIC		
UPDATED BY:		DATE:		TESTER:		MASK#	REV. A
FILENAME:				SHEET		3 OF 6	
~\ISL73849SLH\ISL73849SLHEV3ZA							

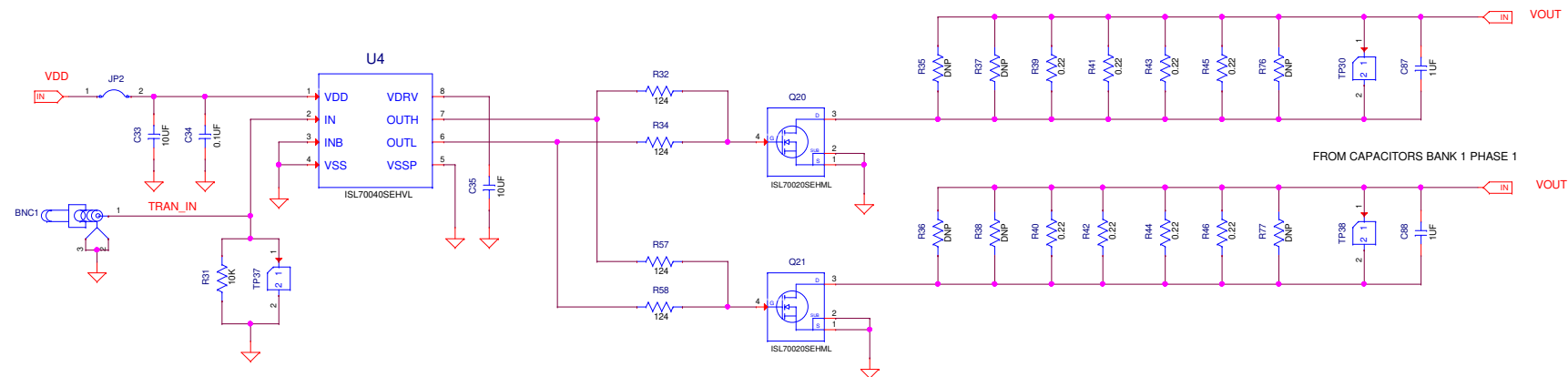
PHASE 3 & 4



DRAWN BY: TIM KLEMMANN	DATE: 10/03/2024	ENGINEER: JUAN GARCIA	DATE:
RELEASED BY:	DATE:	TITLE: <b>ISL73849SLH EVALUATION BOARD SCHEMATIC</b>	
UPDATED BY:	DATE:		
	TESTER	MASK#	REV. <b>A</b>
FILENAME: -ISL73849SLH\ISL73849SLHEV3ZA		SHEET	4 OF 6

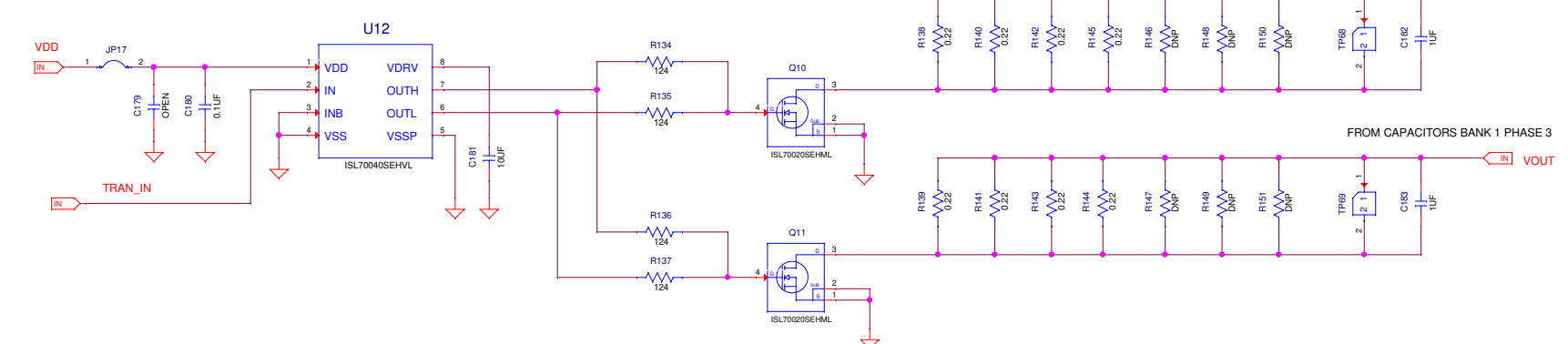
PHASE 1 & 2

TRANSIENT TEST CIRCUIT



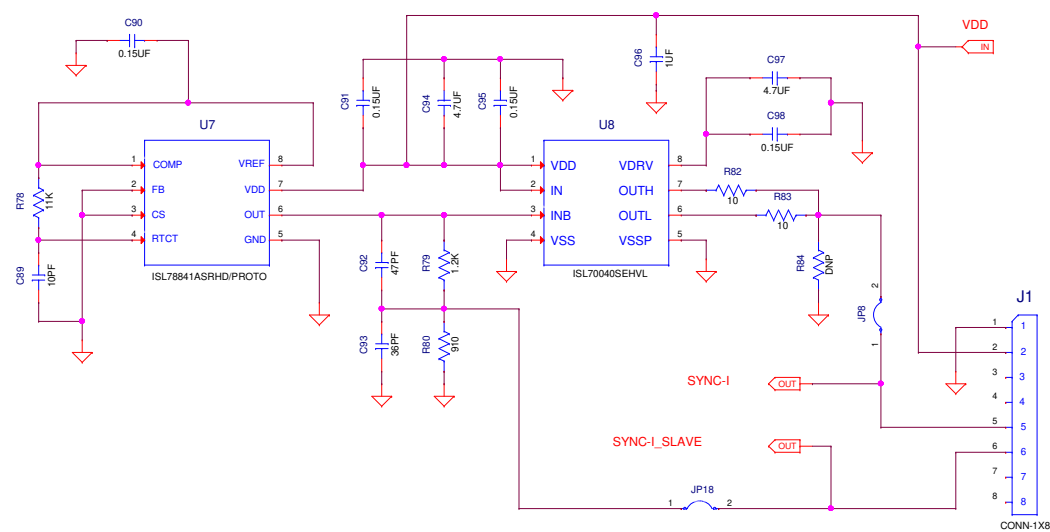
PHASE 3 & 4

TRANSIENT TEST CIRCUIT

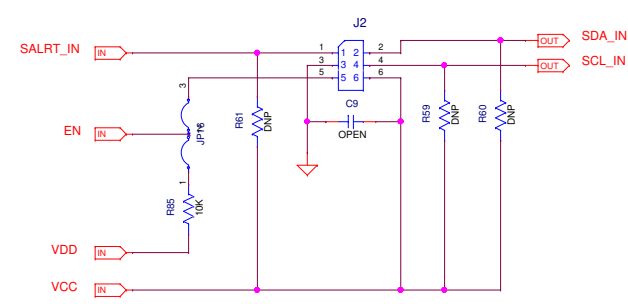


DRAWN BY: TIM KLEMAN	DATE: 09/25/2024	ENGINEER: JUAN GARCIA	DATE:
RELEASED BY:	DATE:	TITLE: ISL73849SLH EVALUATION BOARD SCHEMATIC	
UPDATED BY:	DATE:	TESTER:	
		MASK#	HRDWR ID
		REV. A	
FILENAME: -ISL73849SLH\ISL73849SLHEV32A		SHEET 5 OF 6	

CLOCK SYNCHRONIZATION CIRCUIT



PMBUS INTERFACE



DRAWN BY: TIM KLEMAN	DATE: 09/25/2024	ENGINEER: JUAN GARCIA	DATE:
RELEASED BY:	DATE:	TITLE: <b>ISL73849SLH EVALUATION BOARD SCHEMATIC</b>	
UPDATED BY:	DATE:		
	TESTER		
FILENAME: -ISL73849SLH\ISL73849SLHEV3ZA		MASK#	REV. <b>A</b>
		HRDWR ID	SHEET 6 OF 6