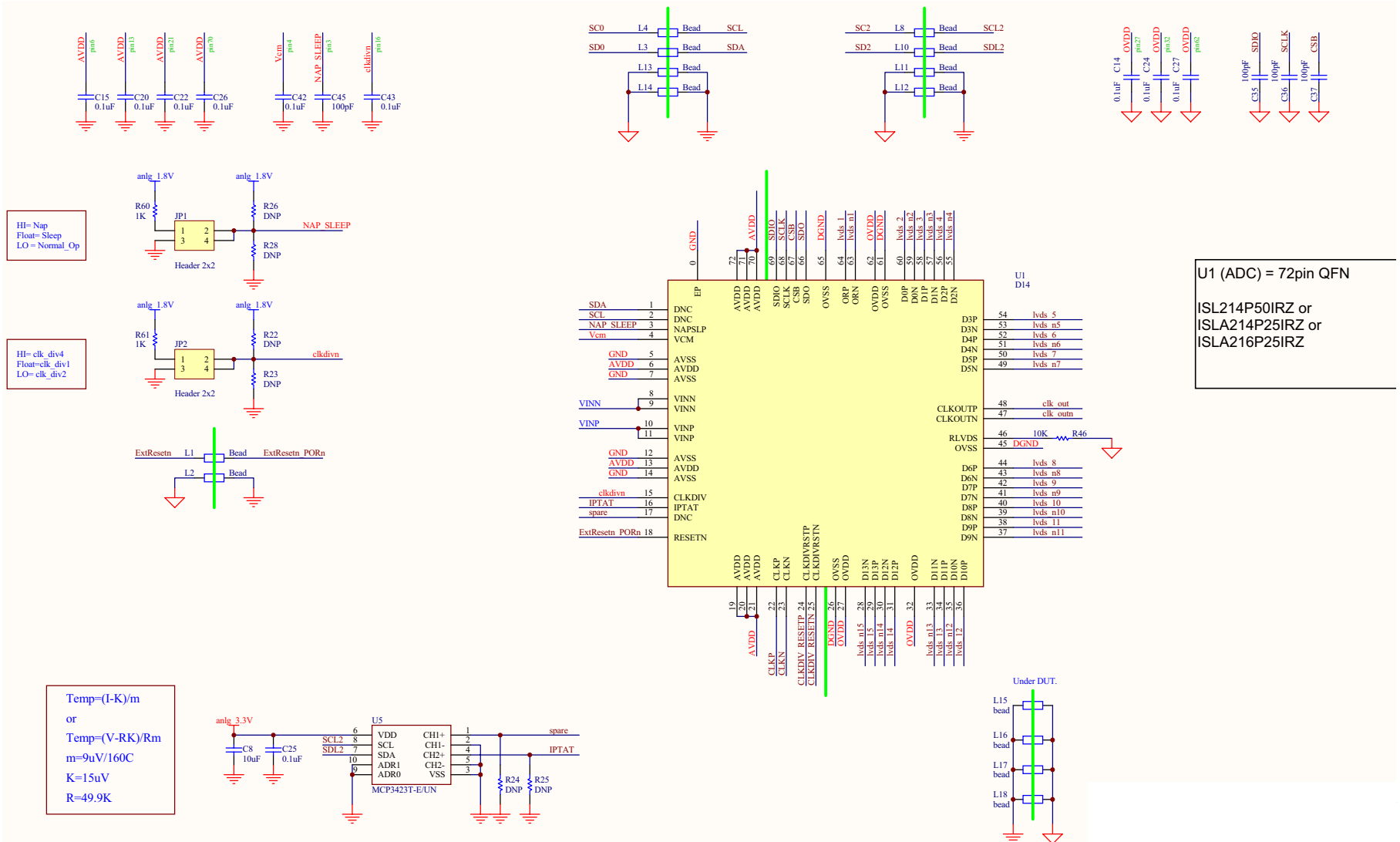


ISLA214P50IR72EV1Z Bill of Materials

Impedance Ratio	Mode	T5 PART NUMBER	T2 PART NUMBER	FS Input Power (dBm)	R19, R21 (Ohms)	R19, R21 Vishay Part number	R16, R17	R18, R20
1:1 *	ISLA214P25	ADTL1-12+	DNP	10	27	CRCW040227R0FKED	DNP	0 Ohm
	ISLA214P50	ADTL1-12+	DNP	10	30	CRCW040230R0FKED	DNP	0 Ohm
	ISLA216P25	ADTL1-12+	DNP	10	30	CRCW040230R0FKED	DNP	0 Ohm
2:1 *	ISLA214P25	TX-2-5-1	DNP	13	13	CRCW040213R0FKED	DNP	0 Ohm
	ISLA214P50	TX-2-5-1	DNP	13	13.7	CRCW040213R7FKED	DNP	0 Ohm
	ISLA216P25	TX-2-5-1	DNP	13	13.7	CRCW040213R7FKED	DNP	0 Ohm
4:1	ISLA214P25	DNP	TC4-19G2+	16	6.34	CRCW04026R34FKED	0 Ohm	DNP
	ISLA214P50	DNP	TC4-19G2+	16	6.49	CRCW04026R49FKED	0 Ohm	DNP
	ISLA216P25	DNP	TC4-19G2+	16	6.49	CRCW04026R49FKED	0 Ohm	DNP
1:2	ISLA214P25	TX-2-5-1 BACKWARD	DNP	7	60.4	CRCW040260R4FKED	DNP	0 Ohm
	ISLA214P50	TX-2-5-1 BACKWARD	DNP	7	75	CRCW040275R0FKED	DNP	0 Ohm
	ISLA216P25	TX-2-5-1 BACKWARD	DNP	7	75	CRCW040275R0FKED	DNP	0 Ohm

* Default PCB Build

ISLA214P50IR72EV1Z Schematics



U1 (ADC) = 72pin QFN
 ISLA214P50IRZ or
 ISLA214P25IRZ or
 ISLA216P25IRZ

ISLA214P50IR72EV1Z

FIGURE 1. ADC

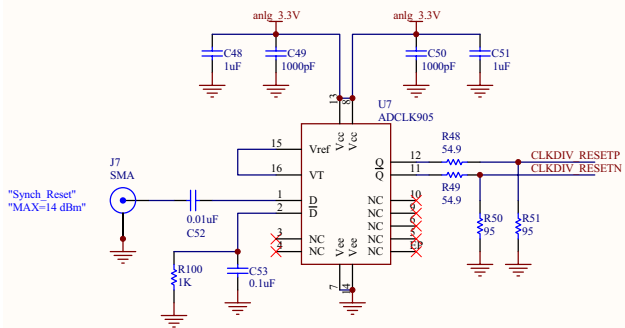
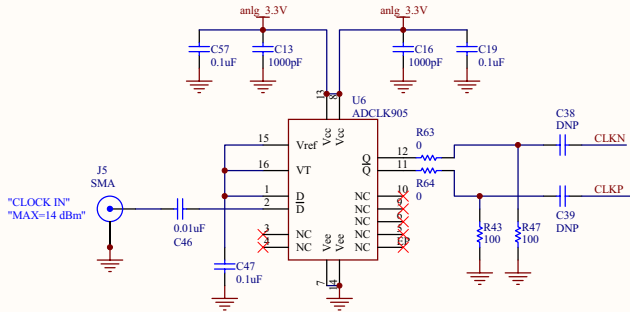
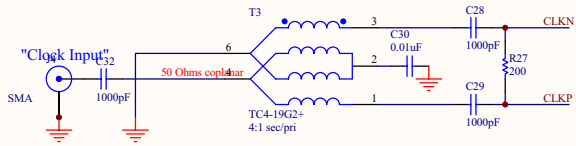
$Temp=(I-K)/m$
 or
 $Temp=(V-RK)/Rm$
 $m=9uV/160C$
 $K=15uV$
 $R=49.9K$

Under DUT.
 L15 bead
 L16 bead
 L17 bead
 L18 bead

ISLA214P50IR72EV1Z Schematics (Continued)

Sampling Clock Populate Depopulate

LVC MOS	C28, C29	C38, C39
LVDS	C38, C39	C28, C29



R100 was added to rev B pcb
Rev B pcb also Cut trace at C53

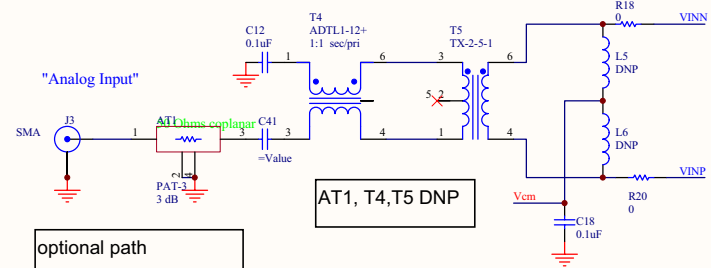
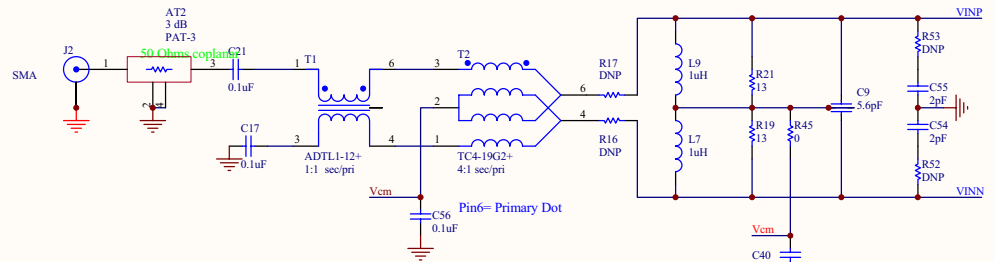


FIGURE 2. ANALOG FRONT END, CLOCK, SYNC RESET

ISLA214P50IR72EV1Z

ISLA214P50IR72EV1Z Layers

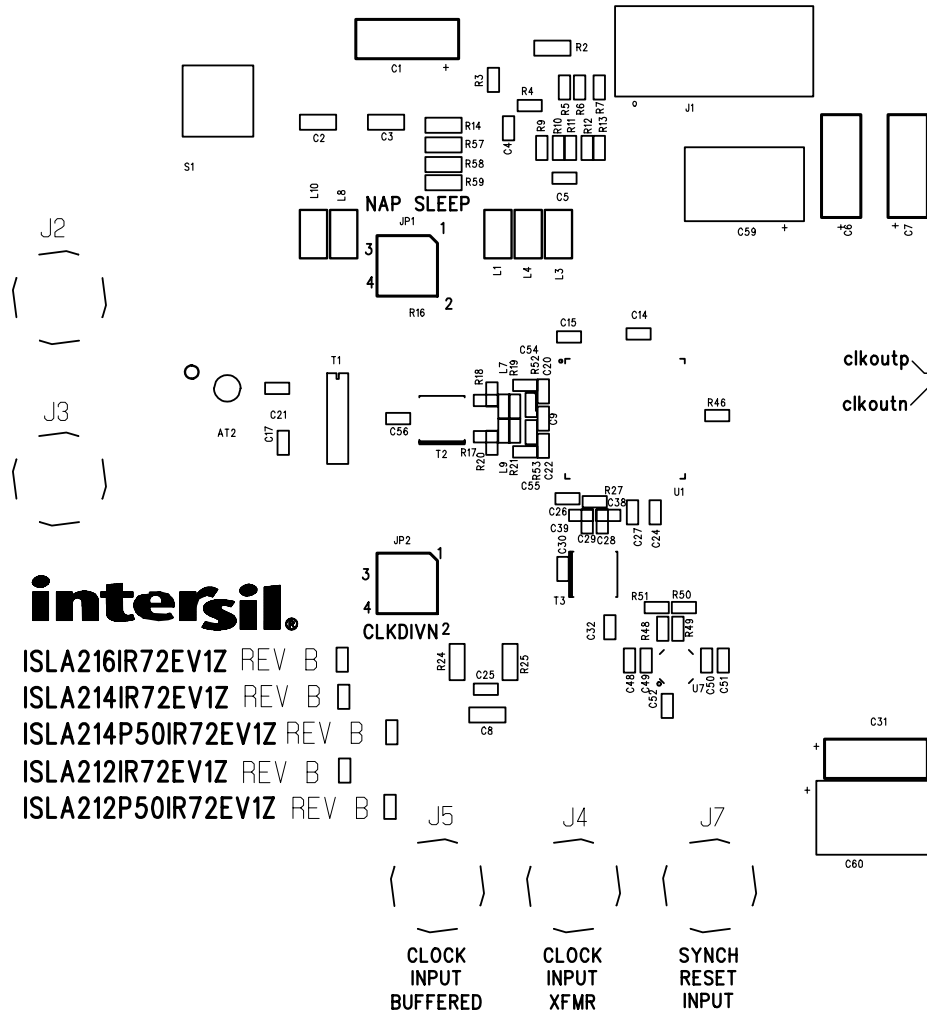


FIGURE 4. TOP SILKSCREEN

ISLA214P50IR72EV1Z Layers (Continued)

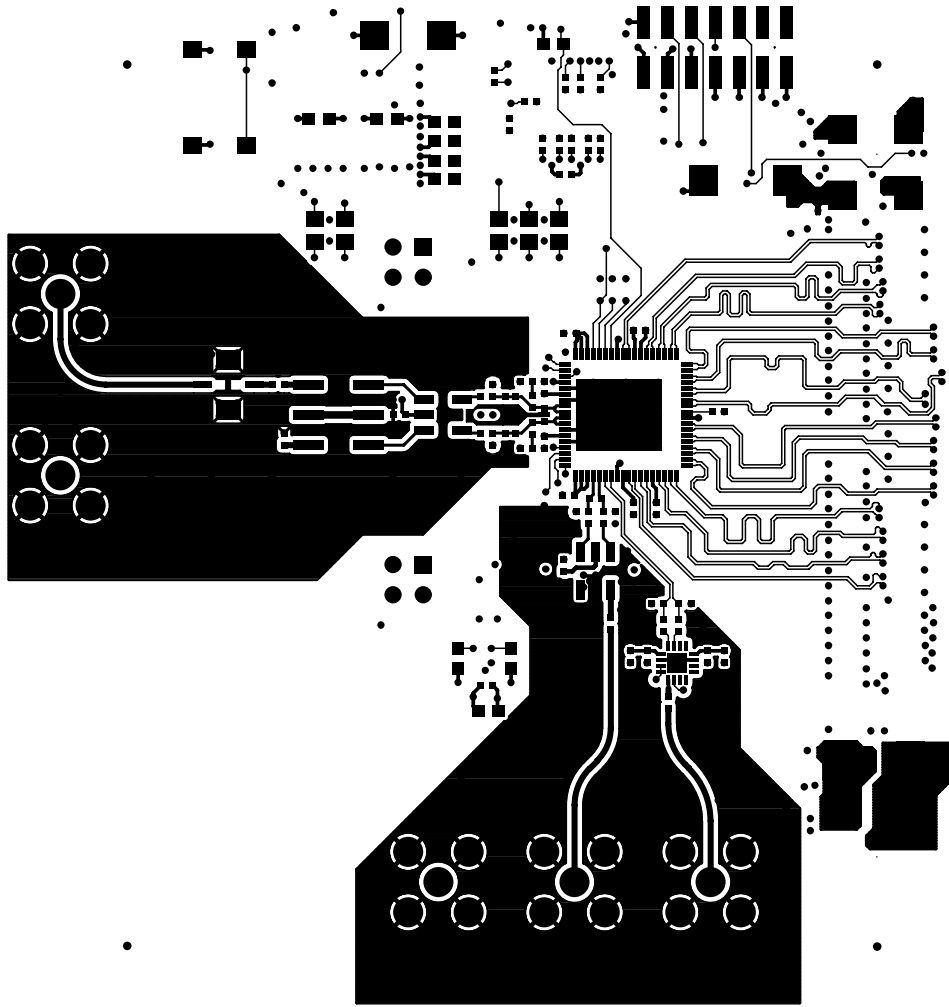


FIGURE 5. TOP LAYER ROUTING

ISLA214P50IR72EV1Z Layers (Continued)

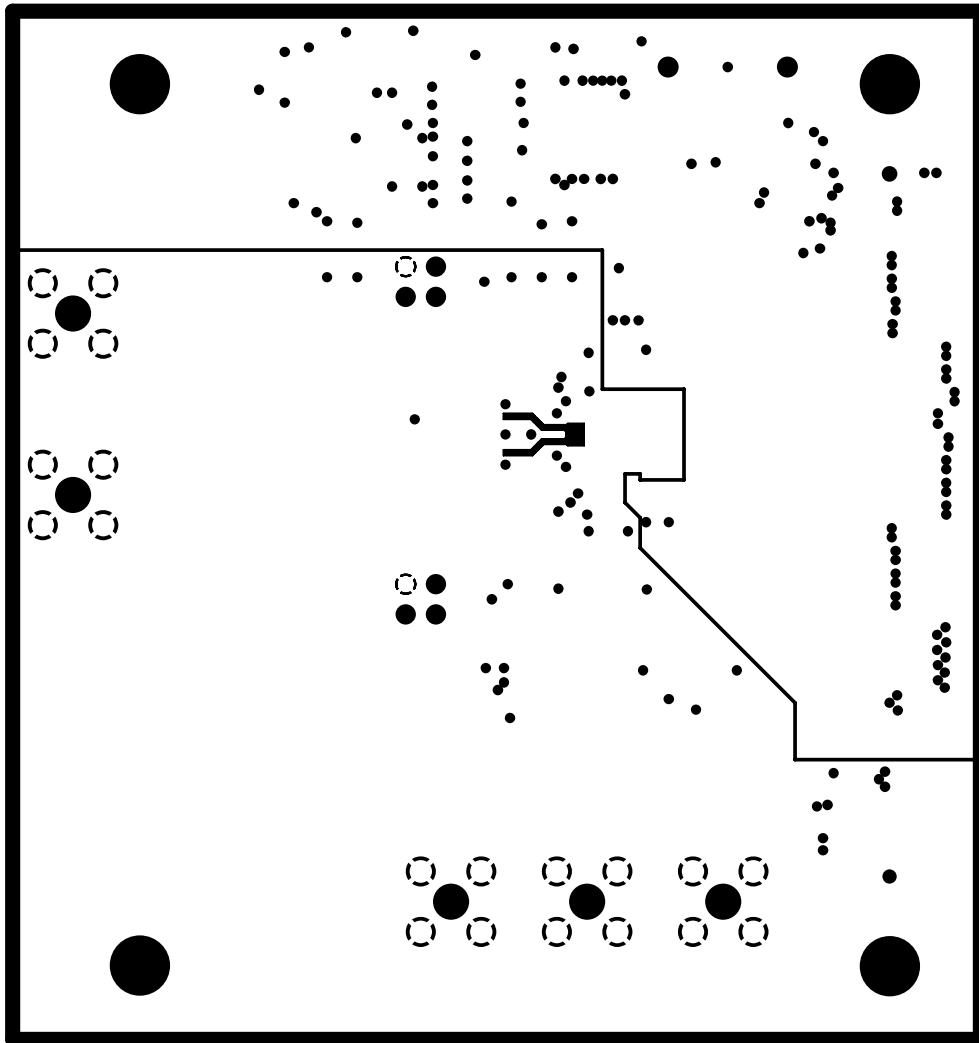


FIGURE 6. SPLIT GROUND PLANE

ISLA214P50IR72EV1Z Layers (Continued)

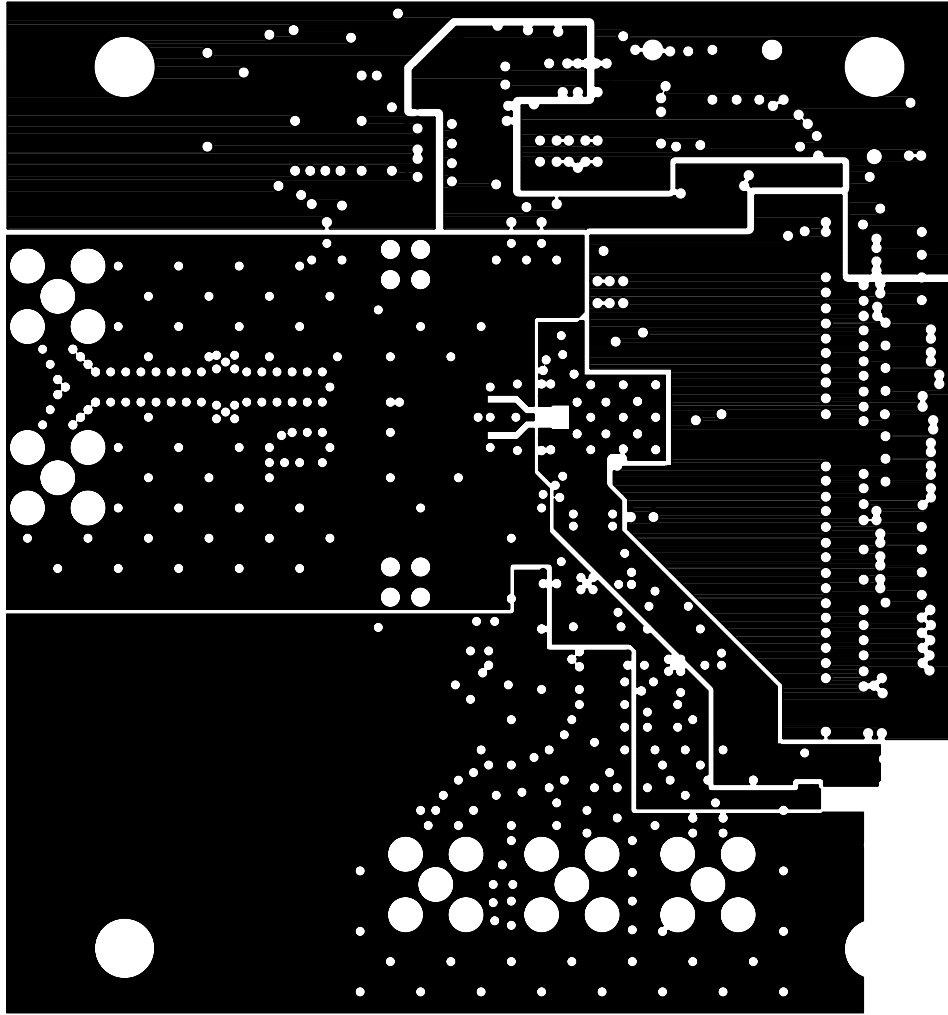


FIGURE 7. SPLIT POWER PLANE

ISLA214P50IR72EV1Z Layers (Continued)

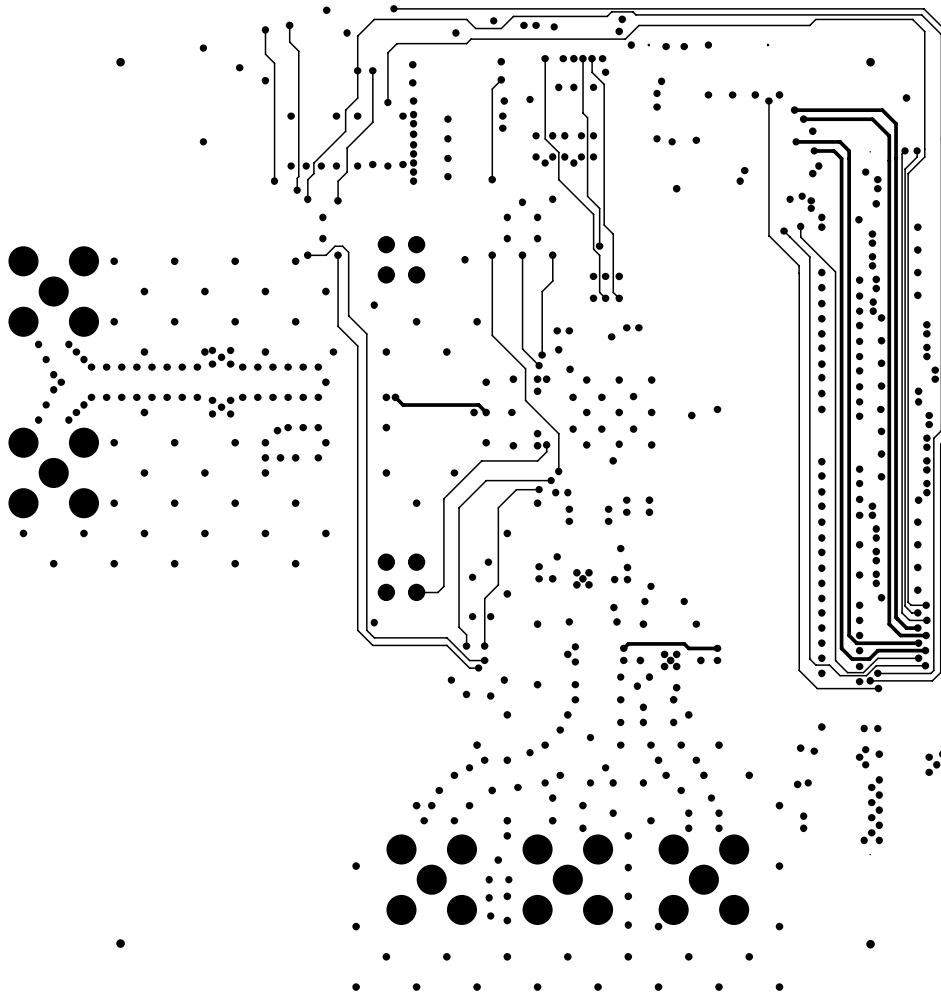


FIGURE 8. INNER LAYER ROUTING

ISLA214P50IR72EV1Z Layers (Continued)

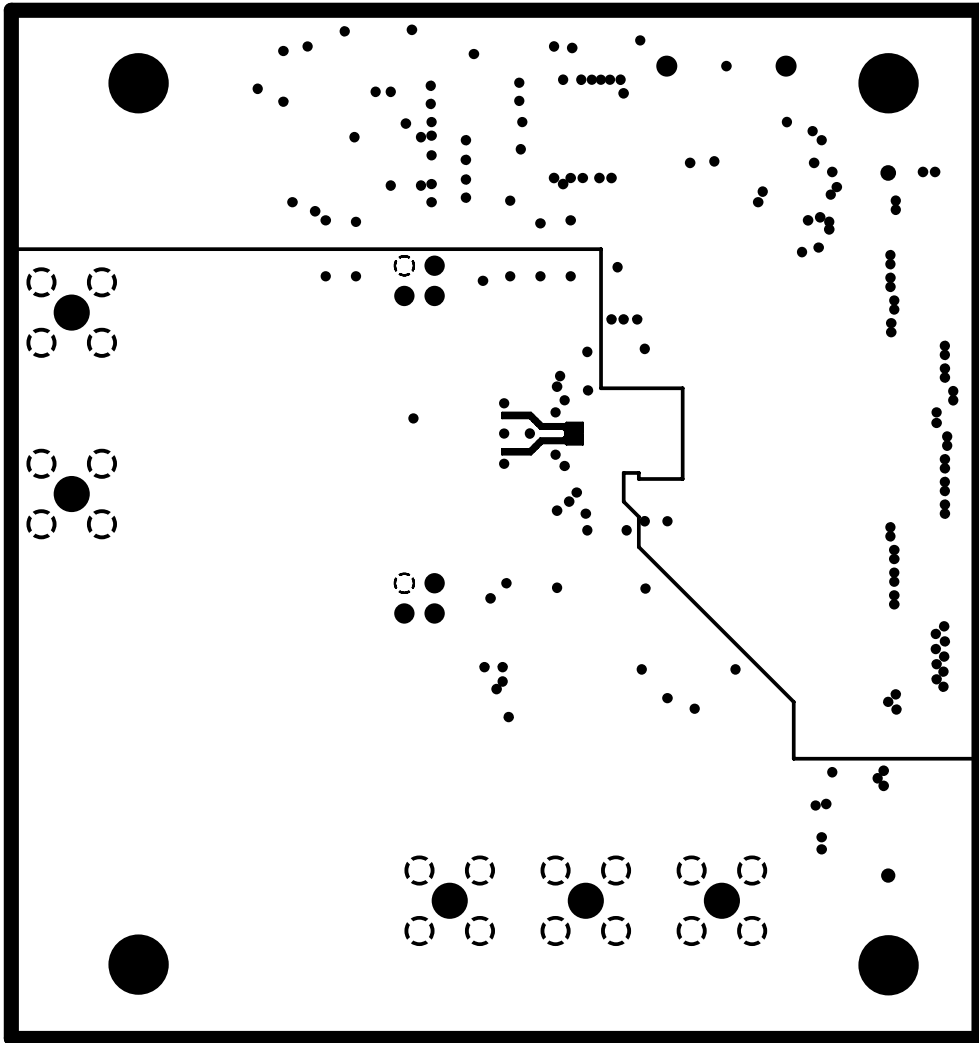


FIGURE 9. 2ND SPLIT GROUND PLANE

ISLA214P50IR72EV1Z Layers (Continued)

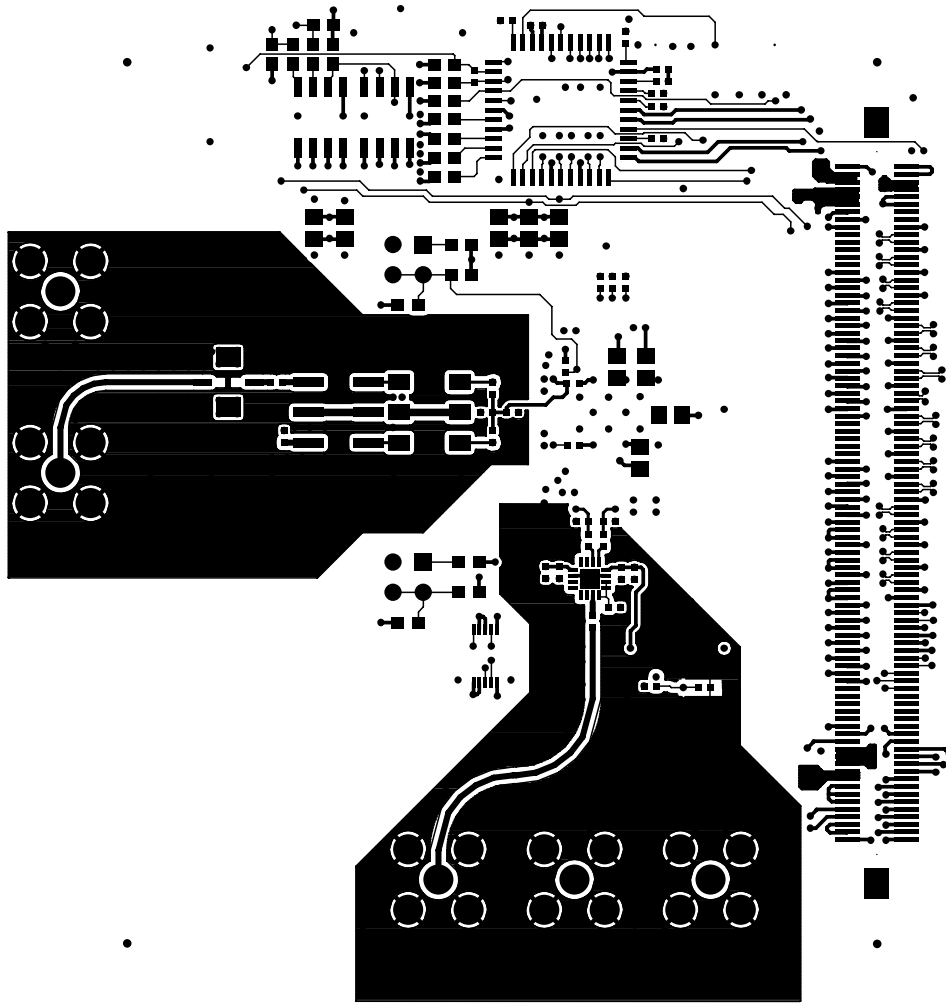


FIGURE 10. BOTTOM LAYER ROUTING

ISLA214P50IR72EV1Z

ISLA214P50IR72EV1Z Layers (Continued)

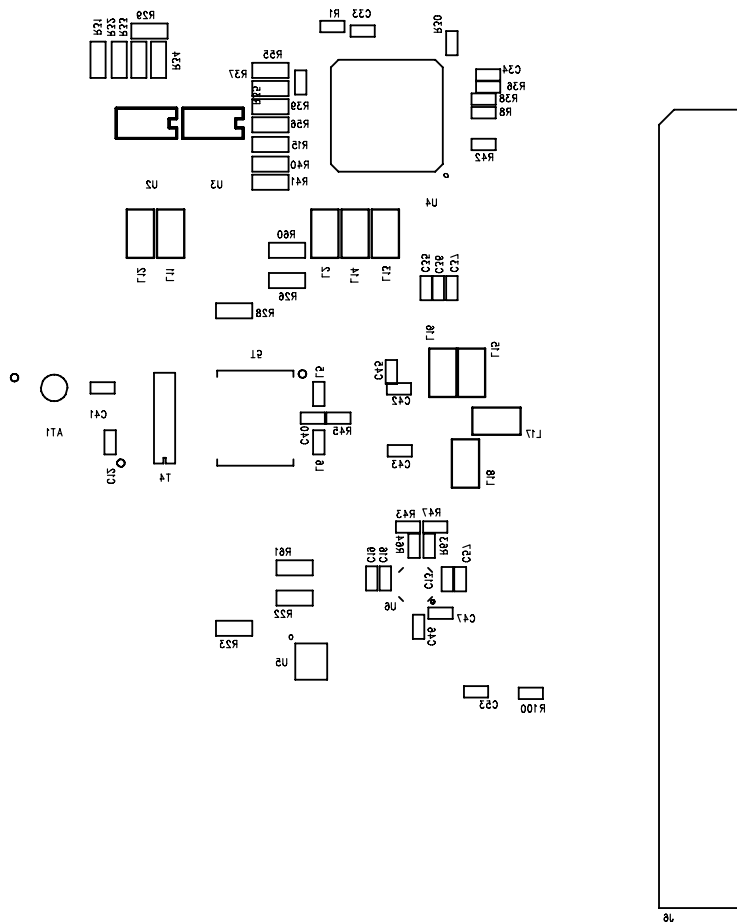


FIGURE 11. BOTTOM SILKSCREEN

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