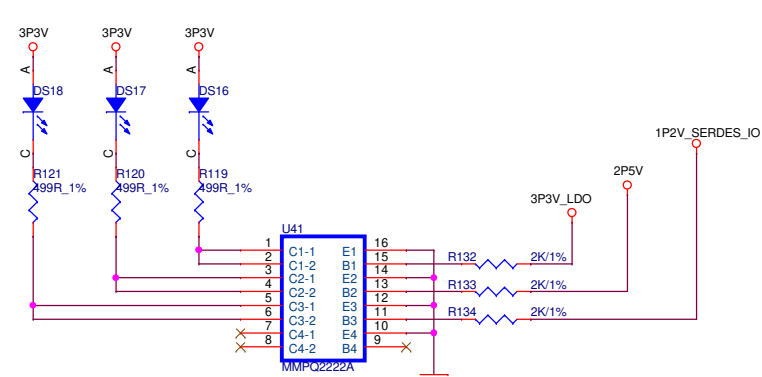
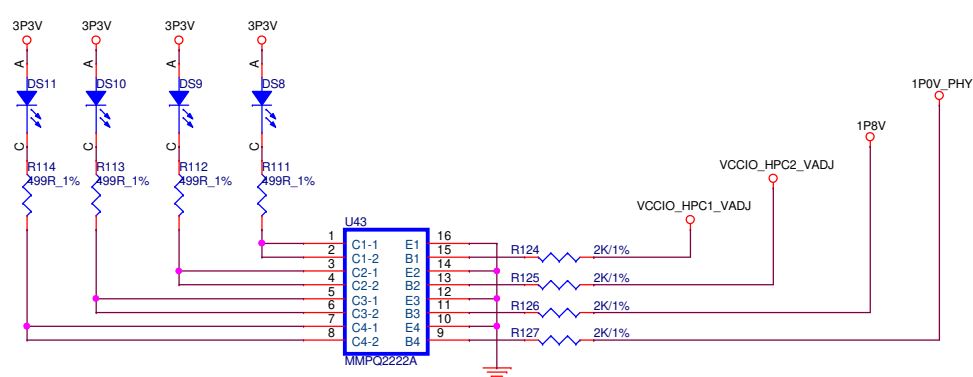
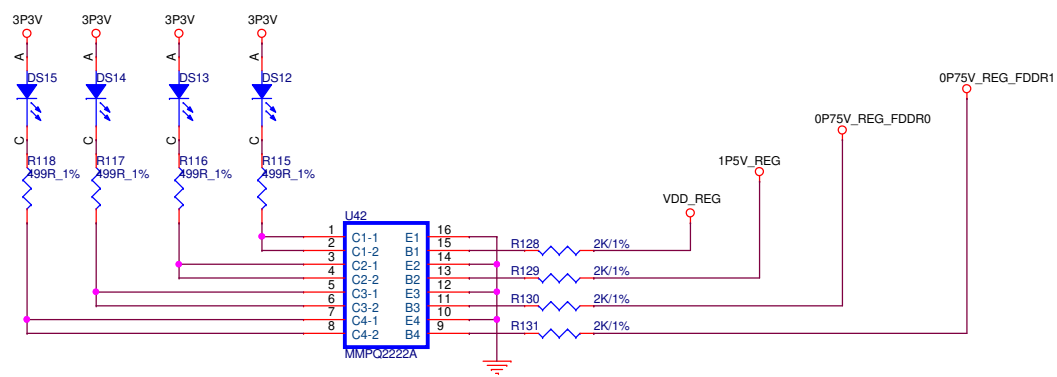
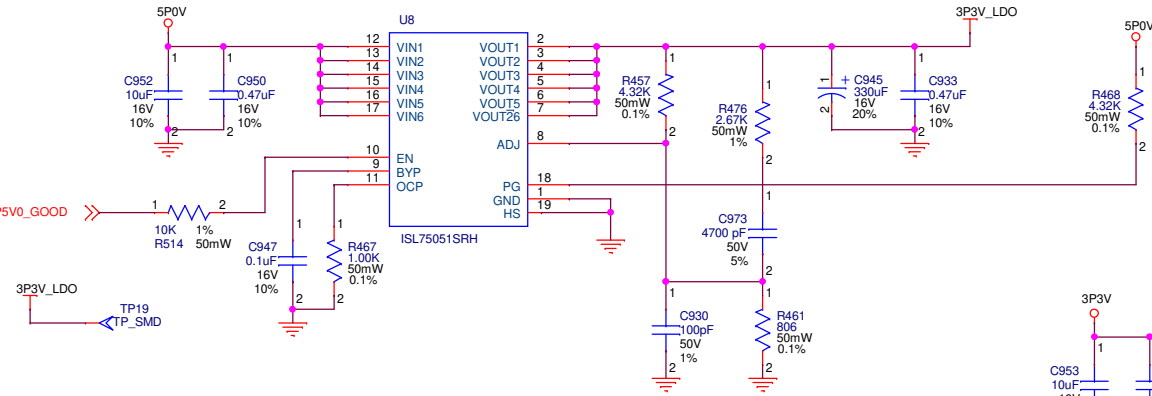


POWER LEDs

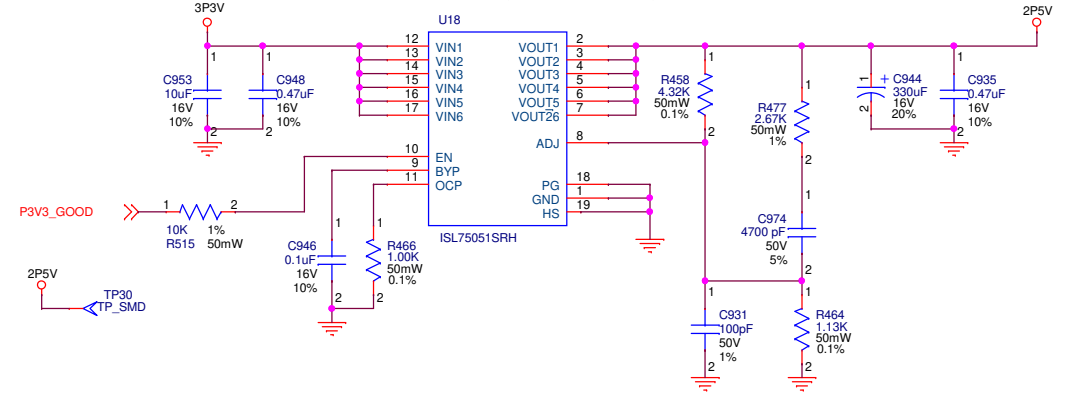


POWER SUPPLIES 6

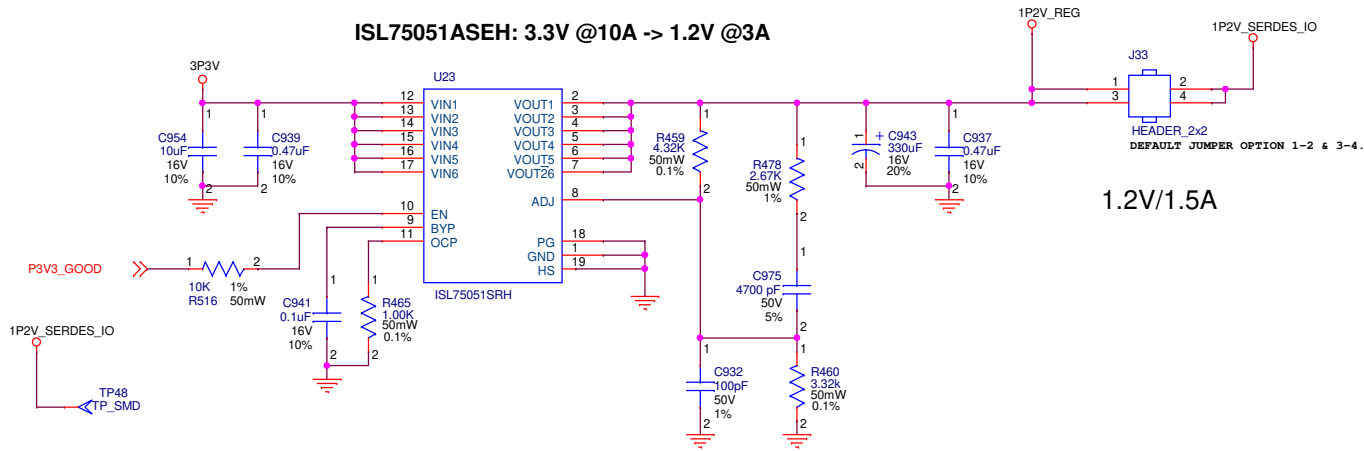
ISL75051ASEH: 5V @9A -> 3.3V @1A



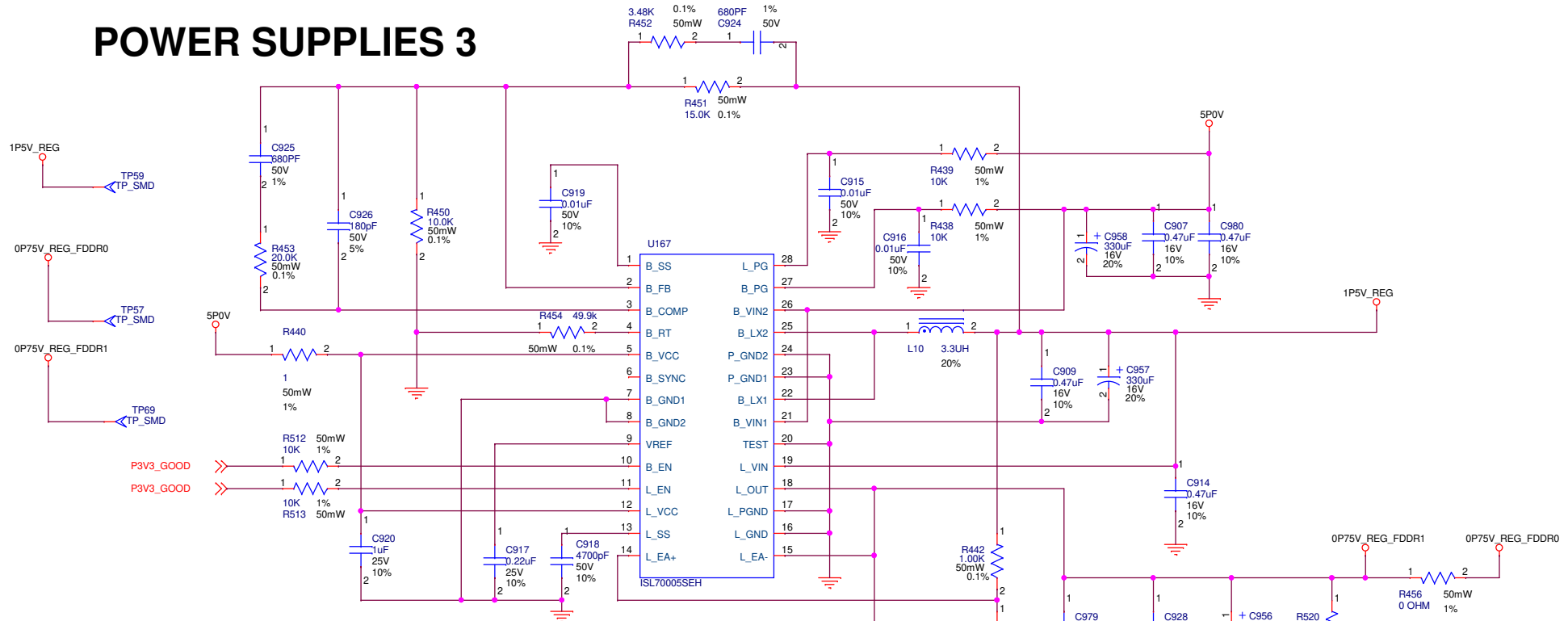
ISL75051ASEH: 3.3V @10A -> 2.5V @2A



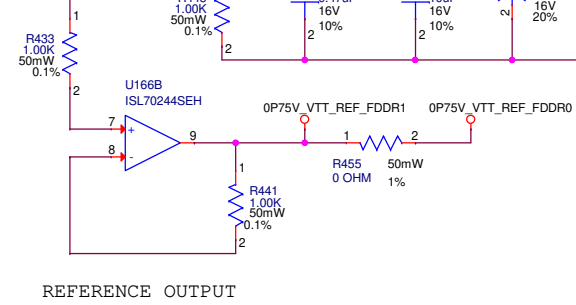
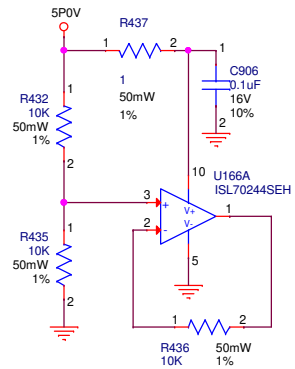
ISL75051ASEH: 3.3V @10A -> 1.2V @3A



POWER SUPPLIES 3

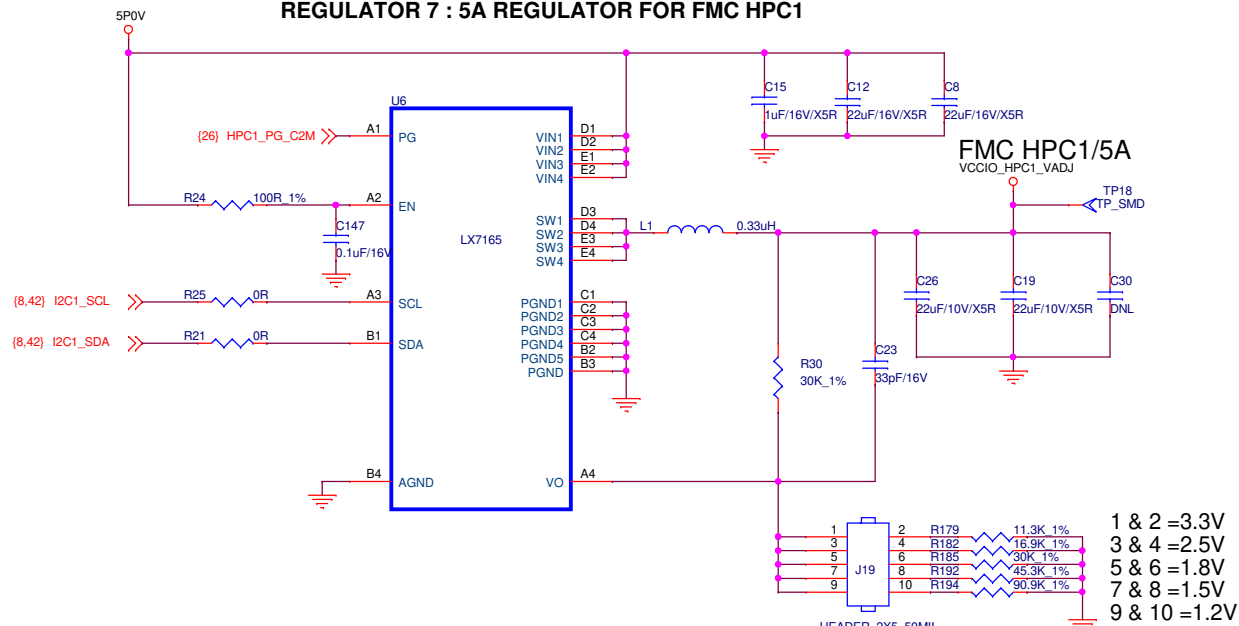


ISL70005: 5V @9A -> 1.5V @3A, and 0.75V @0A



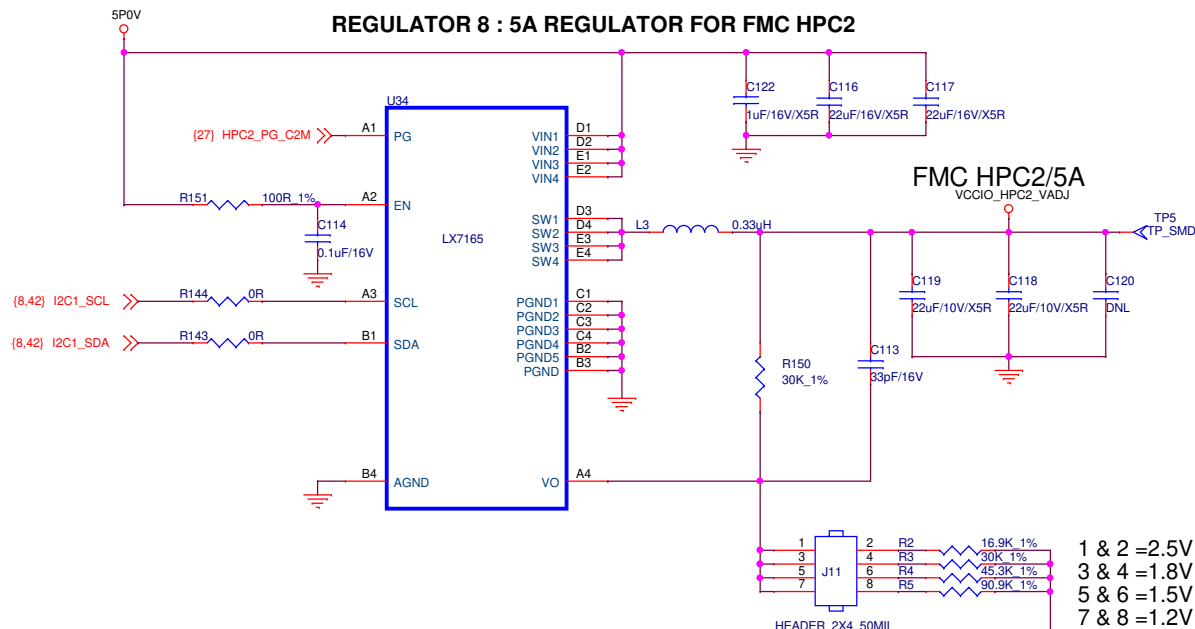
POWER SUPPLIES - 4

REGULATOR 7 : 5A REGULATOR FOR FMC HPC1



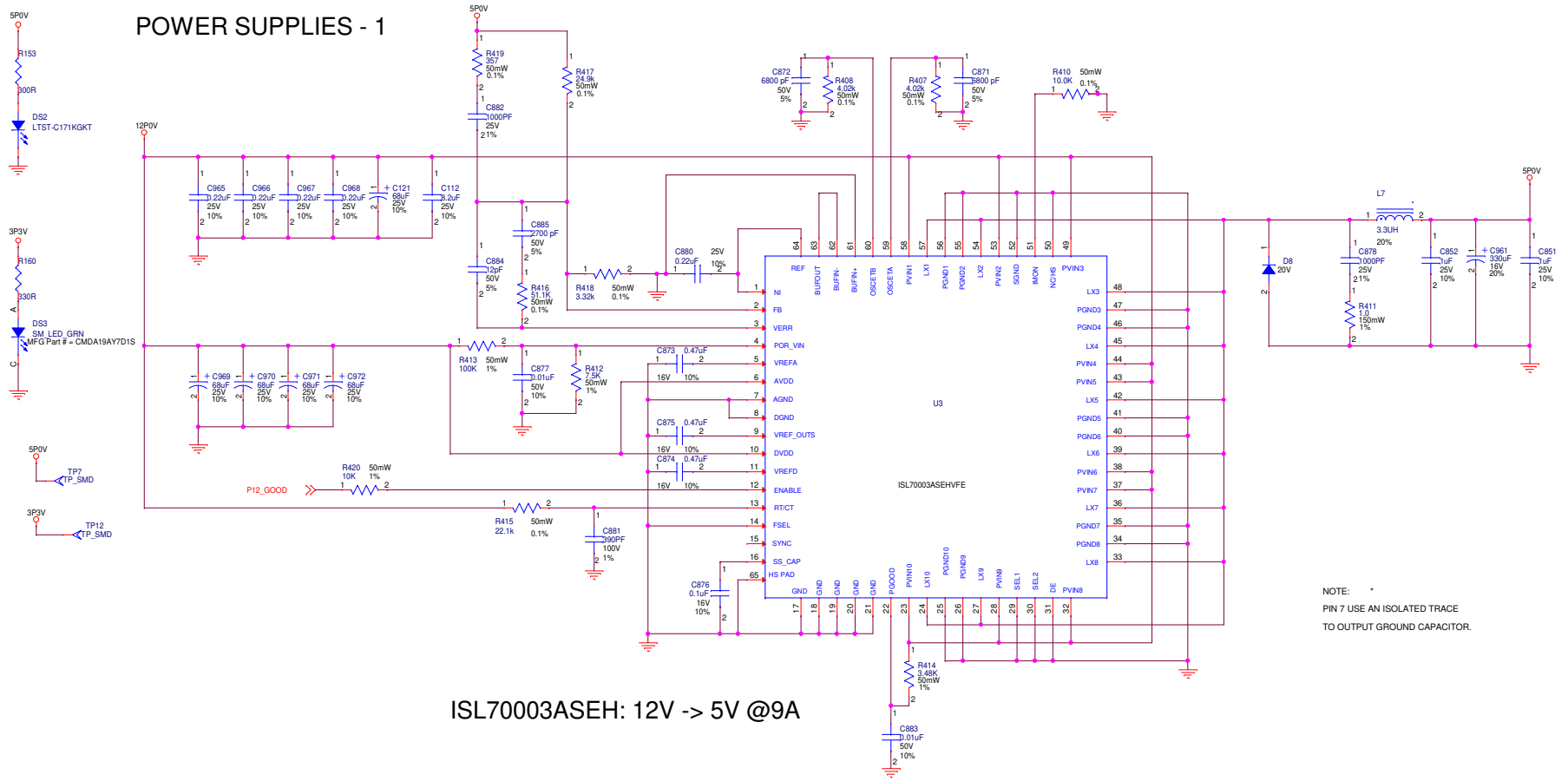
Jumper Default option 1 & 2 = 3.3V

REGULATOR 8 : 5A REGULATOR FOR FMC HPC2

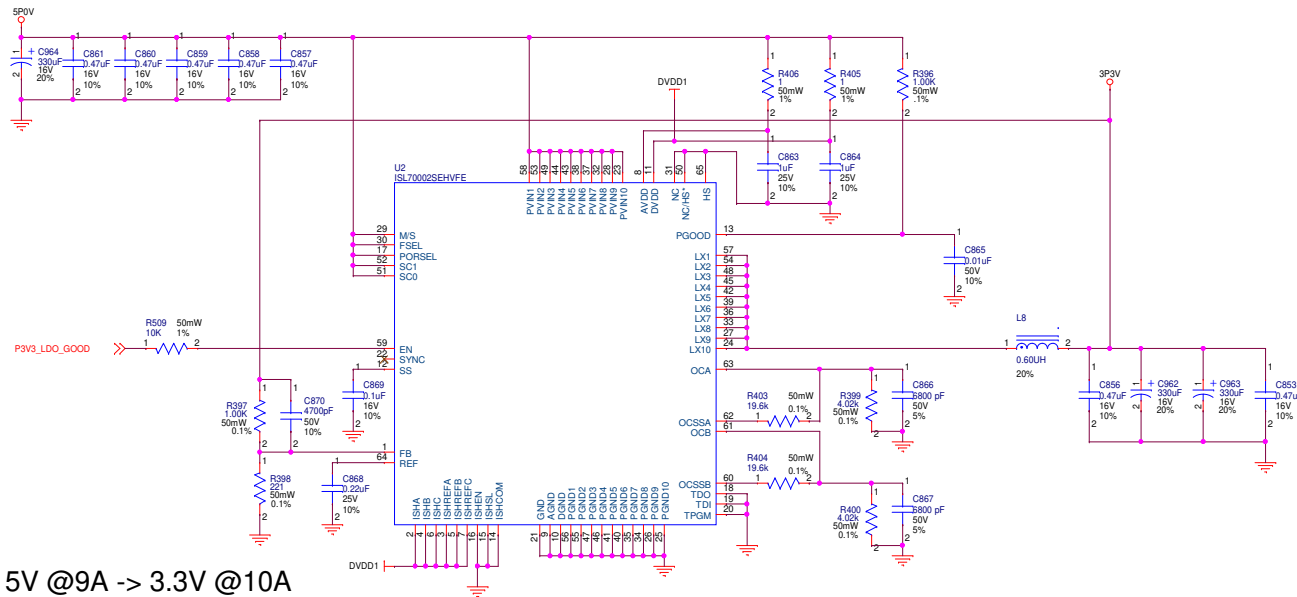


Jumper Default option 1 & 2 = 2.5V

POWER SUPPLIES - 1

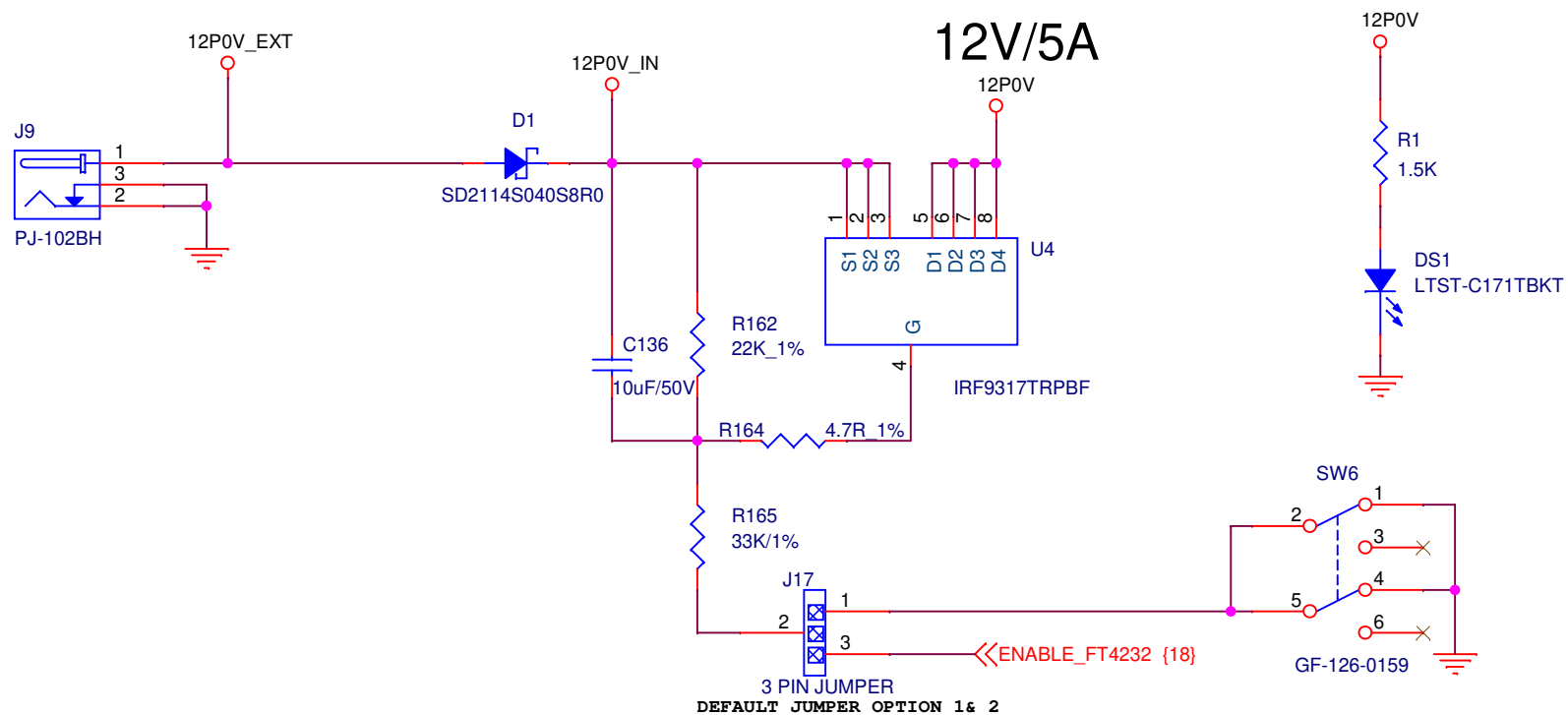


ISL70003ASEH: 12V -> 5V @9A

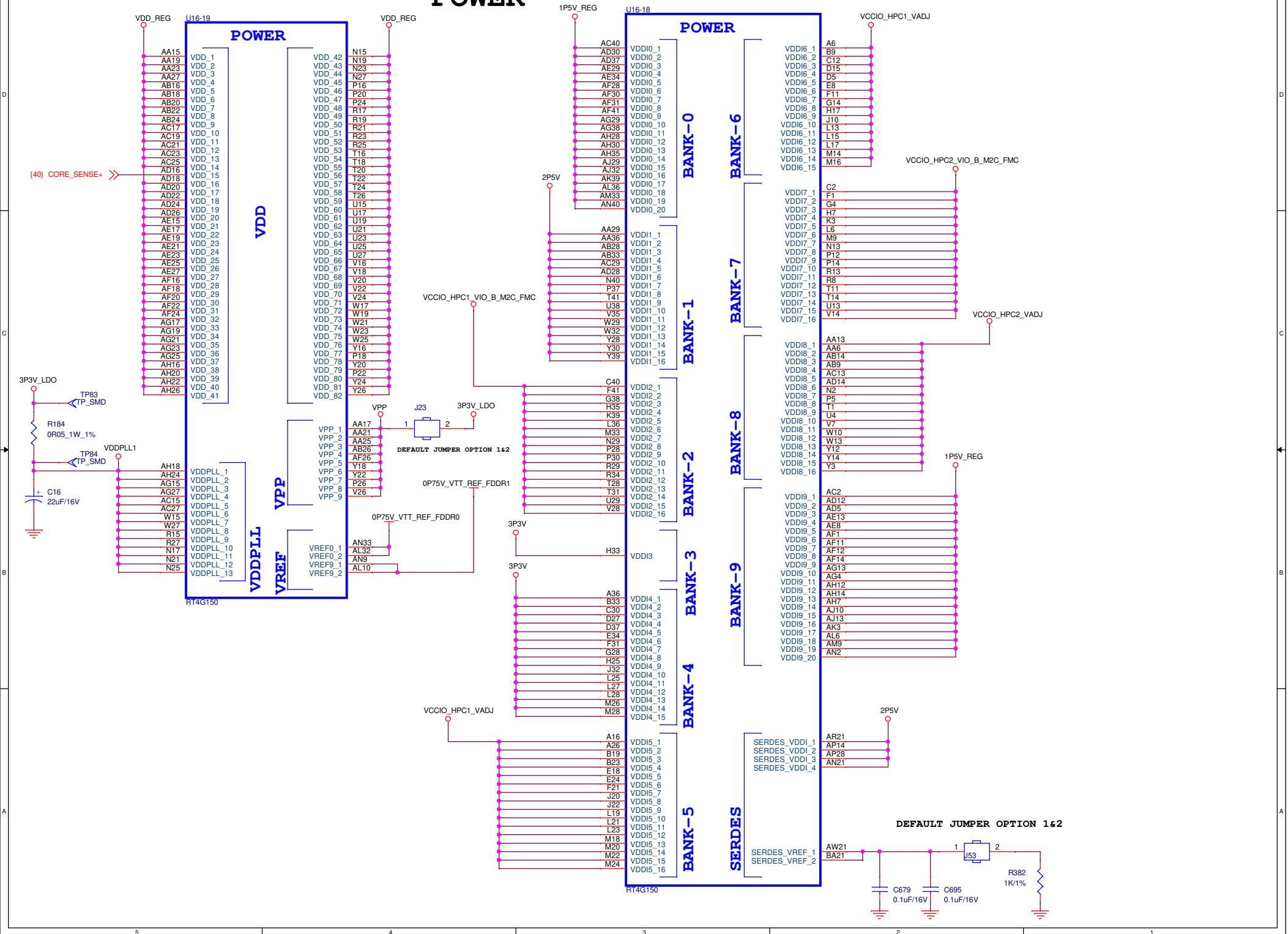


ISL70002SEH: 5V @9A -> 3.3V @10A

12V EXTERNAL SUPPLY

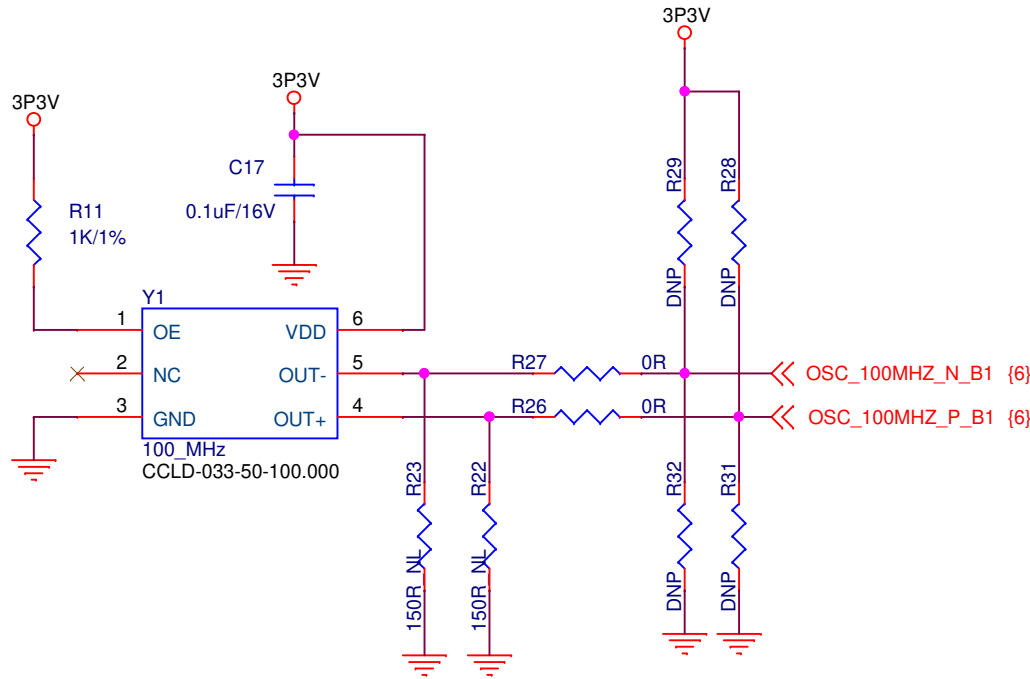


POWER



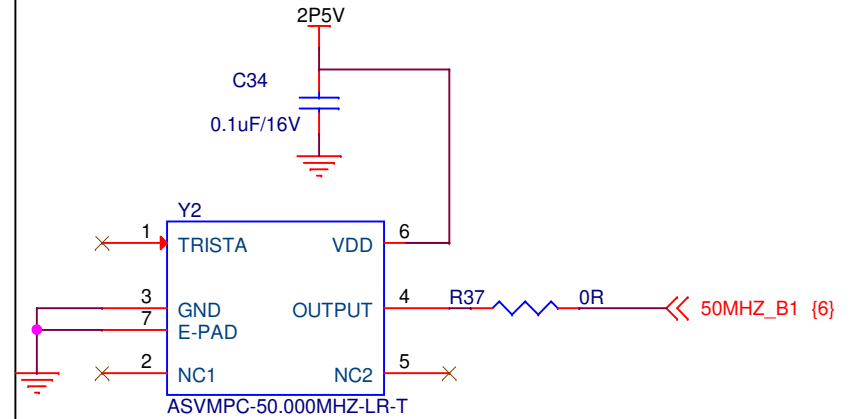
CLOCK CIRCUITRY

CLK -100MHz

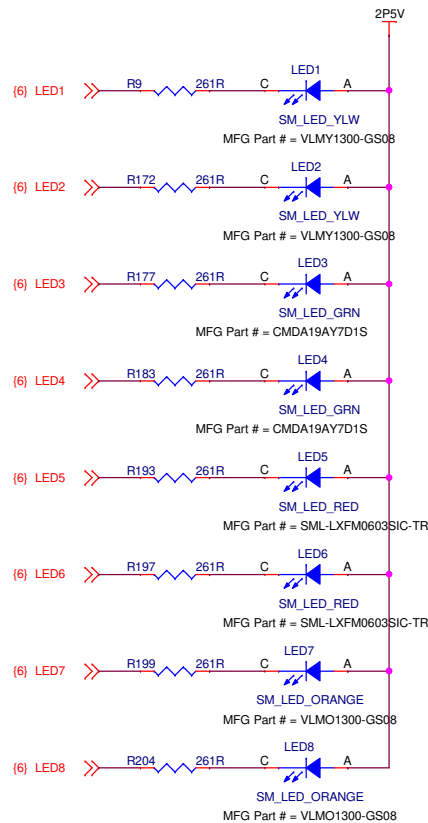
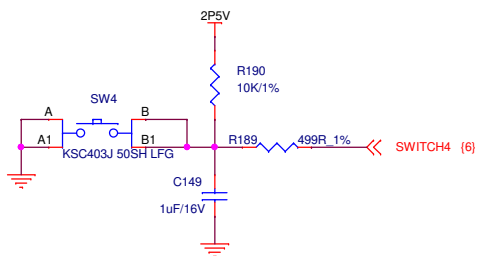
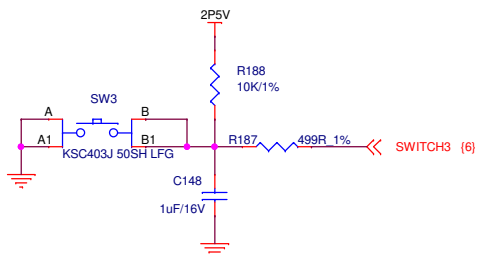
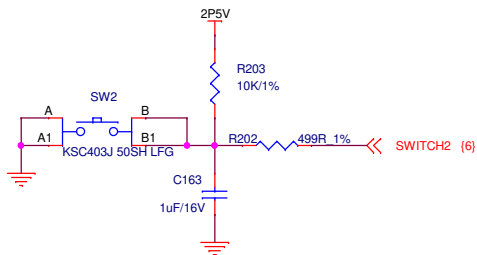
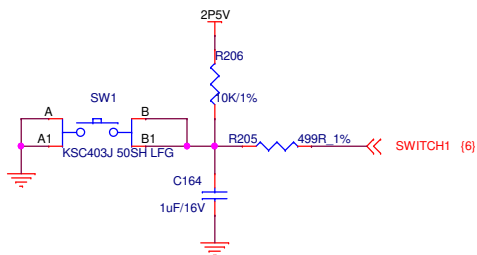


NOTE:
R23, R22, R29, R28, R32, R31 are not populated on board. They were placed for internal debugging purpose

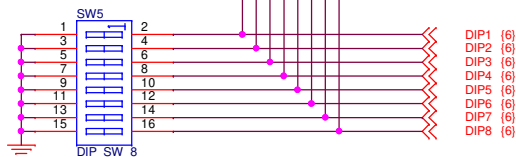
CLK -50MHz



DEBUG CIRCUITRY



SWITCH POSITION	LOGIC LEVEL
ON	GND
OFF	LOGIC1

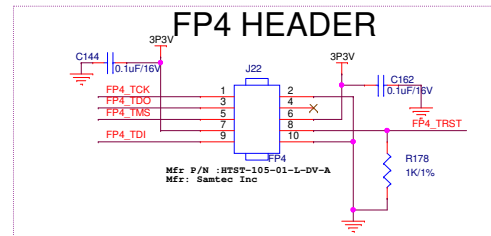
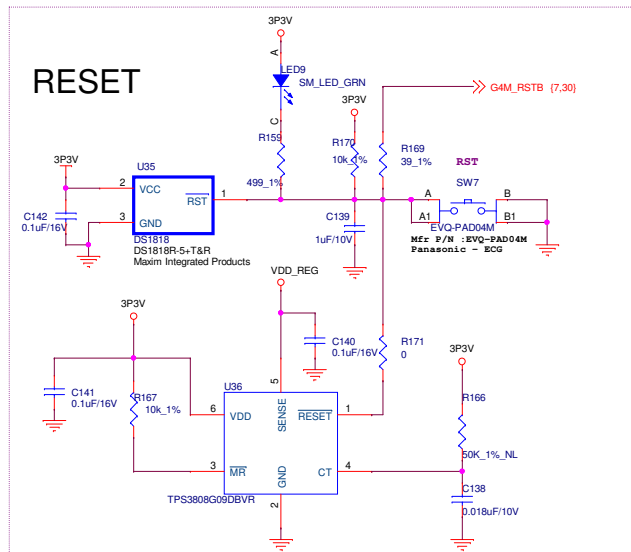
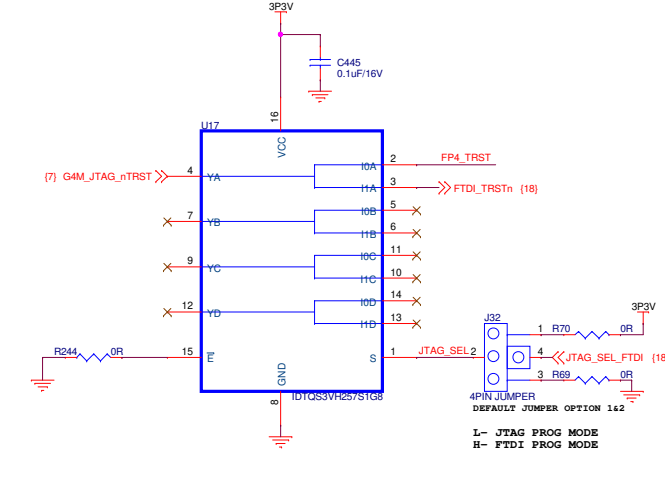
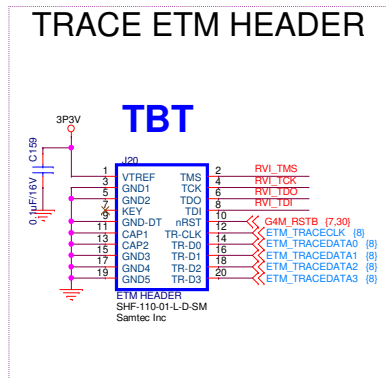
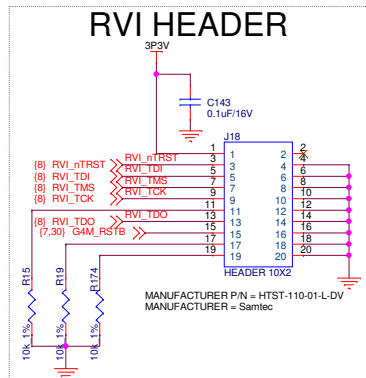
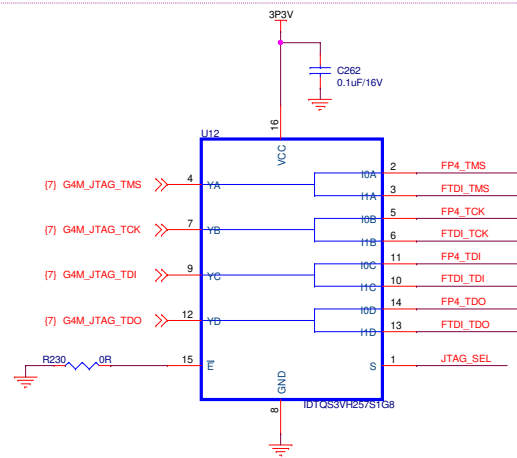
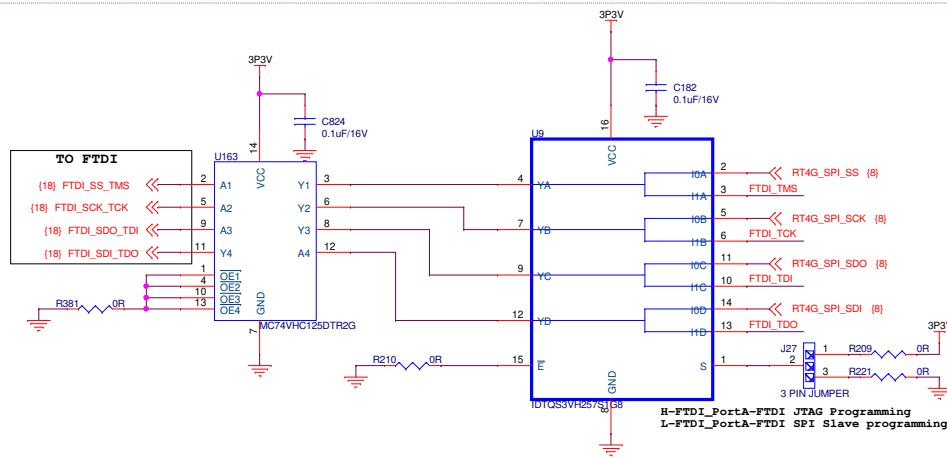


NET NAME	FPGA PIN NAME	FPGA PIN NO
SWITCH1	MSIOD68NB1	AA30
SWITCH2	MSIOD65PB1	AB31
SWITCH3	MSIOD68PB1	AB30
SWITCH4	MSIOD65NB1	AB32

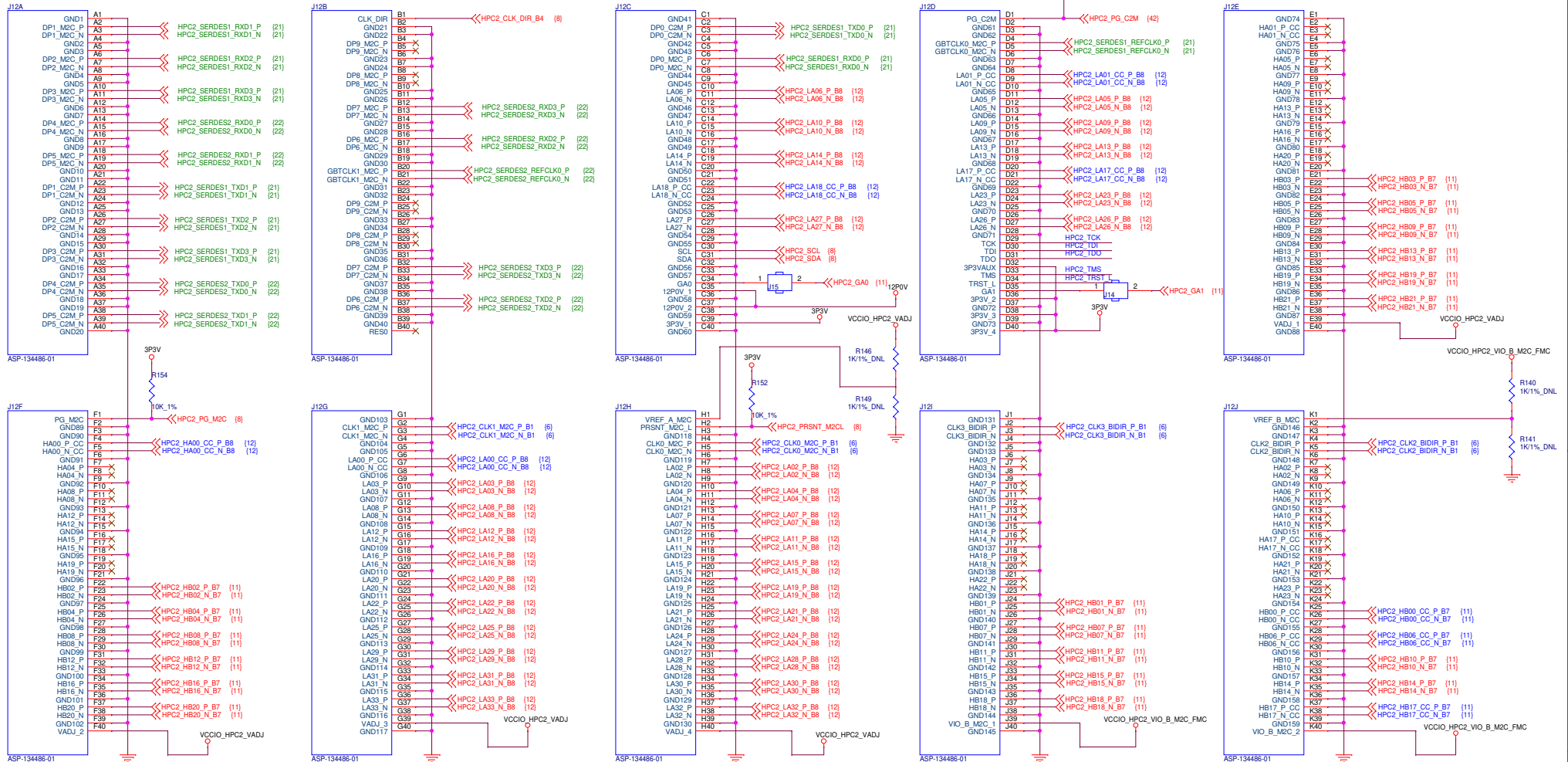
NET NAME	FPGA PIN NAME	FPGA PIN NO
LED1	MSIOD62PB1	W35
LED2	MSIOD46PB1	W34
LED3	MSIOD47PB1	V30
LED4	MSIOD46NB1	W33
LED5	MSIOD38PB1	T33
LED6	MSIOD41NB1	U35
LED7	MSIOD37PB1	R36
LED8	MSIOD38NB1	T34

NET NAME	FPGA PIN NAME	FPGA PIN NO
DIP1	MSIOD57NB1	AA33
DIP2	MSIOD56PB1	Y31
DIP3	MSIOD56NB1	W31
DIP4	MSIOD47NB1	W30
DIP5	MSIOD42NB1	V33
DIP6	MSIOD42PB1	V34
DIP7	MSIOD41PB1	U34
DIP8	MSIOD69PB1	W36

PROGRAMING CIRCUITRY



FMC CONNECTOR-HPC2

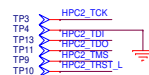


DECOUPLING CAPACITORS

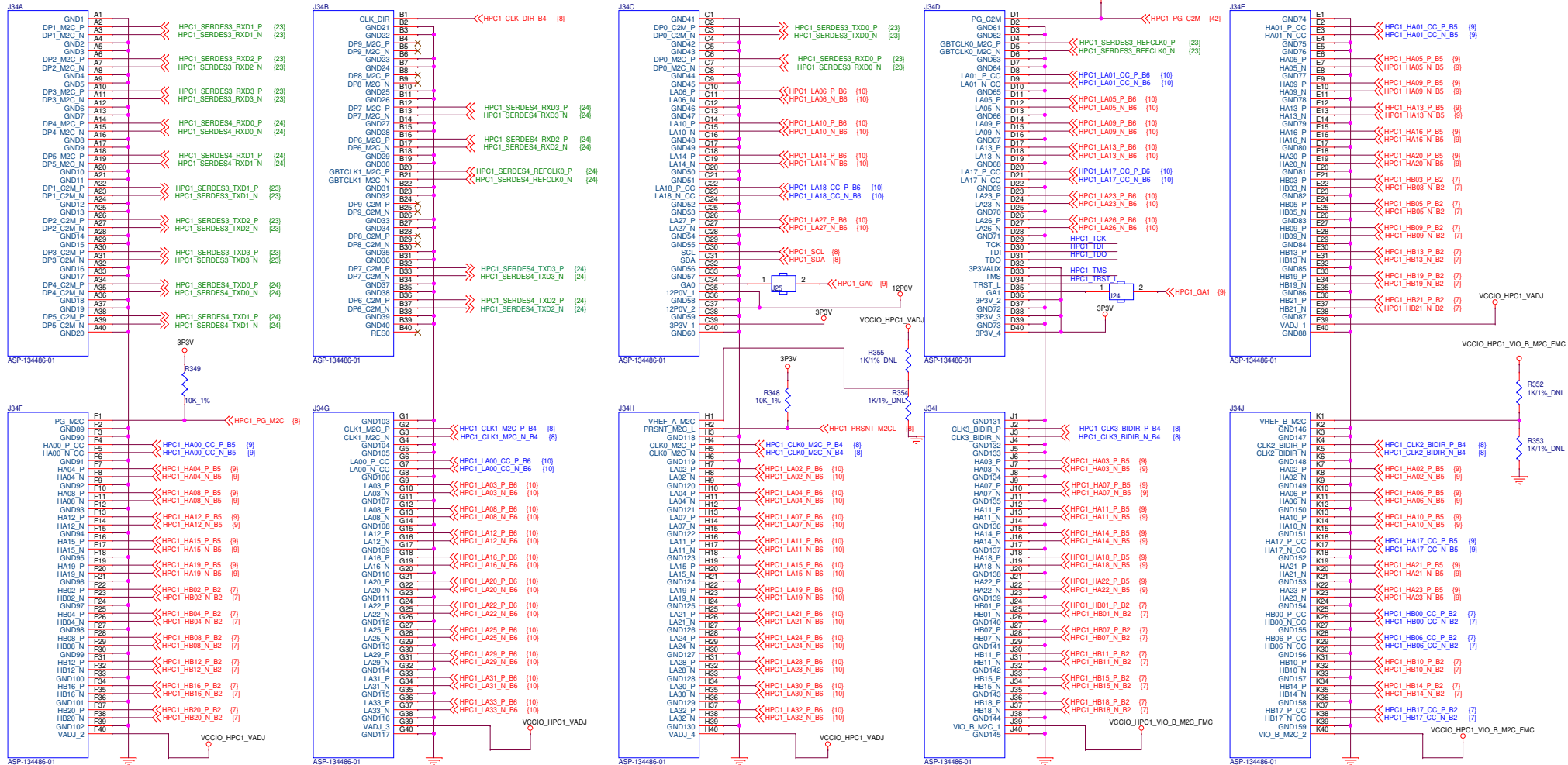


NOTE:

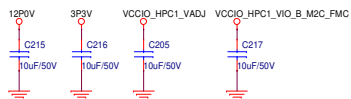
- 2.The Supporting Voltages of FMC HPC2(VCCIO HPC2_VADJ) are 1.2V,1.5V,1.8V and 2.5V.



FMC CONNECTOR-HPC1

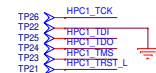


DECOUPLING CAPACITORS

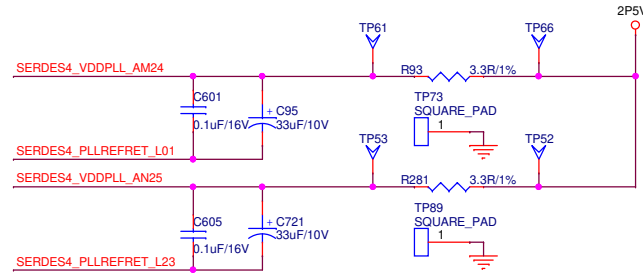
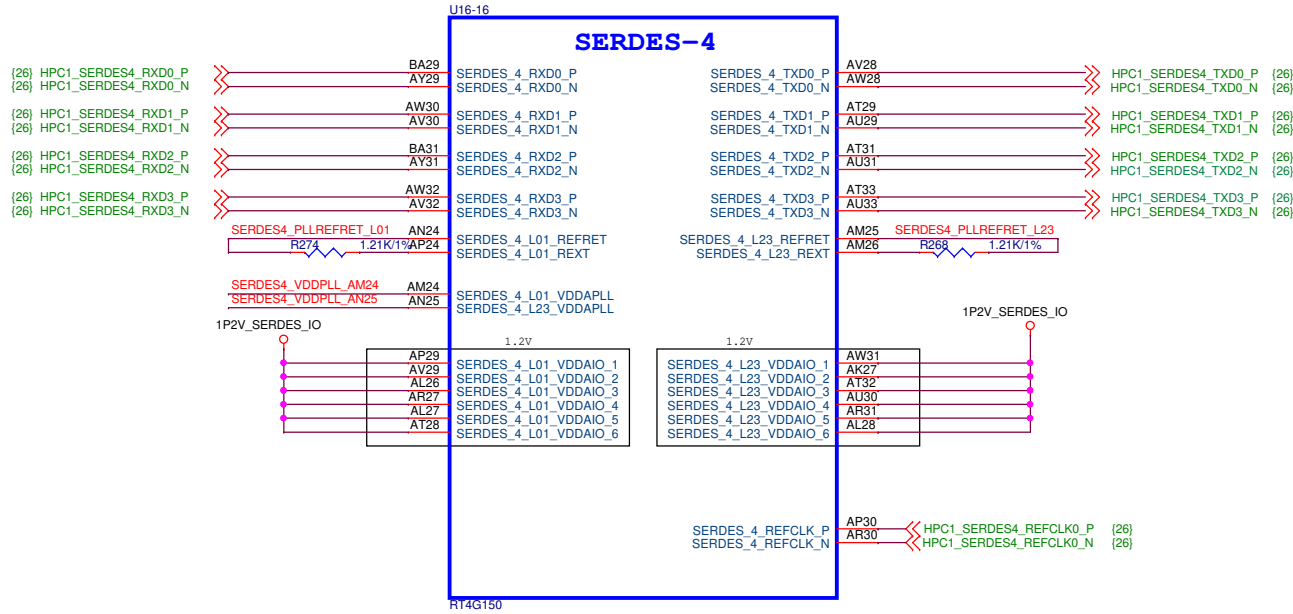


NOTE:

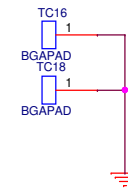
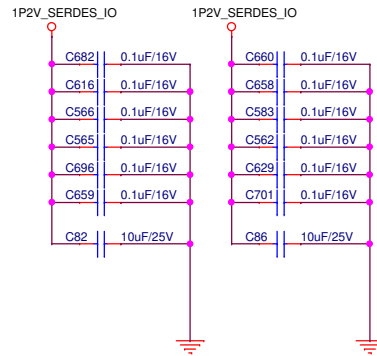
- 1.FMC HPC1 LA & HA bank IO's support maximum of 3.3V.
- 2.FMC HPC1 HB bank IO's support maximum of 2.5V.
- 3.The Supporting Voltages of FMC HPC1(VCCIO_HPC1_VADJ) are 1.2V,1.5V,1.8V, 2.5V and 3.3V.



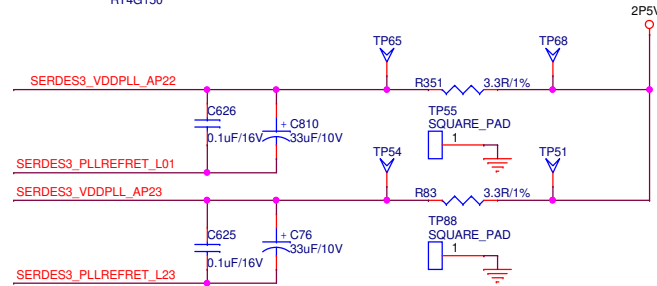
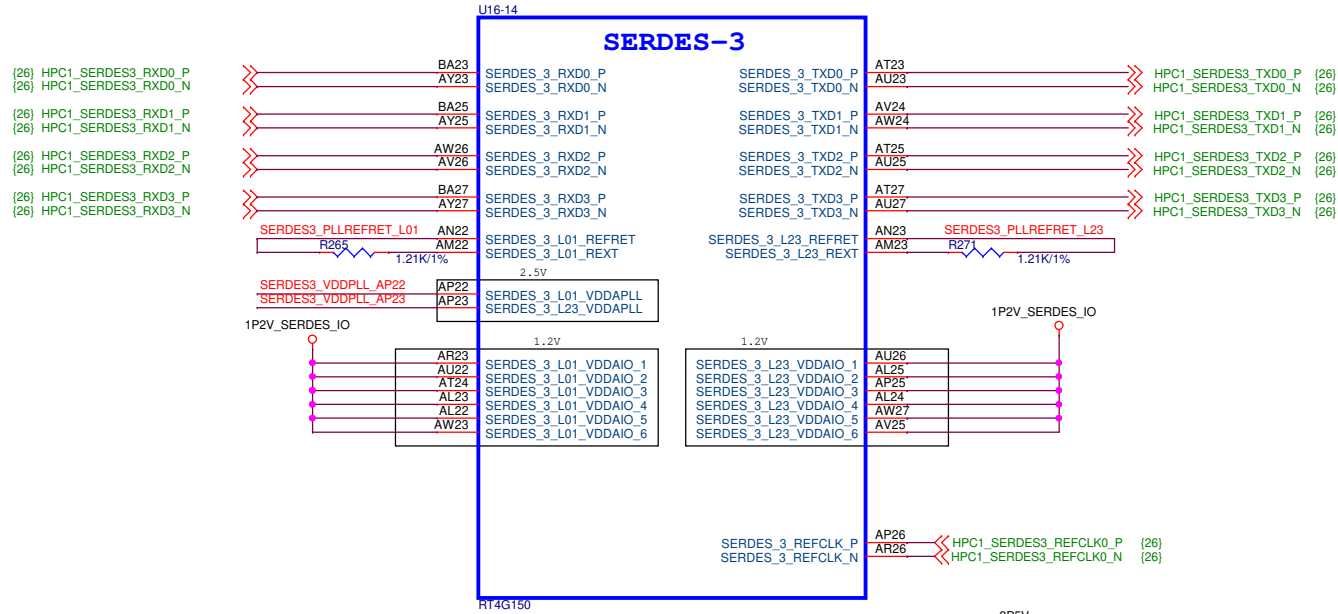
SERDES 4



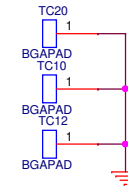
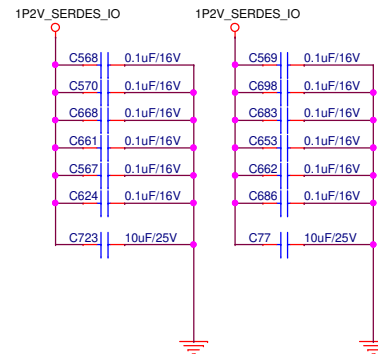
SERDES4-DECOUPLING CAPACITORS



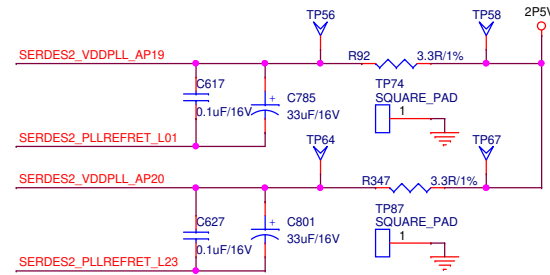
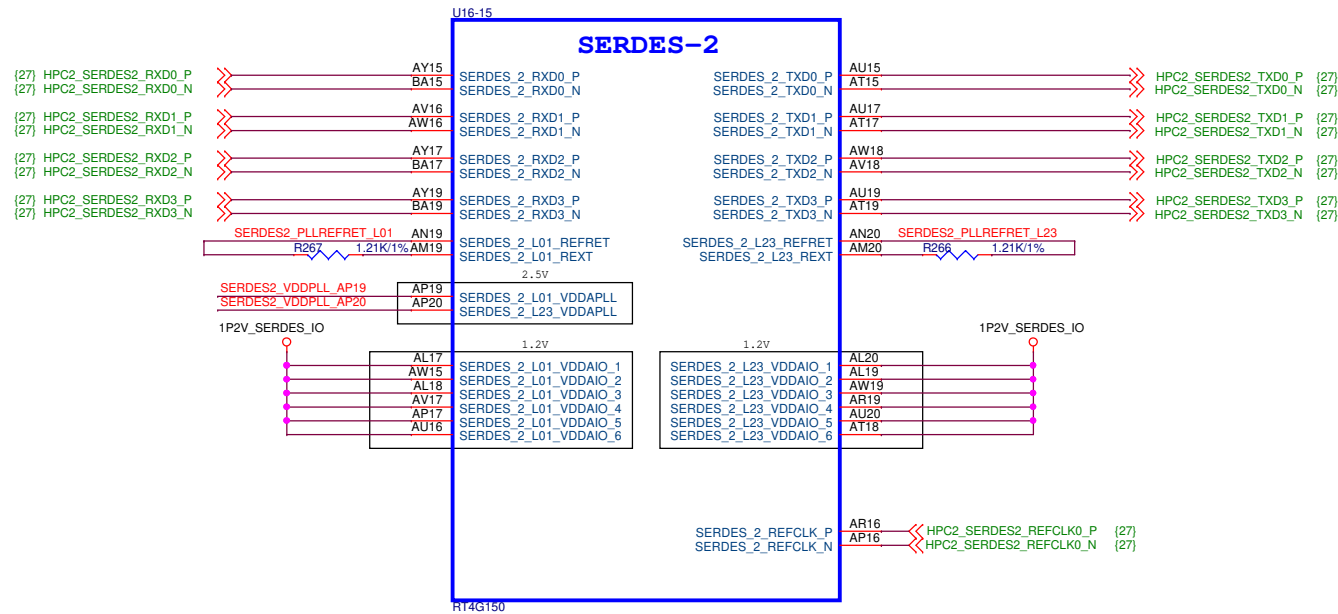
SERDES 3



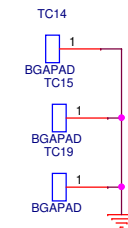
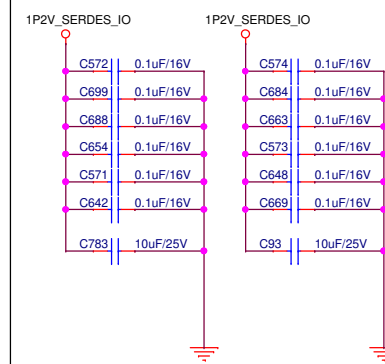
SERDES3-DECOUPLING CAPACITORS



SERDES 2



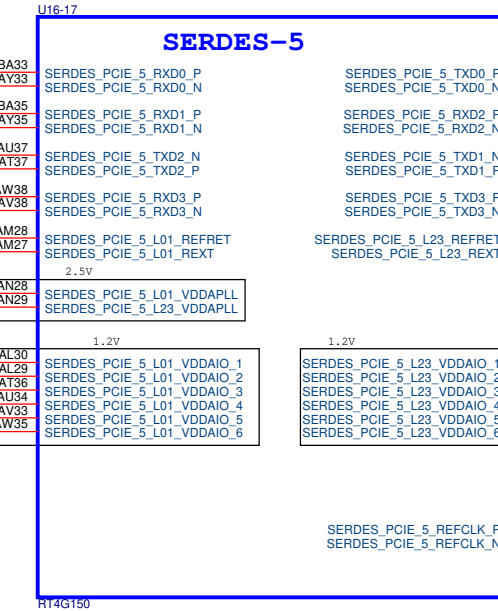
SERDES2-DECOUPLING CAPACITORS



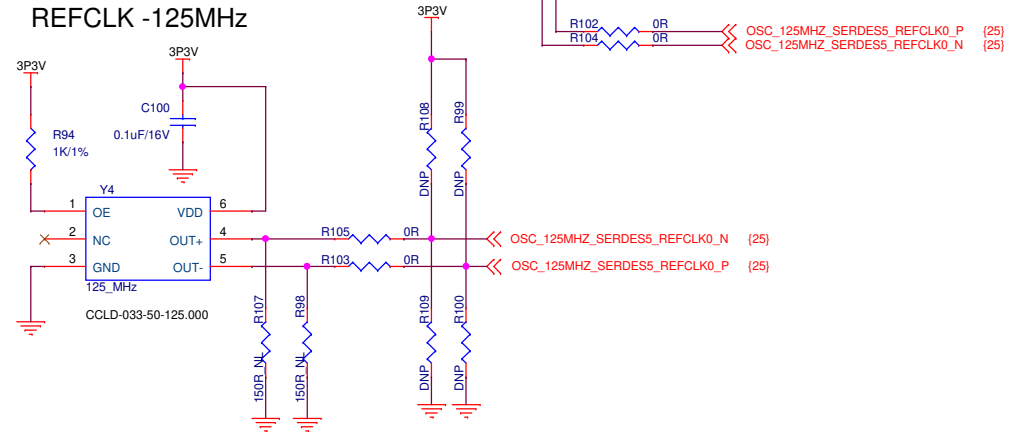
SERDES 5

TRACE LENGTH SHOULD BE 6 INCHES
(17) P0_S_OUTP
(17) P0_S_OUTN

TRACE LENGTH SHOULD BE 6 INCHES
(17) P0_S_INP
(17) P0_S_INN

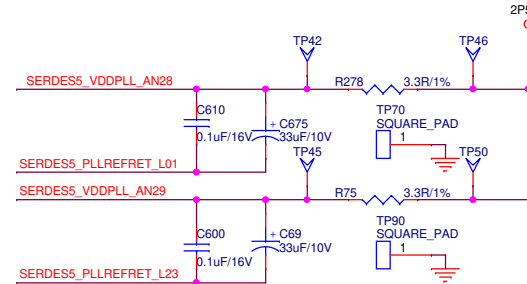
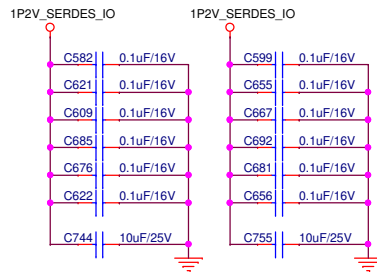


REFCLK -125MHz

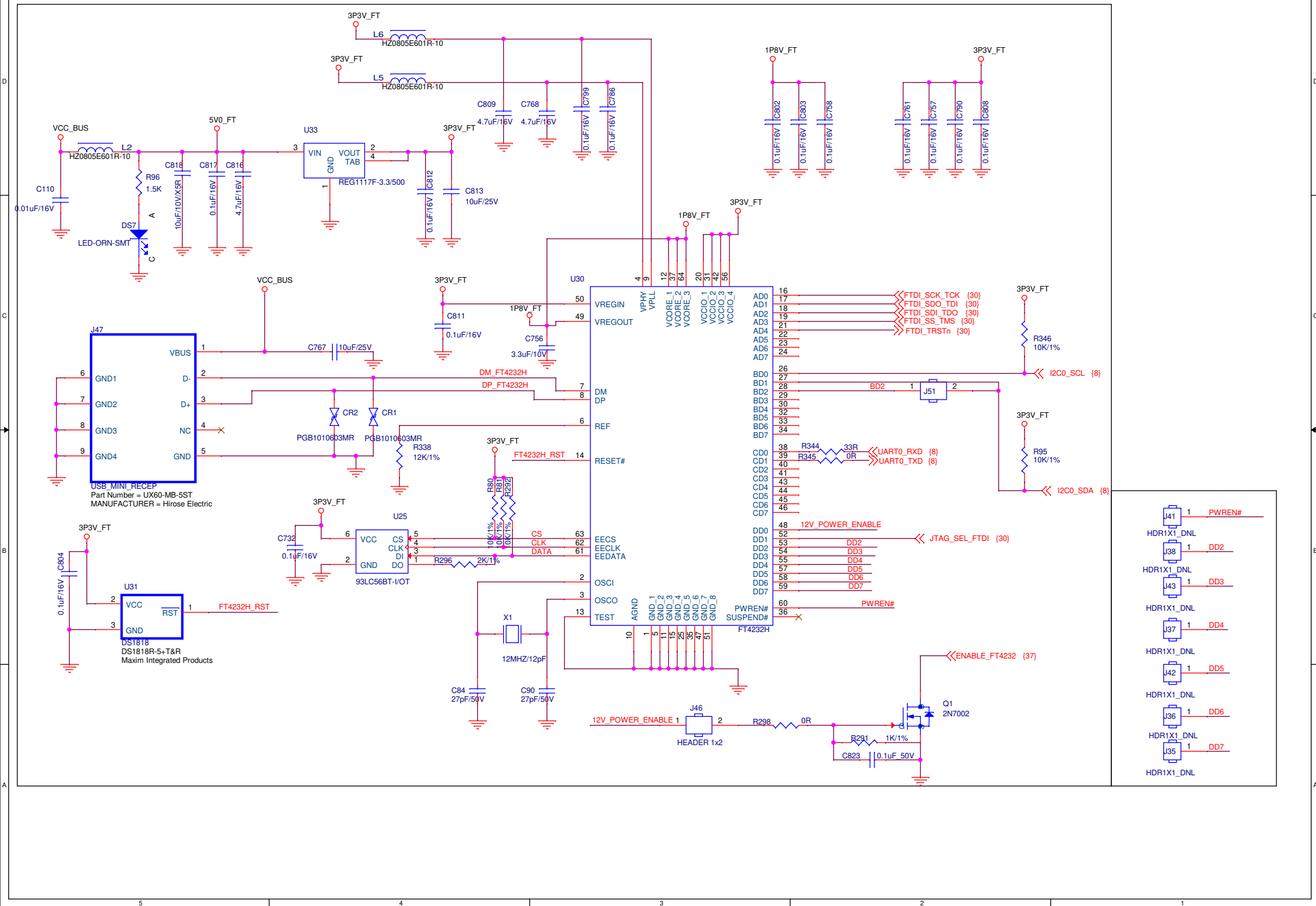


NOTE:
R107, R98, R109, R100, R108, R99 are not populated on board. They were placed for internal debugging purpose

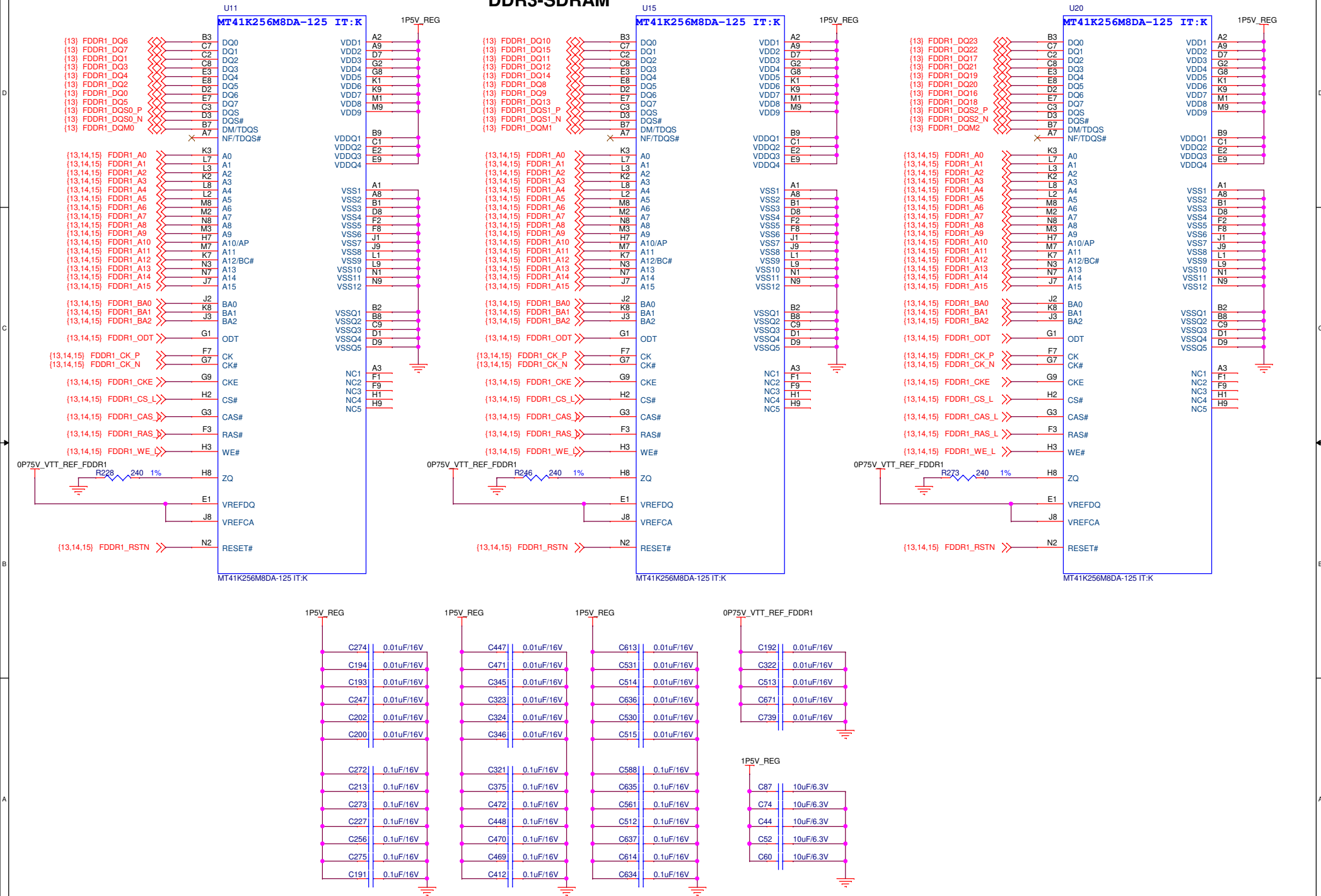
SERDESS-DECOUPLING CAPACITORS



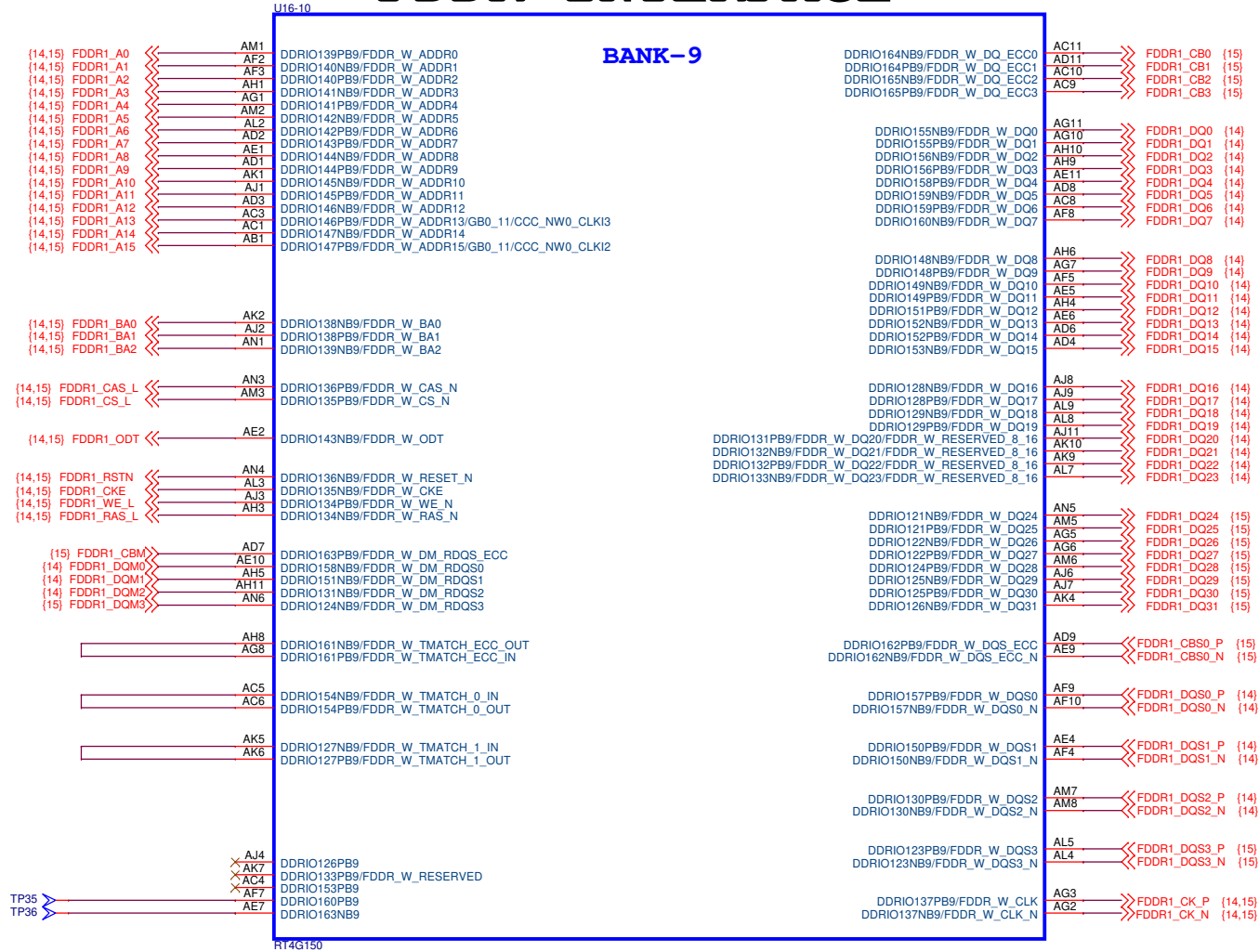
FT4232H CIRCUITRY



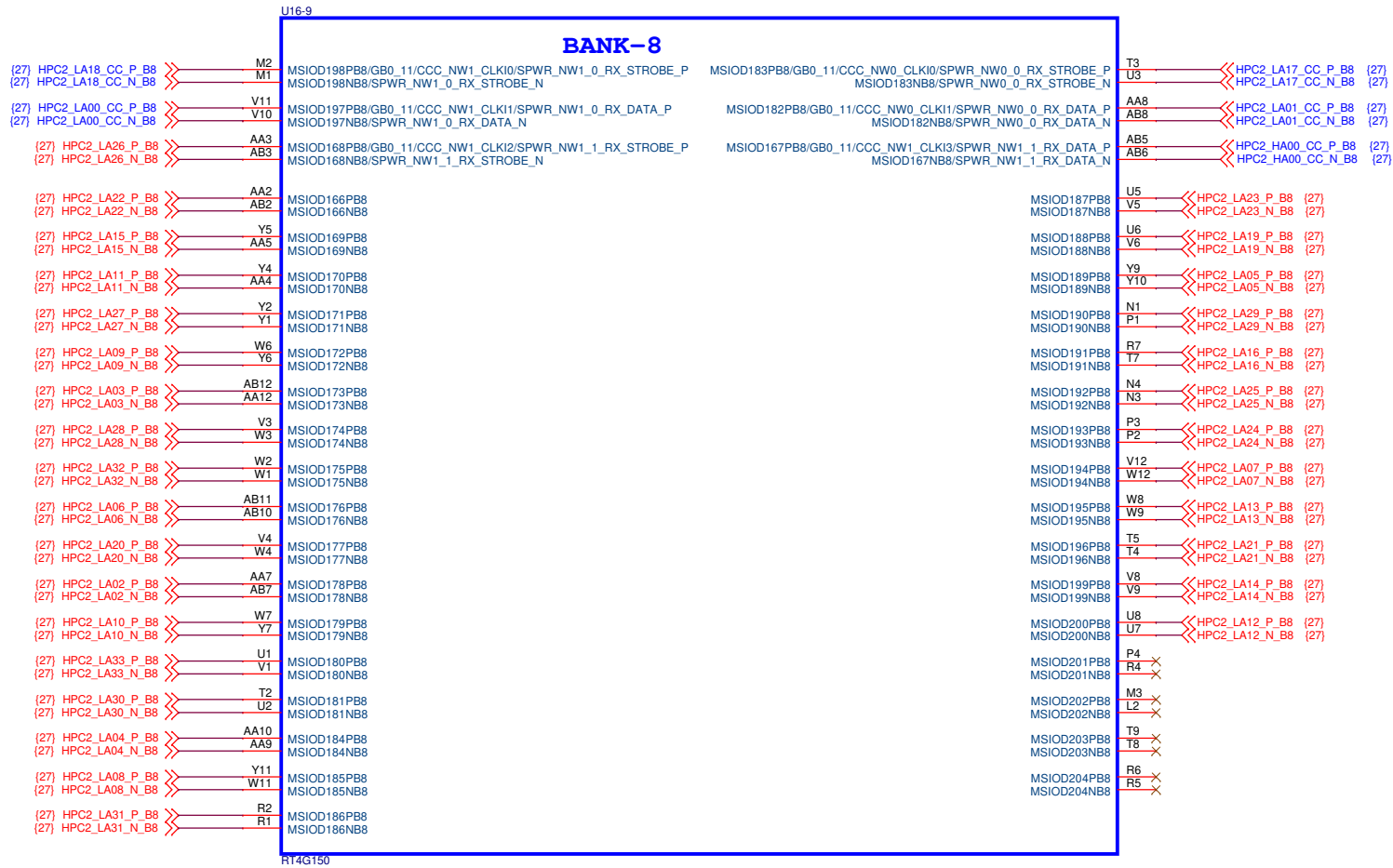
DDR3-SDRAM



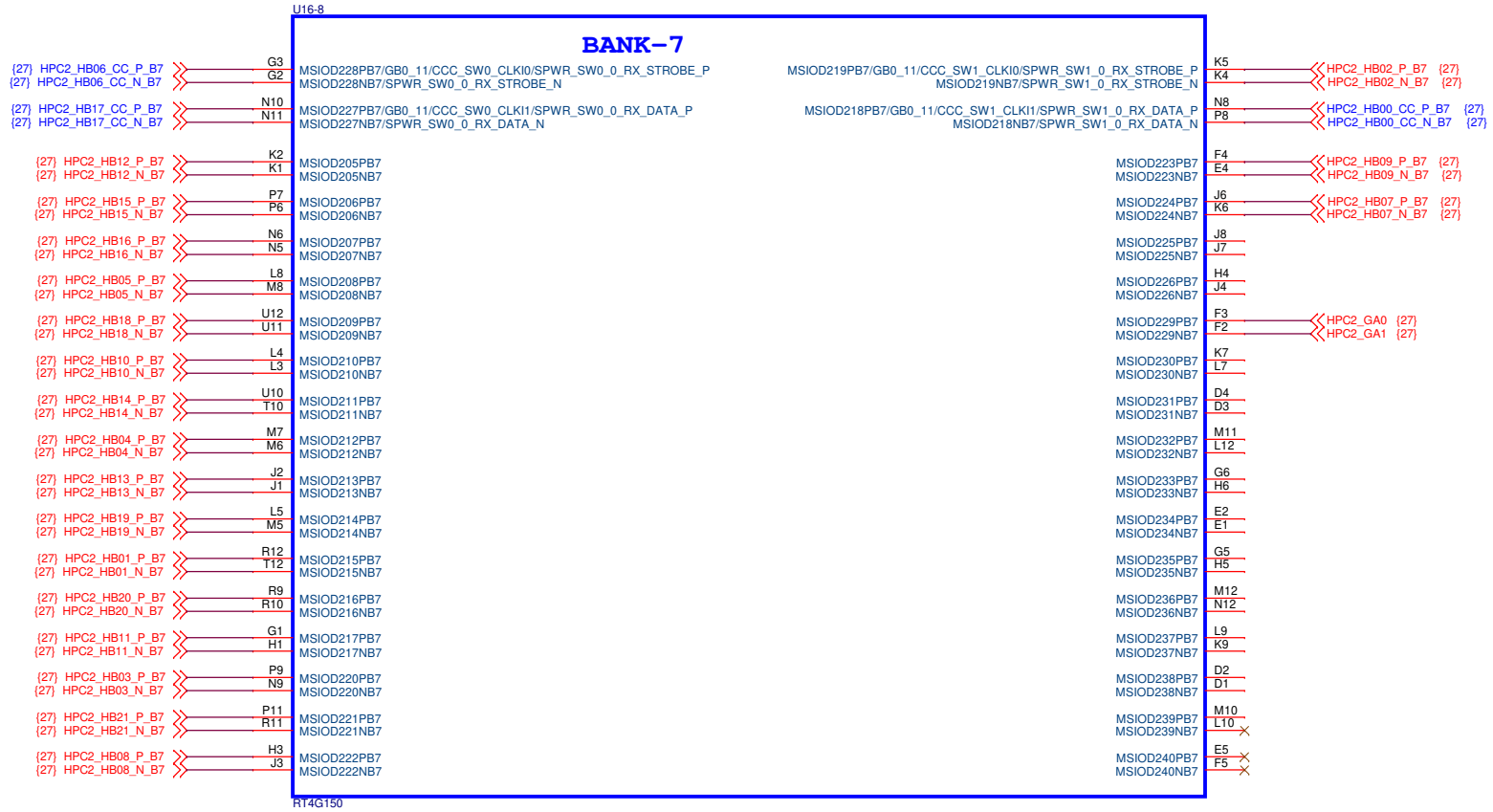
FDDR INTERFACE



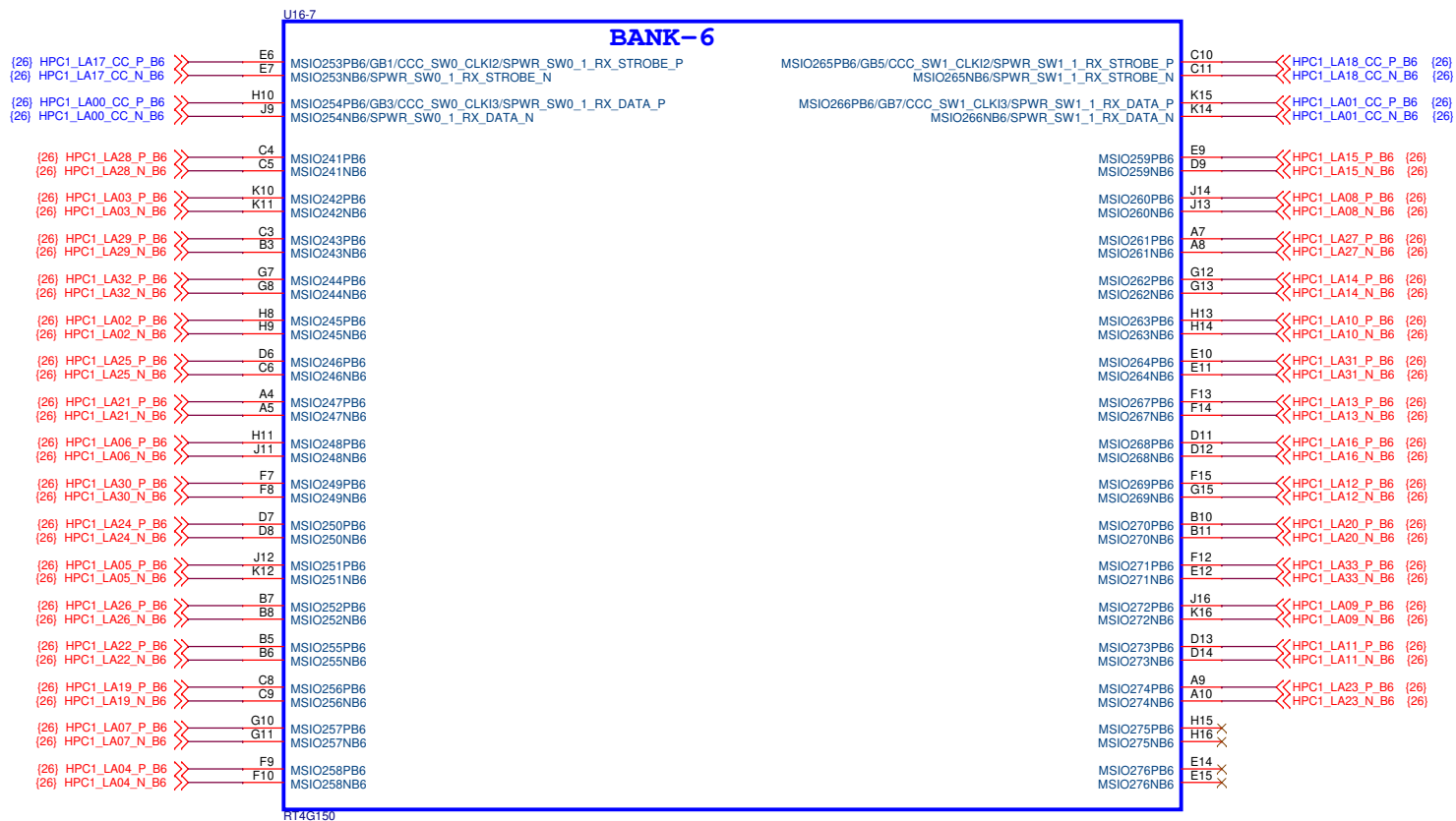
BANK-8



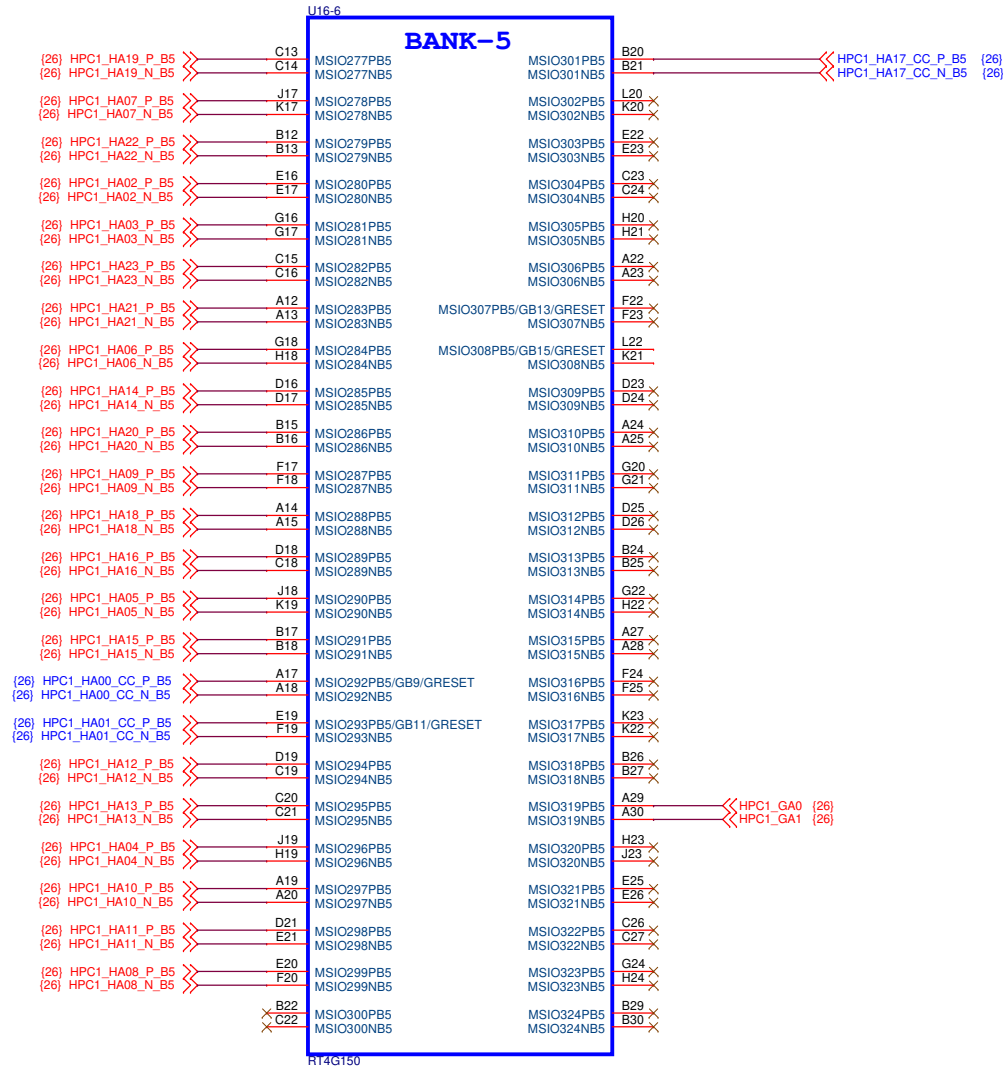
BANK-7



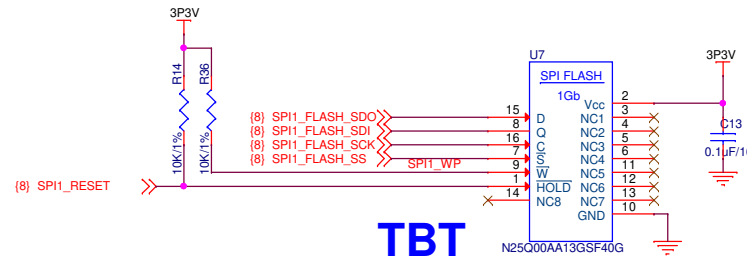
BANK-6



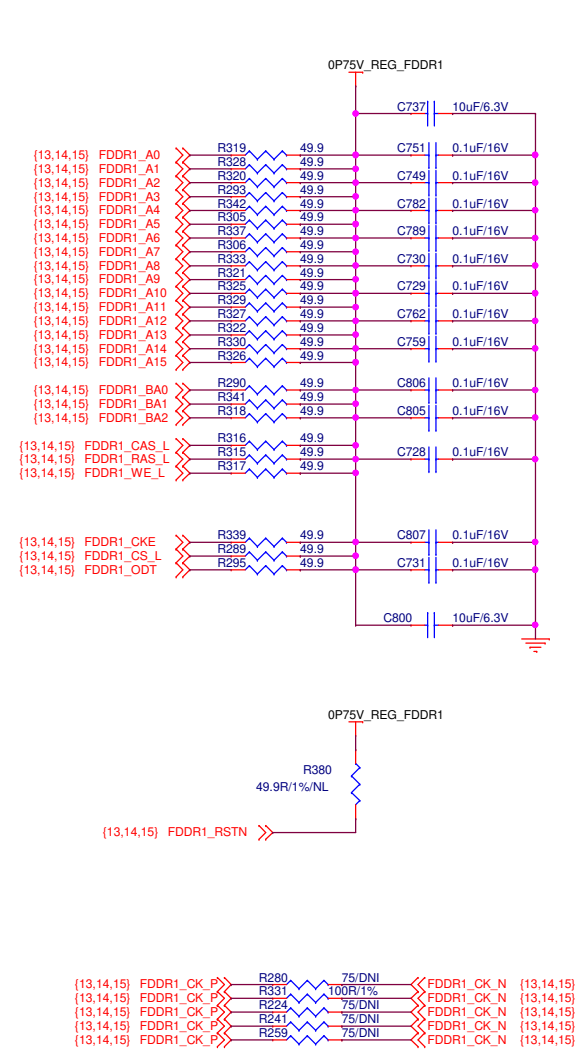
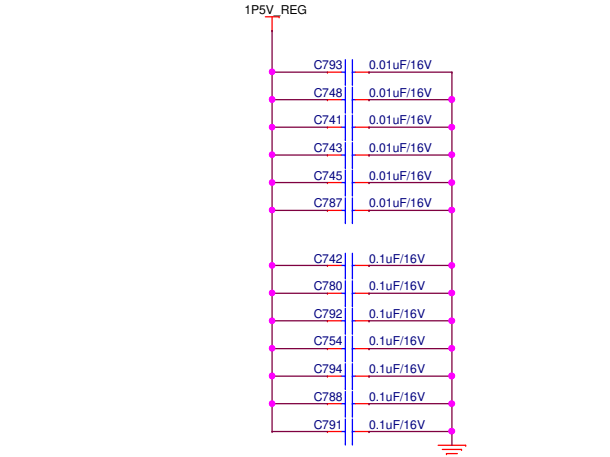
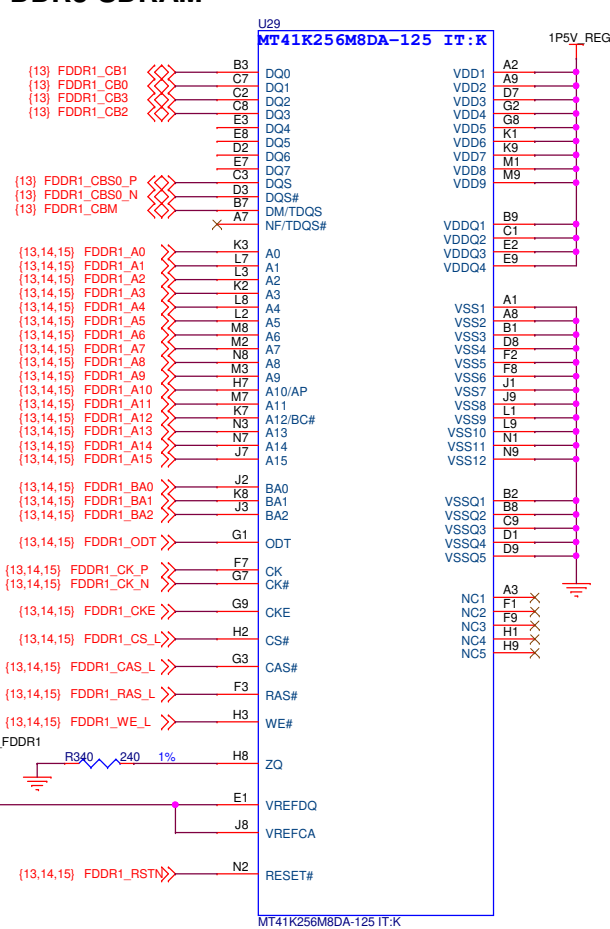
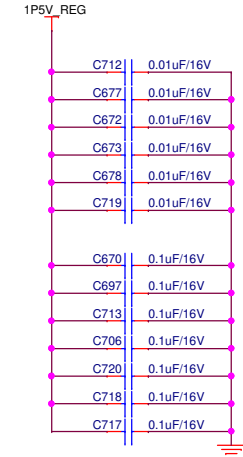
BANK-5



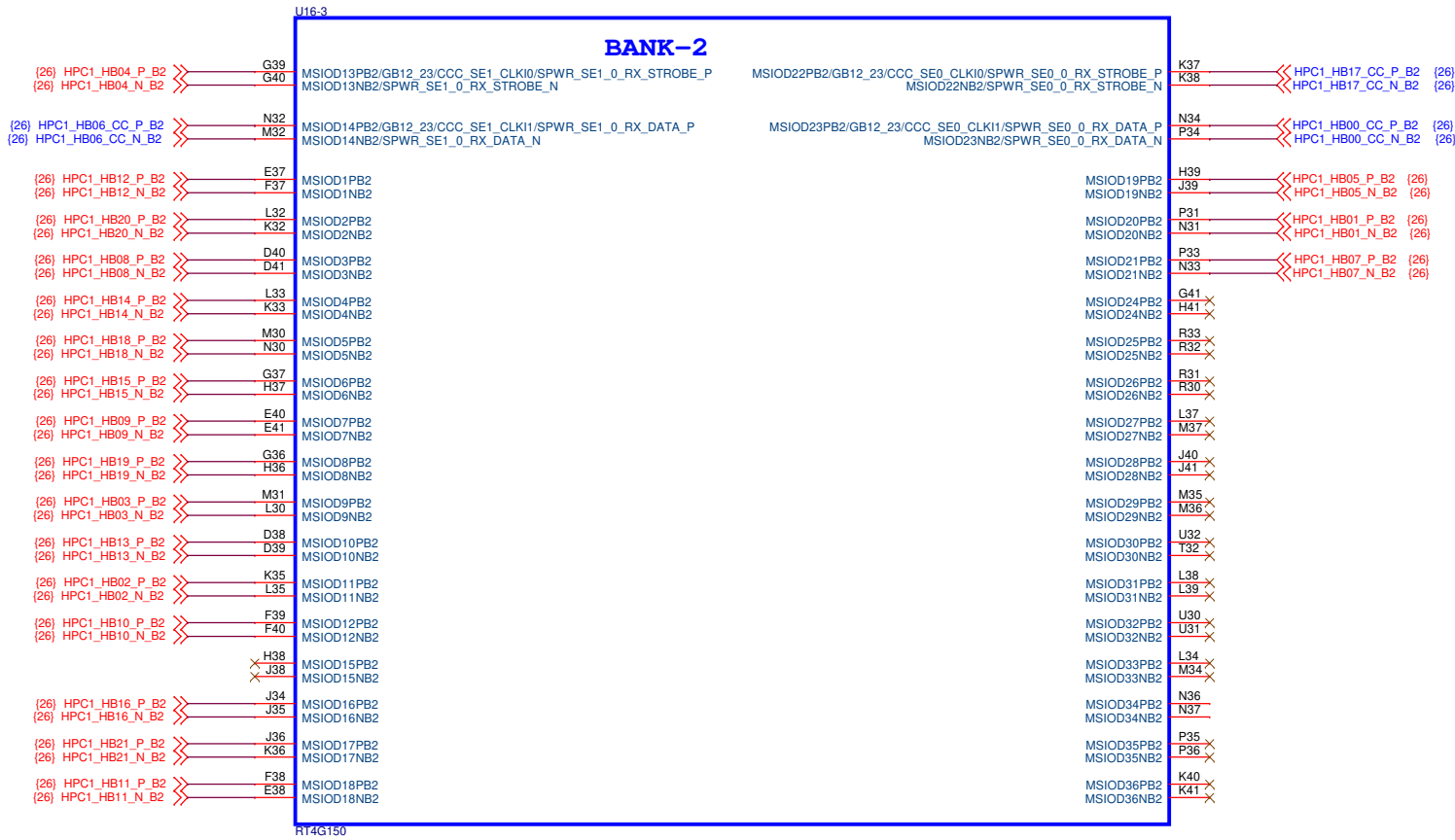
BANK-4



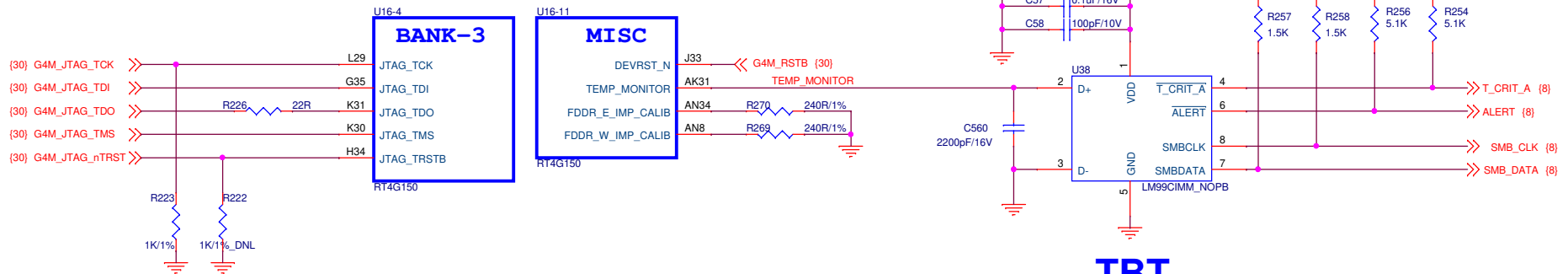
DDR3-SDRAM



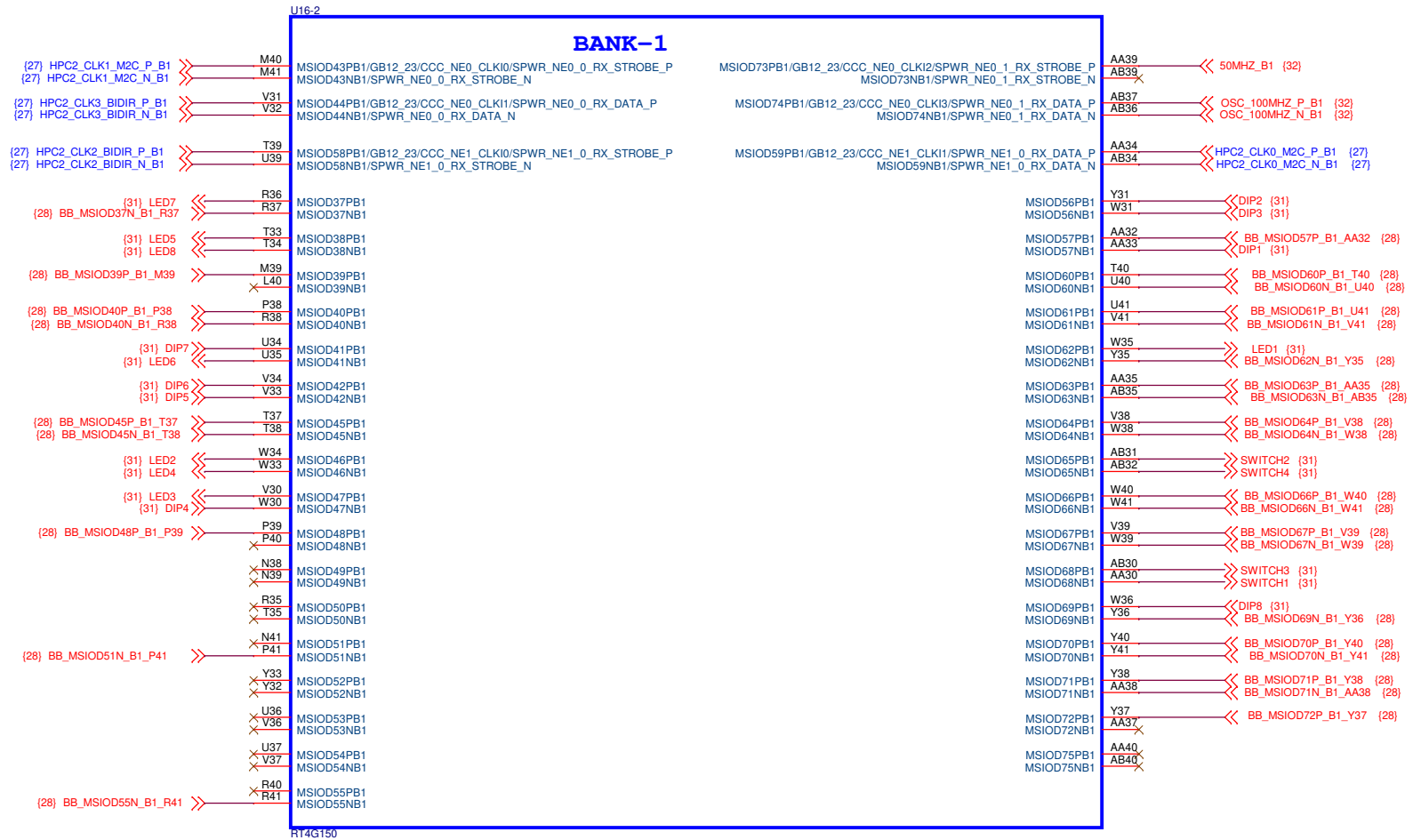
BANK-2



BANK-3 & MISC



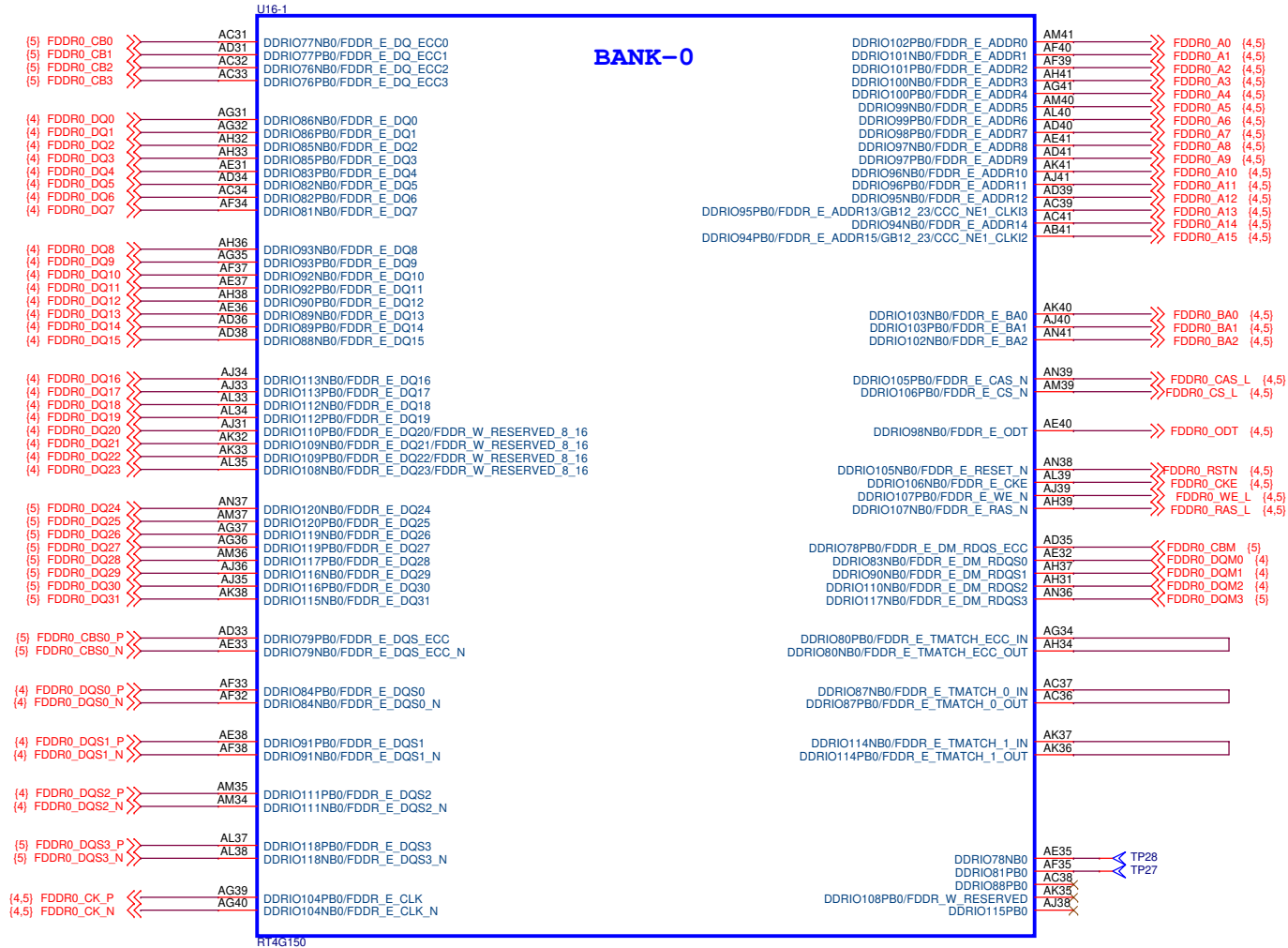
BANK-1



DDR3-SDRAM



MEMORY INTERFACE

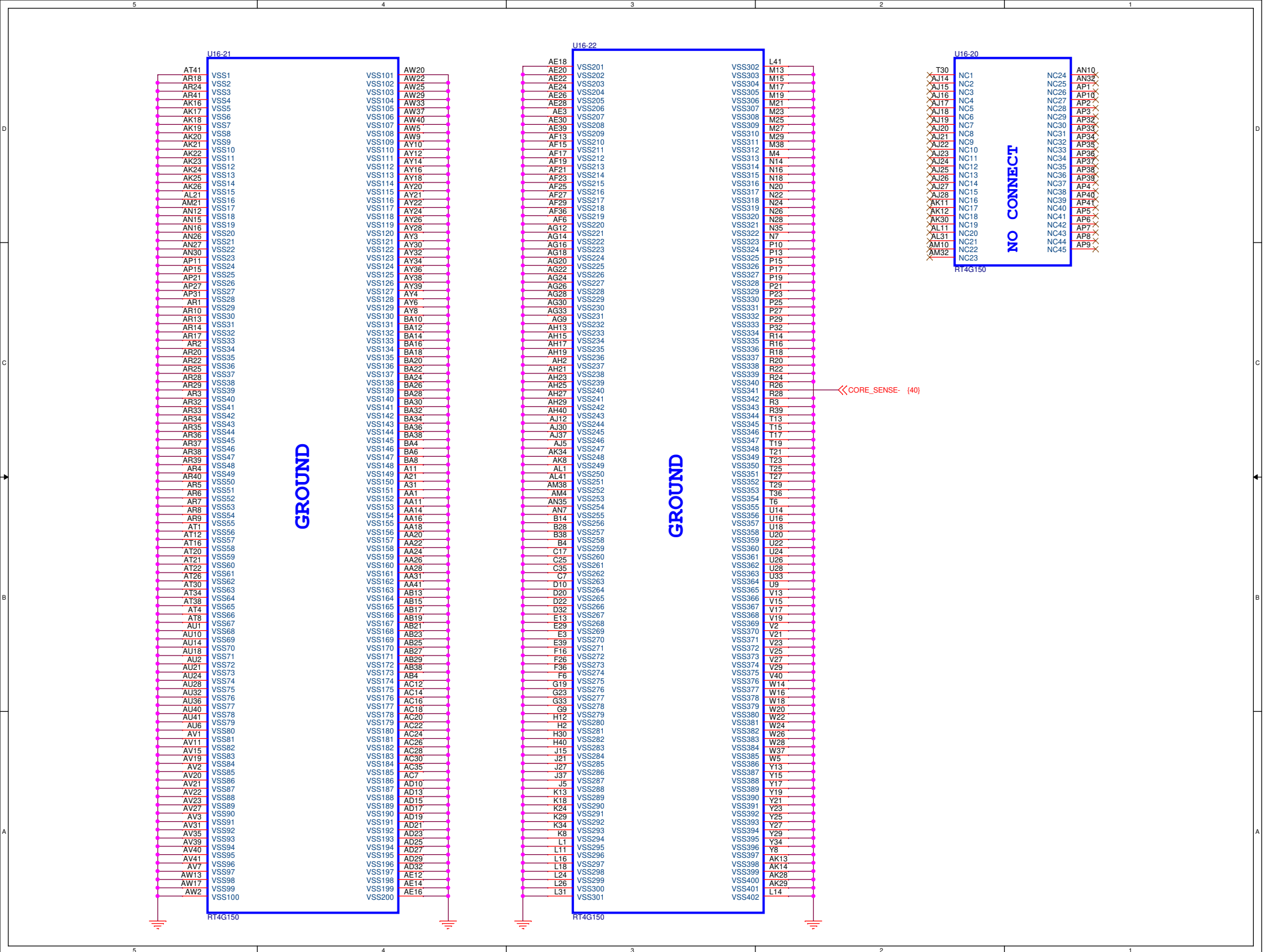


RTG4_DEV_KIT

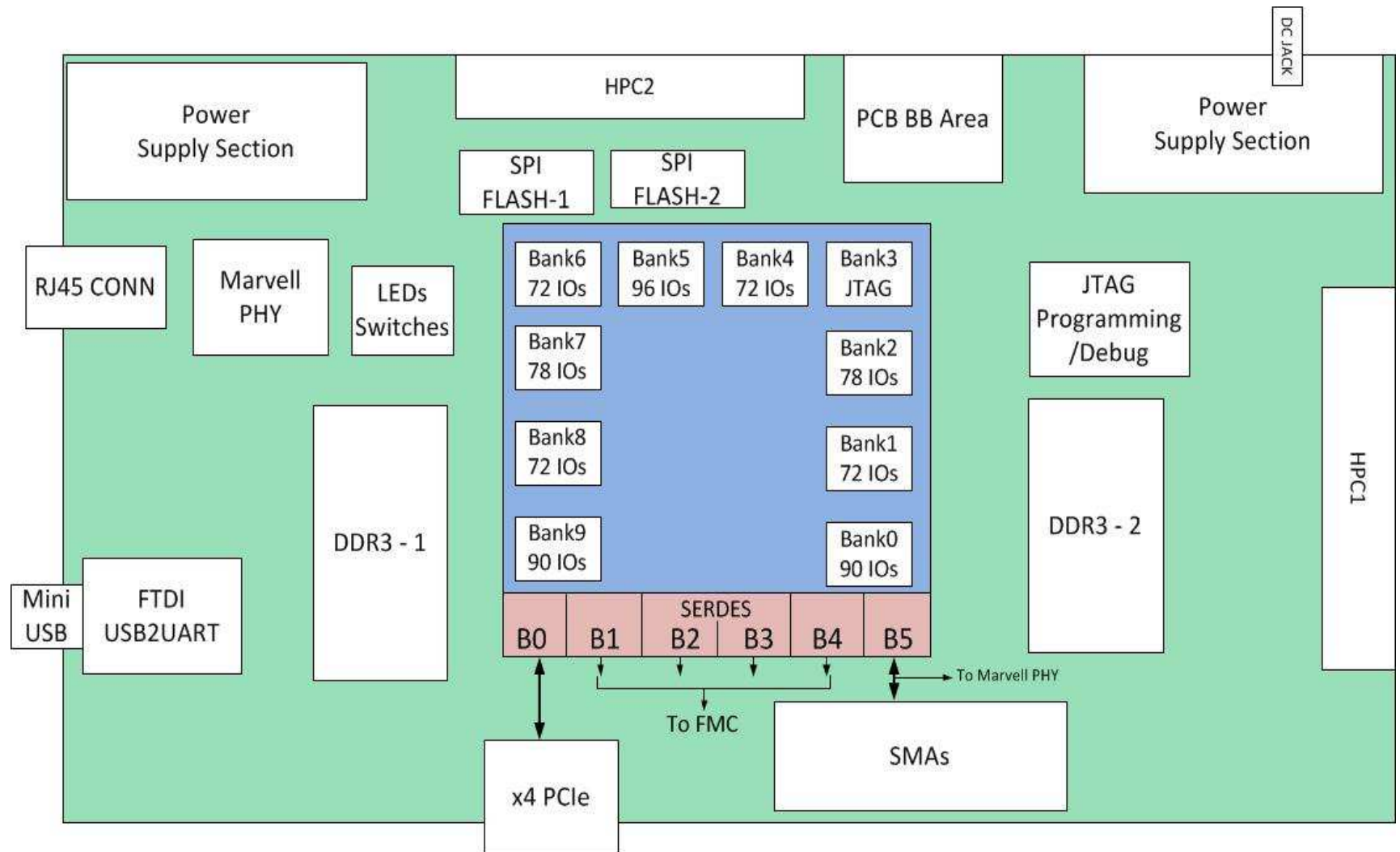
ISLRTG4DEMO1ZB_Rev_B

PAGE NO	TITLE	PAGE NO	TITLE
01	TITLE PAGE	24	SERDES4 CONNECTION
02	BLOCK DIAGRAM	25	SERDES5 CONNECTION
03	BANK0-FDDR0 CONNECTION	26	FMC_CONNECTOR-HPC1
04	DDR3-SDRAM INTERFACE 1-FDDR0	27	FMC_CONNECTOR-HPC2
05	DDR3-SDRAM INTERFACE 2-FDDR0	28	BREAD BOARD CONNECTOR
06	BANK-1 CONNECTION	29	PROGRAMMING BLOCK DIAGRAM
07	BANK-2,3 & MISC CONNECTION	30	PROGRAMMING CIRCUITRY
08	BANK-4 CONNECTION	31	DEBUGGING CIRCUITRY
09	BANK-5 CONNECTION	32	CLOCK CIRCUITRY
10	BANK-6 CONNECTION	33	POWER CONNECTION
11	BANK-7 CONNECTION	34	GROUND & NC CONNECTION
12	BANK-8 CONNECTION	35	DECOUPLING CAPACITOR CONNECTION
13	BANK9-FDDR1 CONNECTION	36	POWER SCHEME
14	DDR3-SDRAM INTERFACE 1-FDDR1	37	12V POWER SUPPLY CONNECTION
15	DDR3-SDRAM INTERFACE 2-FDDR1	38	POWER HEADER CONNECTION
16	MARVELL PHY-88E1340S	39	POWER SUPPLIES-1
17	MARVELL PHY - RJ45 INTERFACE	40	POWER SUPPLIES-2
18	FT4232H CIRCUITRY	41	POWER SUPPLIES-3
19	SERDES BLOCK DIAGRAM	42	POWER SUPPLIES-4
20	SERDES0 CONNECTION	43	POWER SUPPLIES-5
21	SERDES1 CONNECTION	44	POWER SUPPLIES-6
22	SERDES2 CONNECTION	45	POWER LEDs
23	SERDES3 CONNECTION		

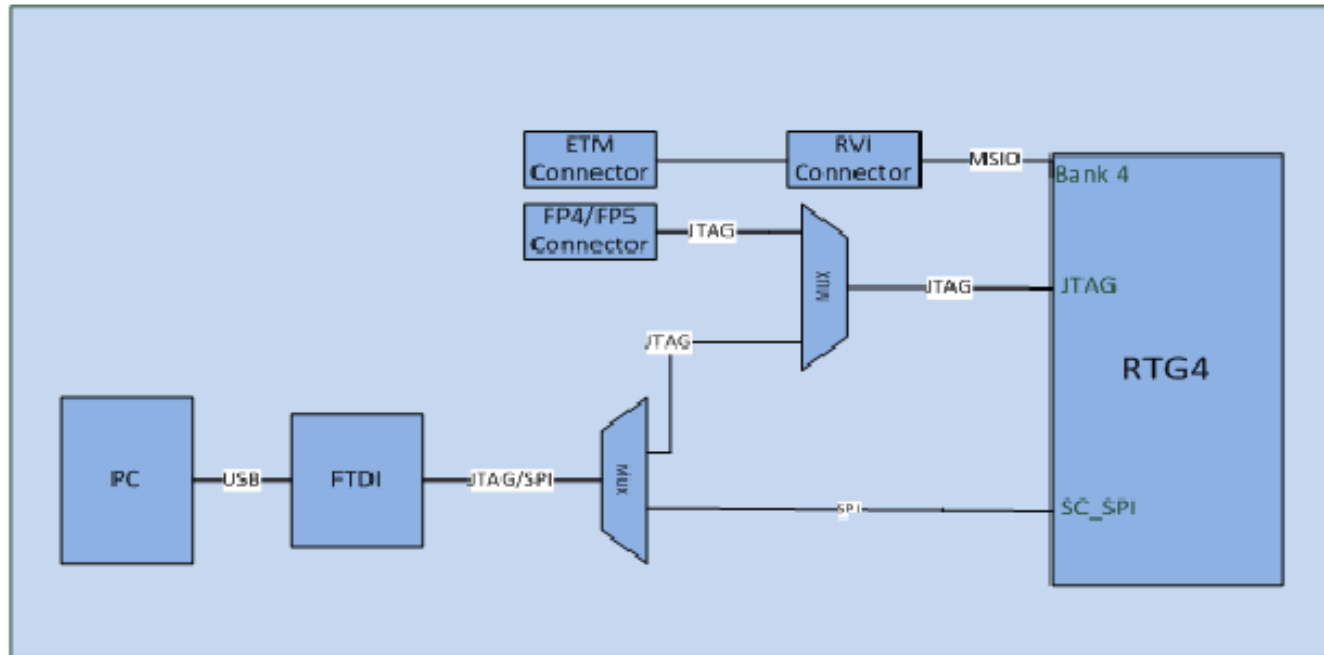




BLOCK DIAGRAM

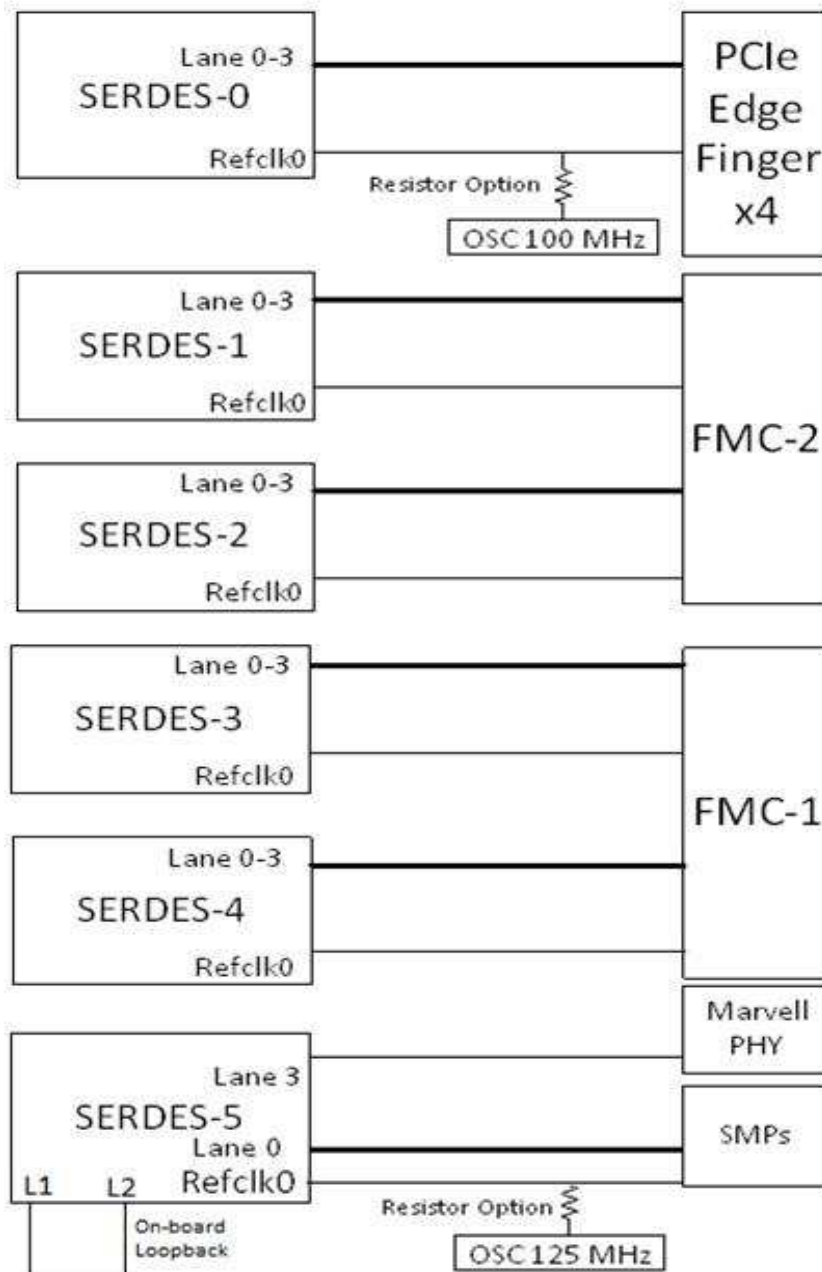


PROGRAMING SCHEME

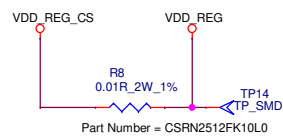
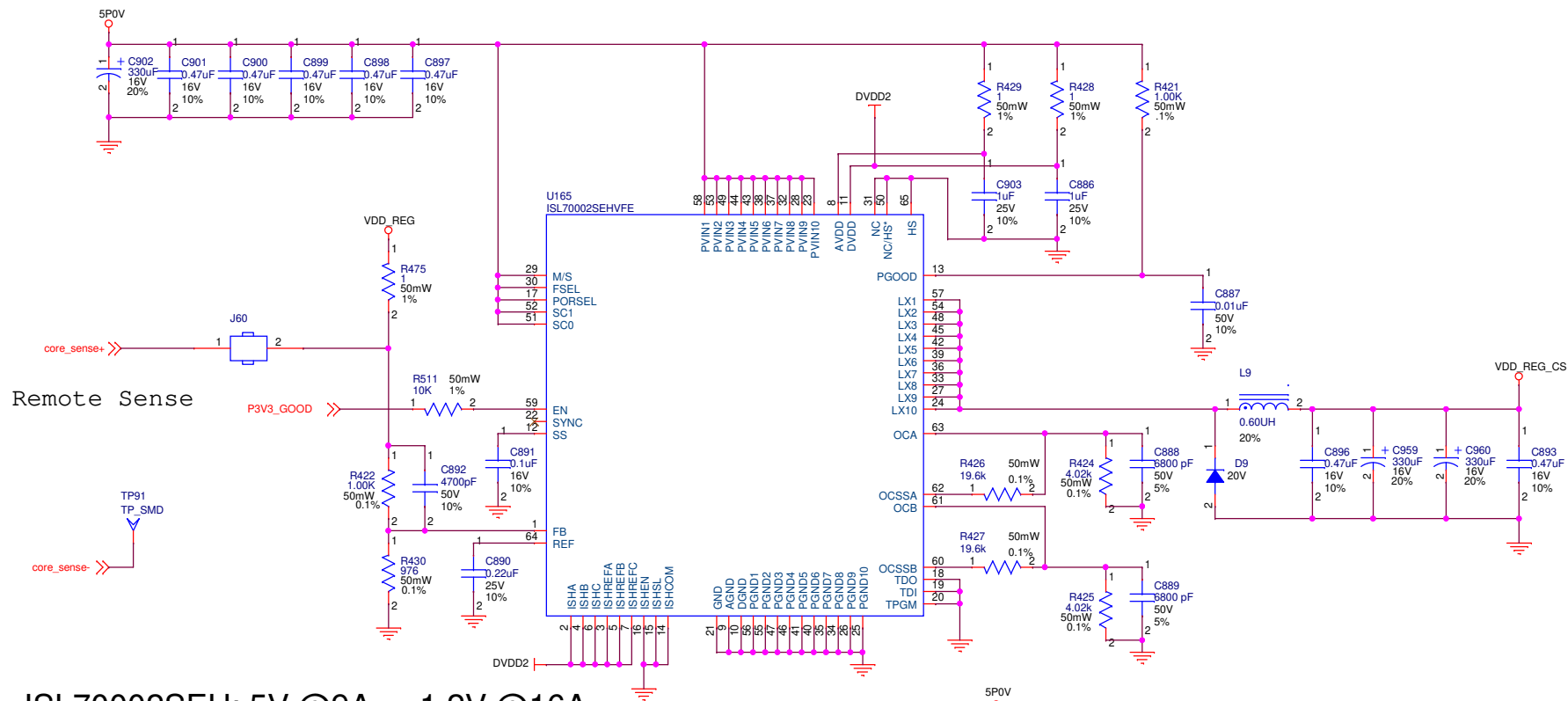


SERDES BLOCK DIAGRAM

SERDES Block allocation for RTG4 DEV KIT



POWER SUPPLIES - 2

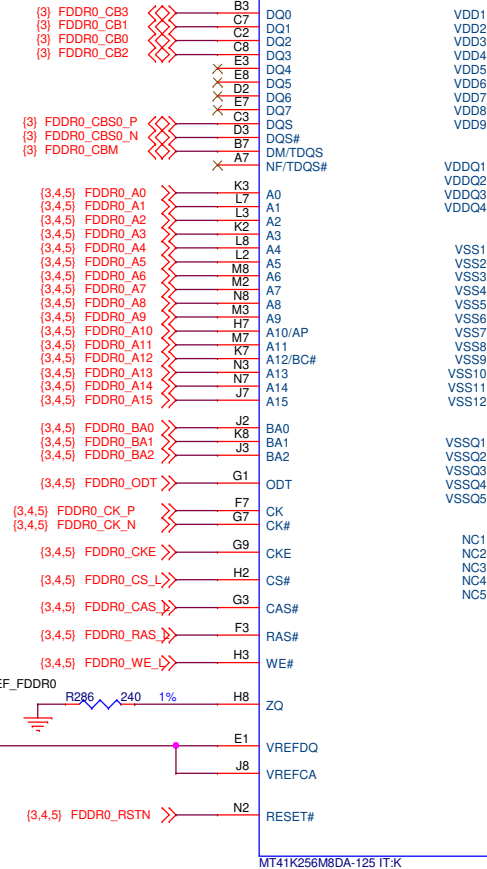


CORE CURRENT SENSING CIRCUIT

DDR3-SDRAM

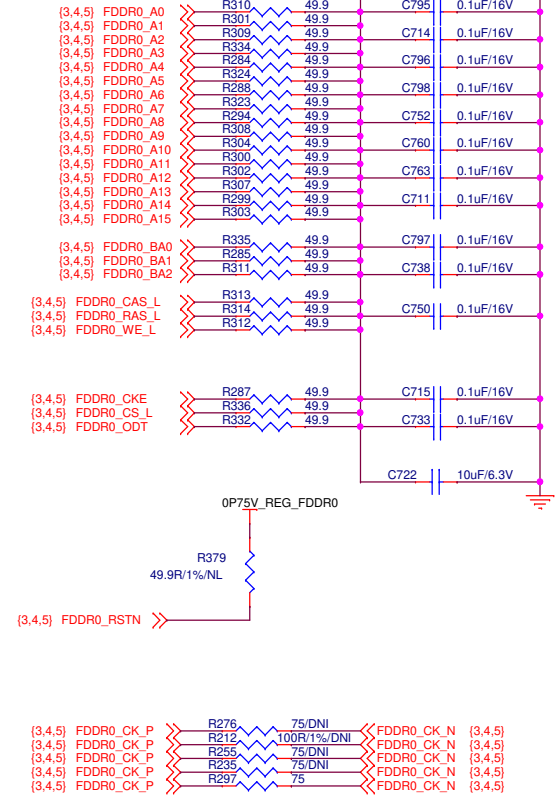


1P5V_REG

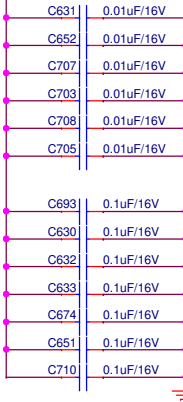


1P5V_REG

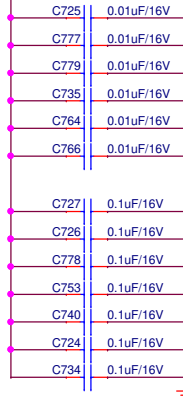
0P75V_REG_FDDR0



1P5V_REG

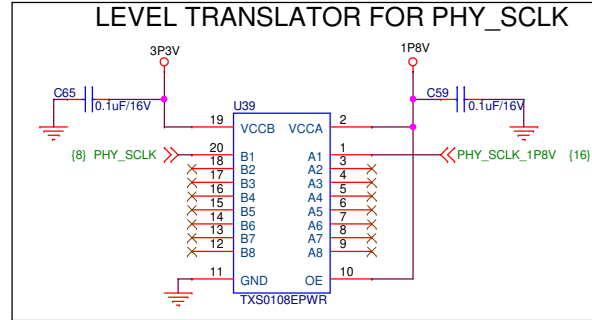
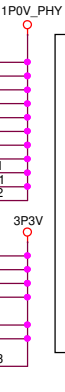
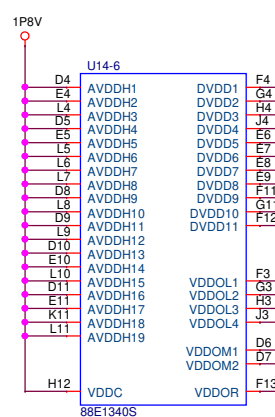
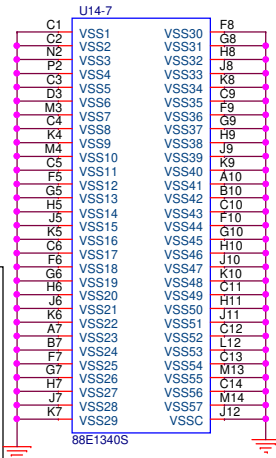
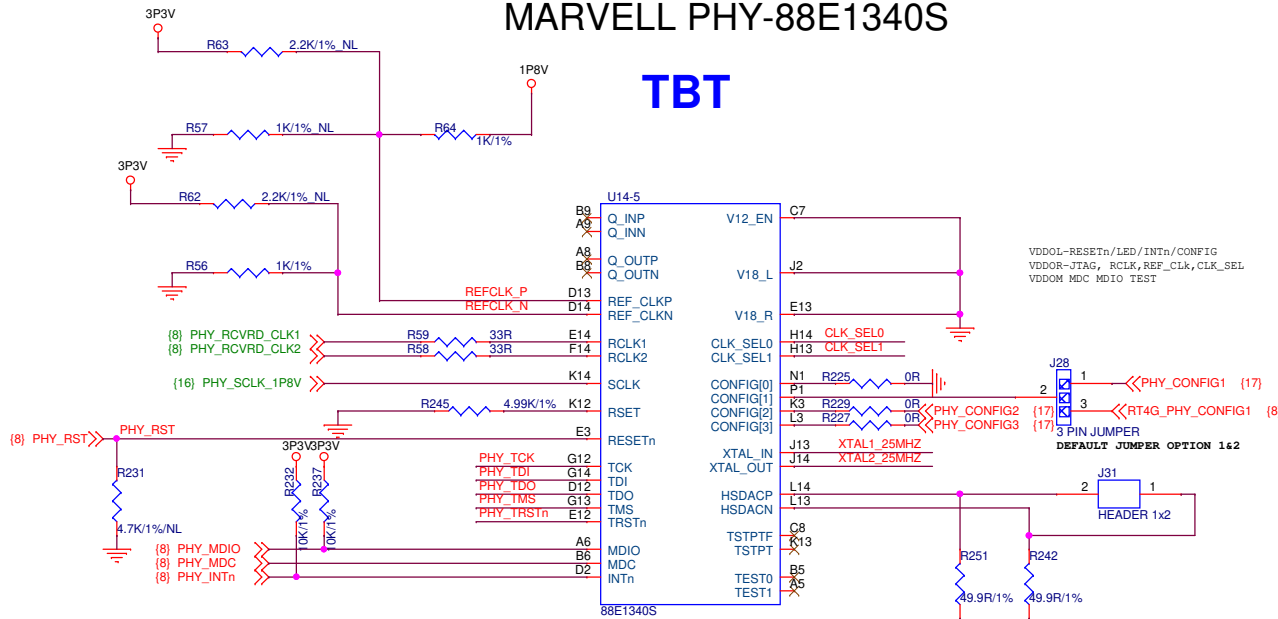
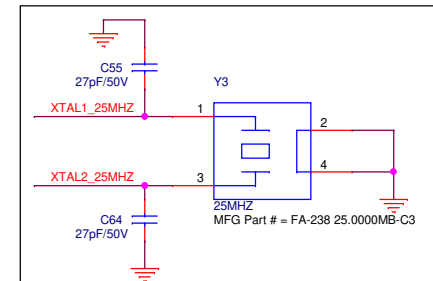
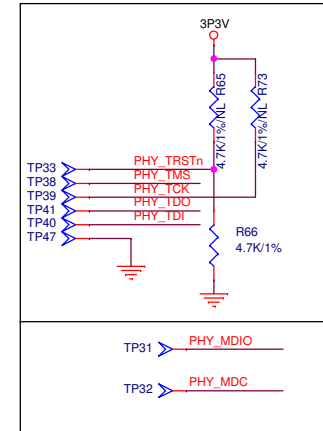
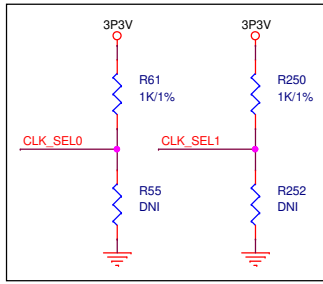


1P5V_REG

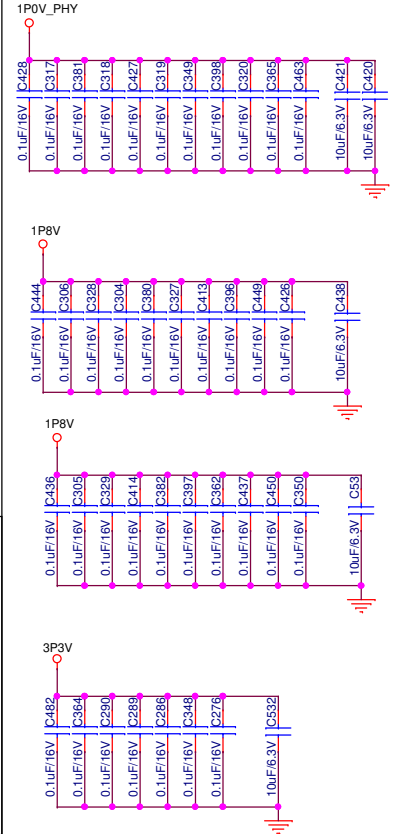


MARVELL PHY-88E1340S

TBT

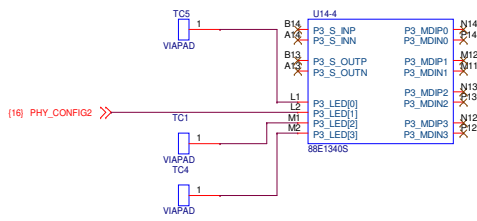
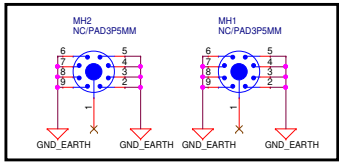
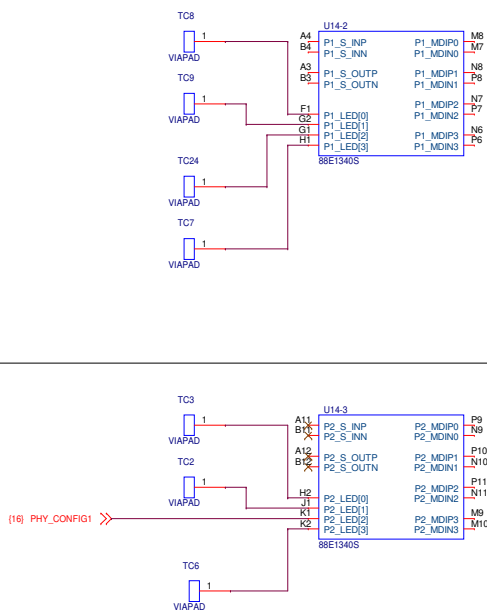
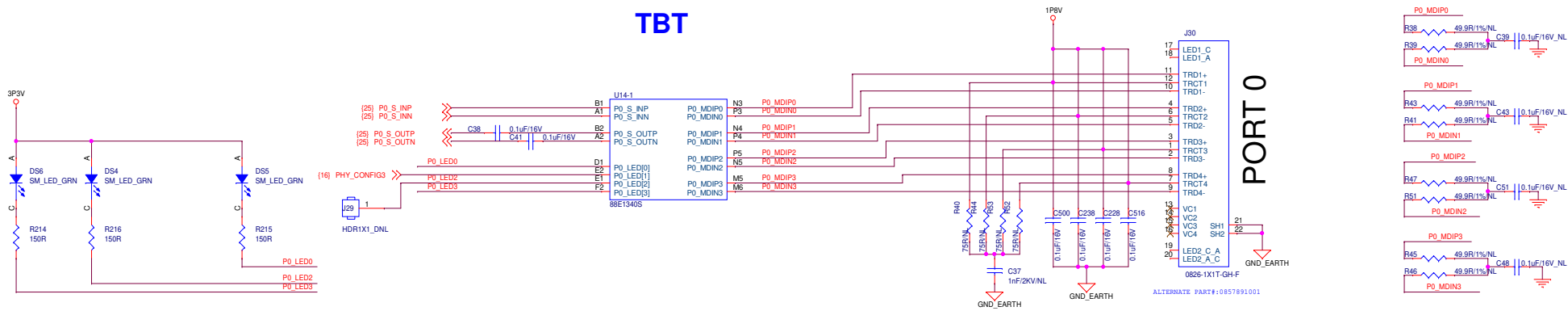


DECOUPLING CAPACITORS



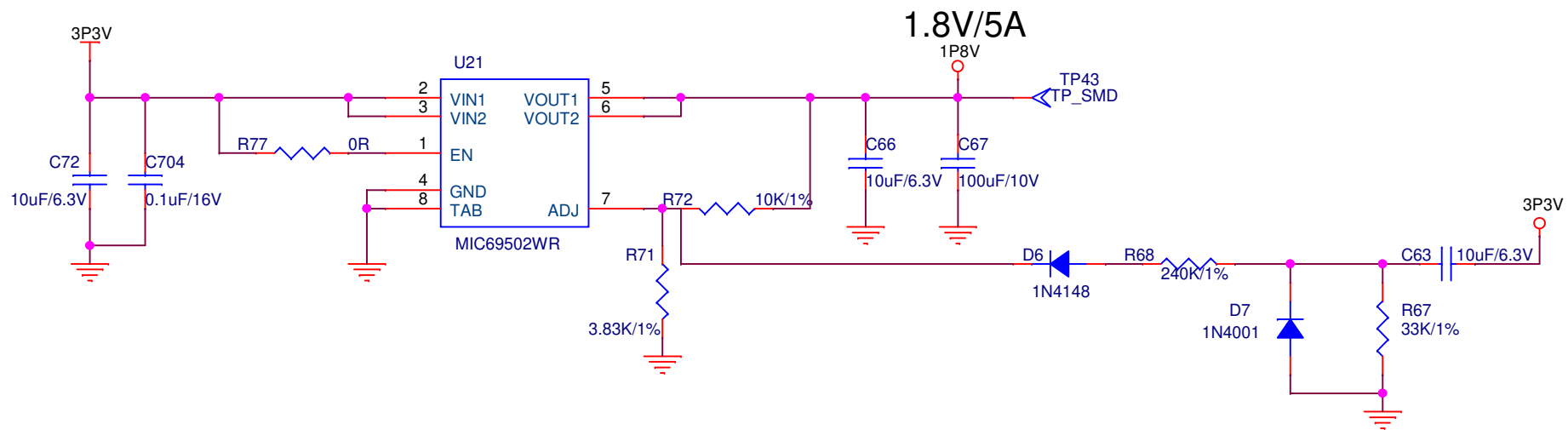
MARVELL PHY - RJ45 INTERFACE

TBT

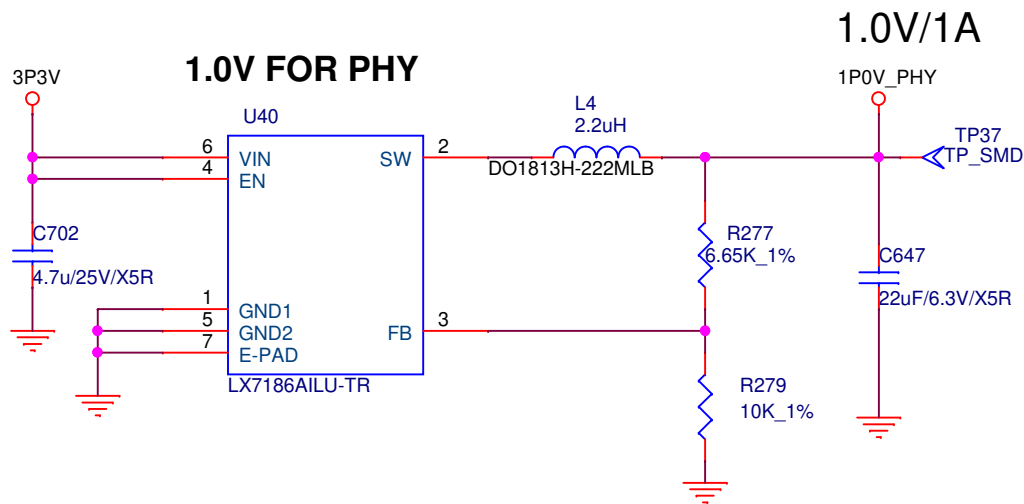


POWER SUPPLIES - 5

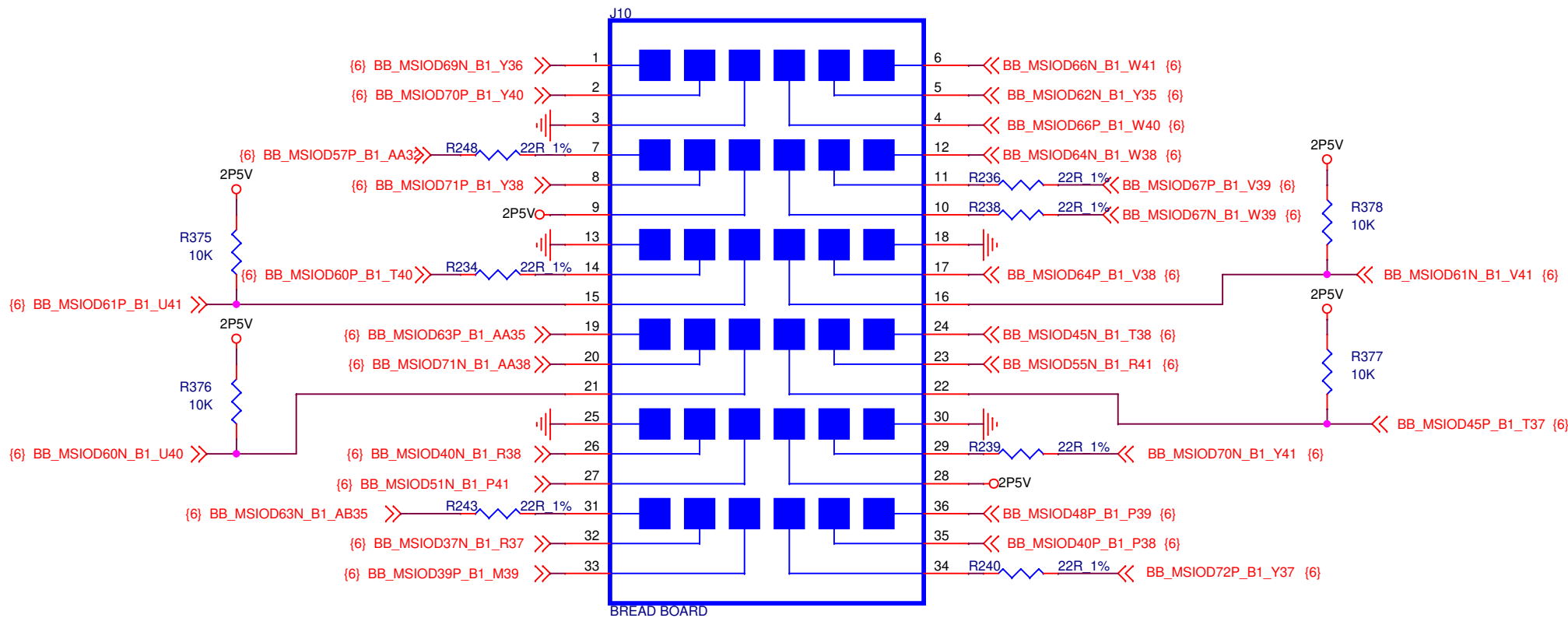
REGULATOR 9: 1.8V/5A FOR 88E1340 ANALOG CORE/USB

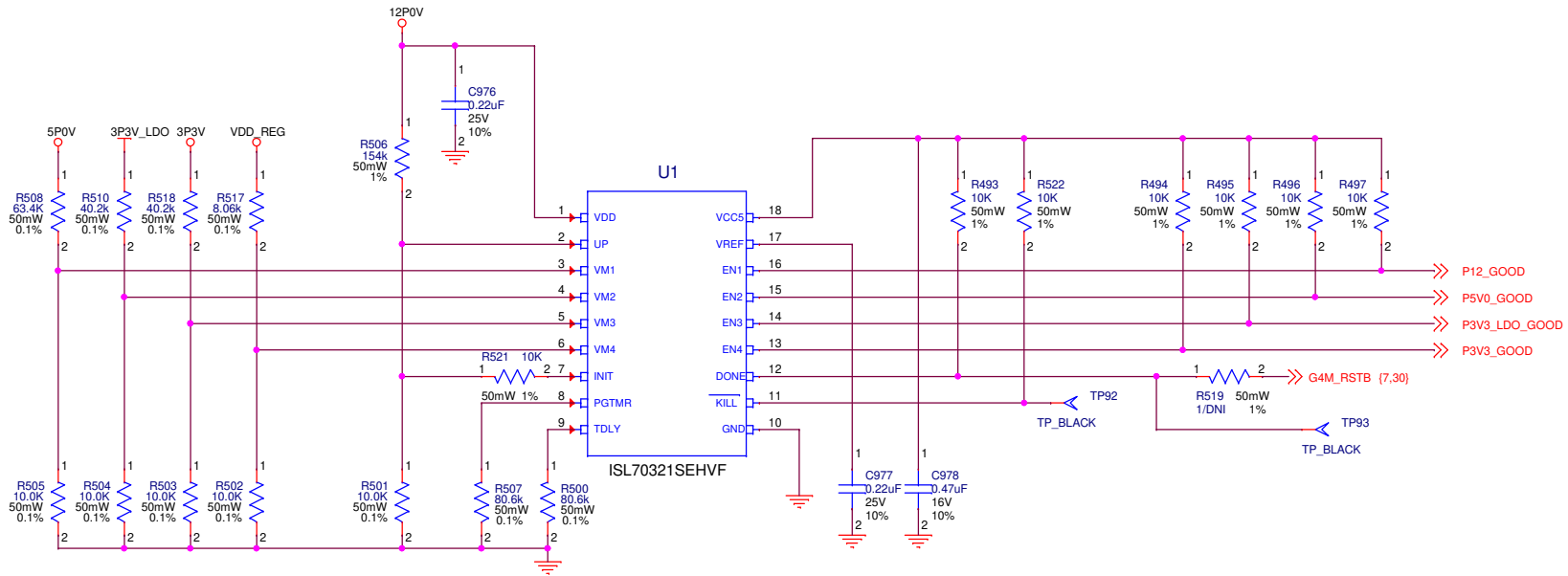
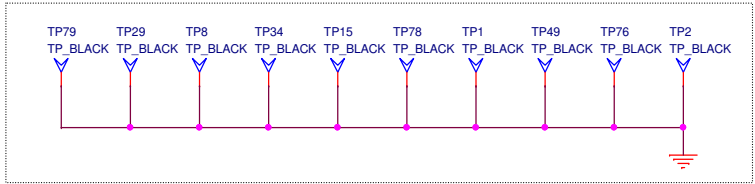
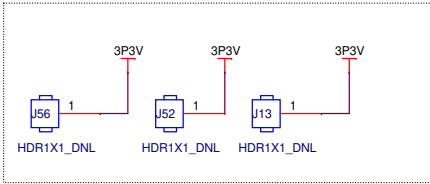
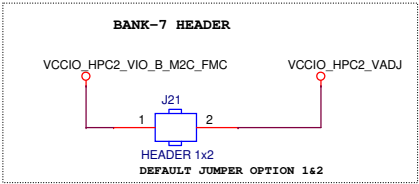
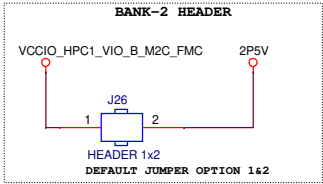


REGULATOR 10: 1V/1A_FOR PHY 88E1340



BREAD BOARD CONNECTOR





Sequencer

