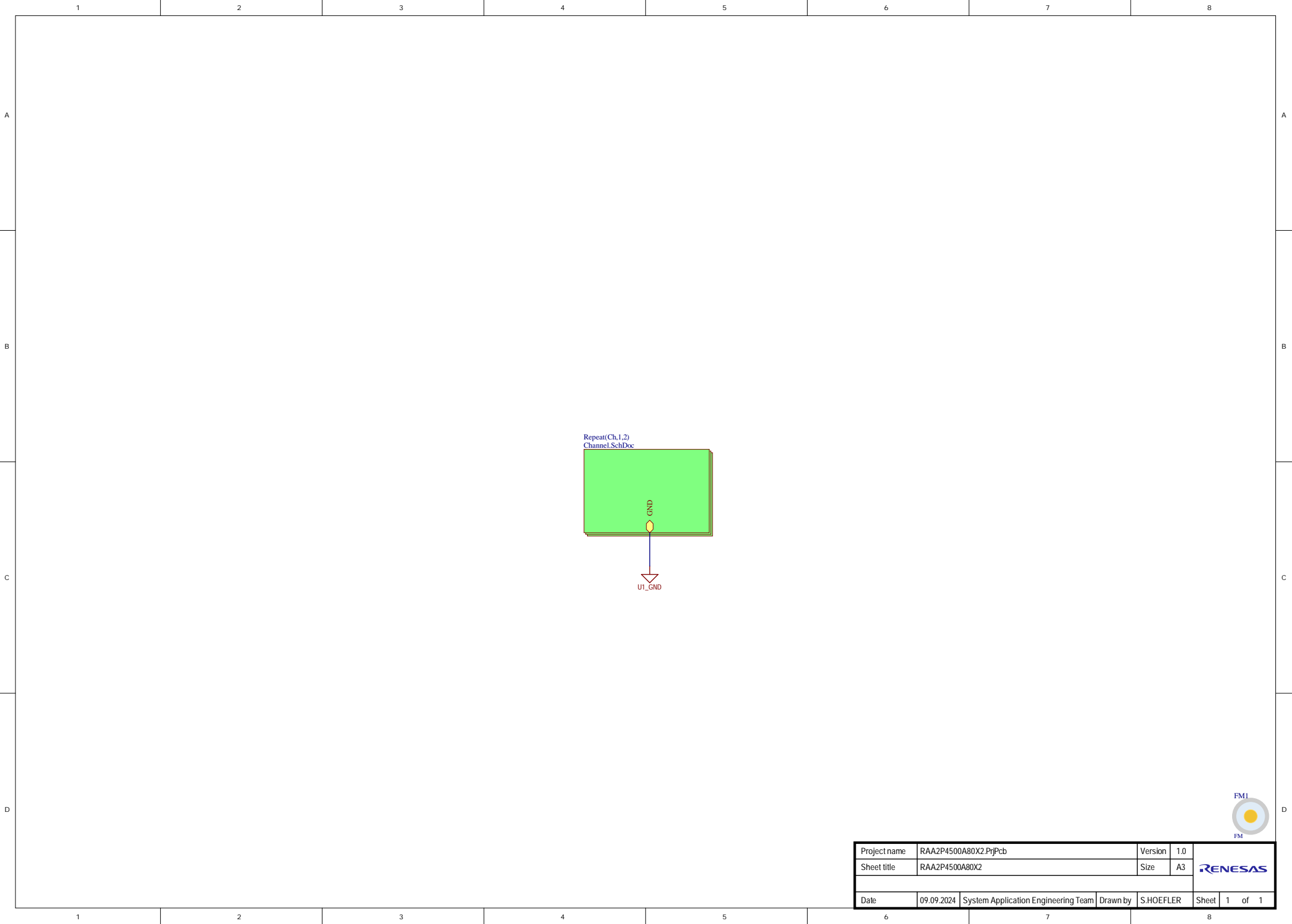



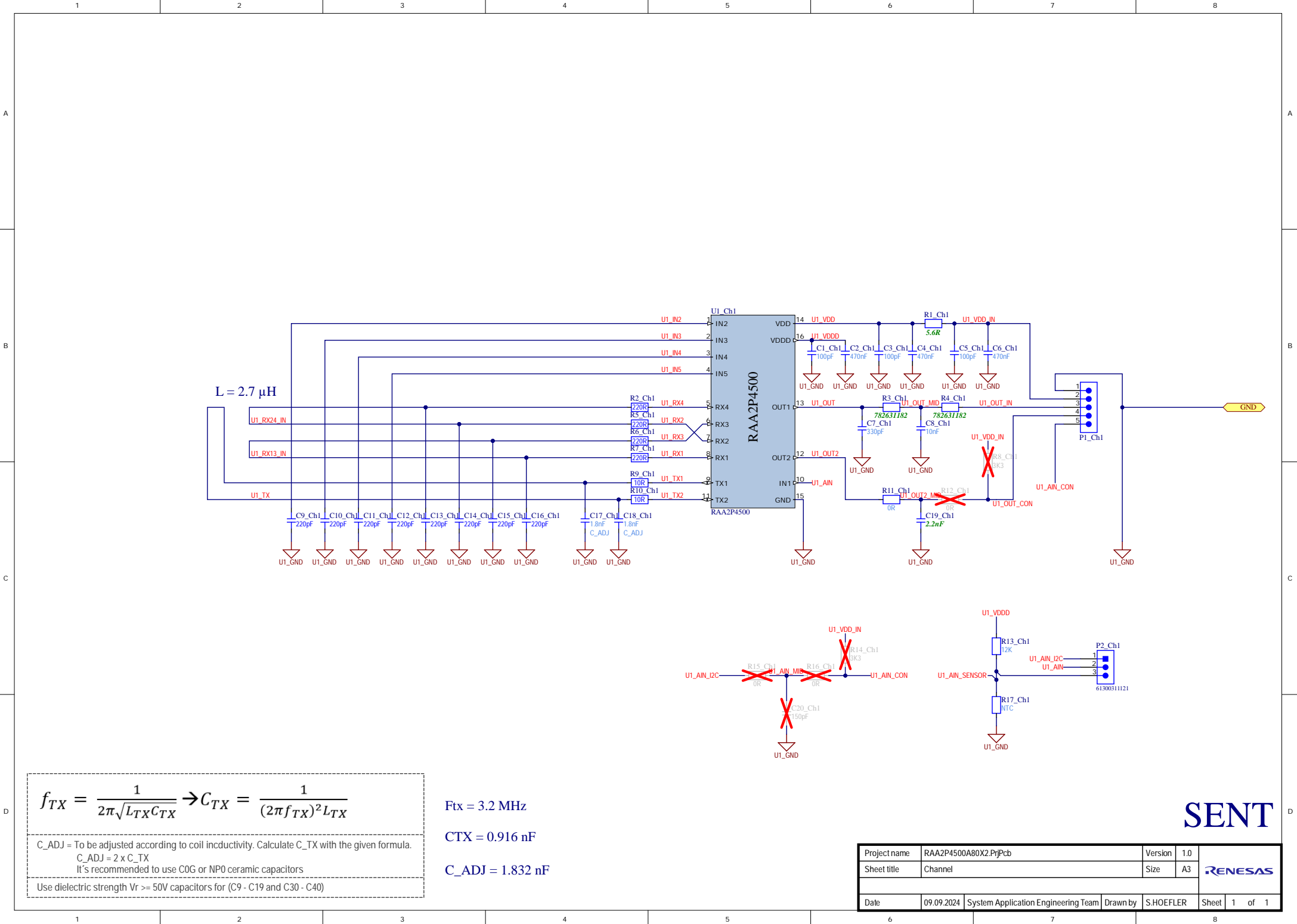


RAA2P4500A80X2

Date:	13.11.2024
Project:	RAA2P4500A80X2.PrjPcb
Version	1.0
Content:	Schematic Sensor PCB Layout Sensor PCB Placement Sensor PCB 3D Model PCB Manufacturing Requirements Sensor PCB Layer View Sensor PCB Layer Stack Bill Of Materials Target PCB Layout Target PCB 3D Model



Project name	RAA2P4500A80X2.PrjPcb			Version	1.0		
Sheet title	RAA2P4500A80X2			Size	A3		
Date	09.09.2024	System Application Engineering Team		Drawn by	S.HOEFLER	Sheet	1 of 1



$$f_{TX} = \frac{1}{2\pi\sqrt{L_{TX}C_{TX}}} \rightarrow C_{TX} = \frac{1}{(2\pi f_{TX})^2 L_{TX}}$$

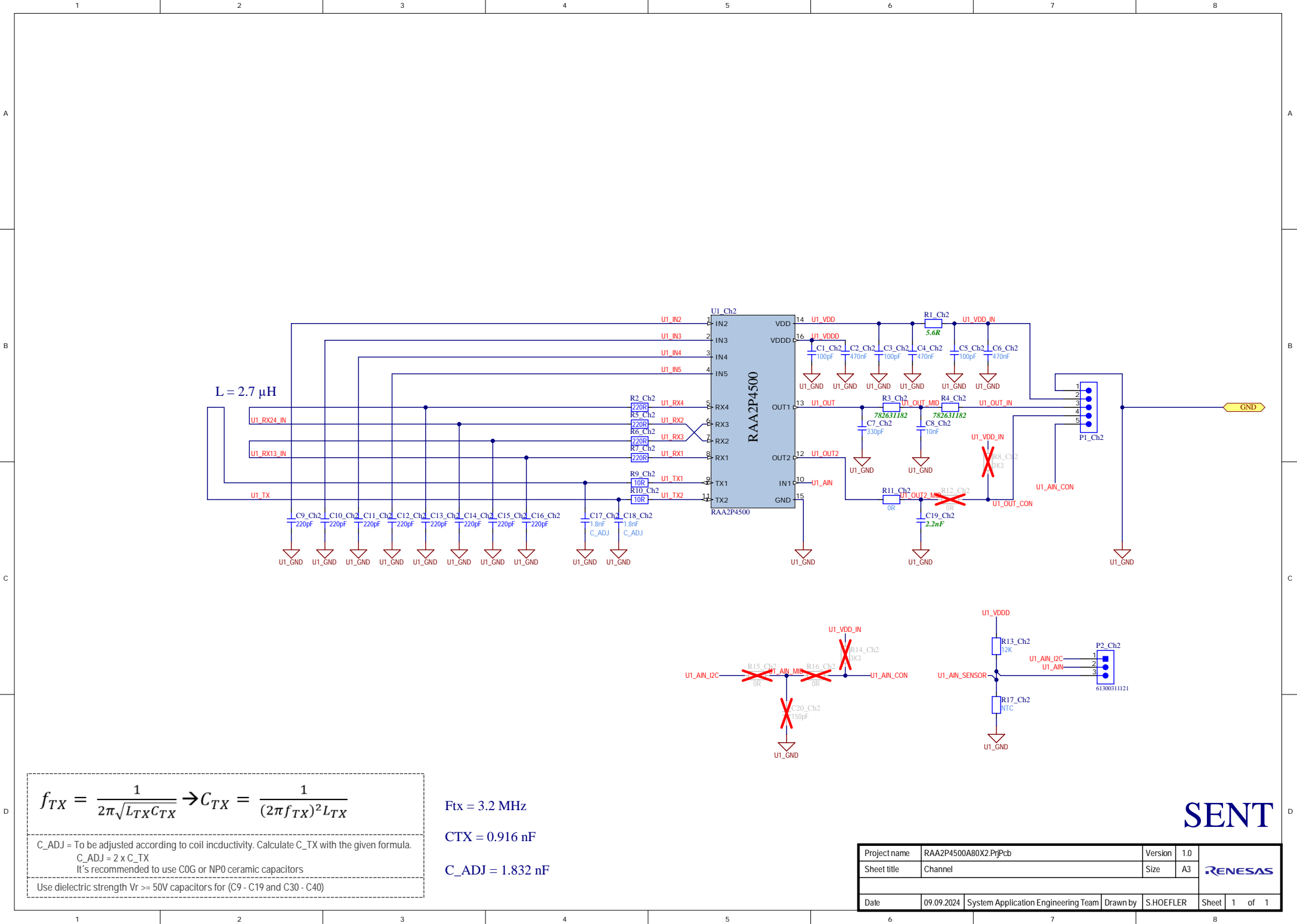
C_ADJ = To be adjusted according to coil inductivity. Calculate C_TX with the given formula.
C_ADJ = 2 x C_TX
It's recommended to use C0G or NP0 ceramic capacitors
Use dielectric strength Vr >= 50V capacitors for (C9 - C19 and C30 - C40)

Ftx = 3.2 MHz

CTX = 0.916 nF

C_ADJ = 1.832 nF

Project name	RAA2P4500A80X2.PrjPcb	Version	1.0	RENEASAS
Sheet title	Channel	Size	A3	
Date	09.09.2024	System Application Engineering Team	Drawn by	S.HOEFLER
Sheet	1	of	1	



$$f_{TX} = \frac{1}{2\pi\sqrt{L_{TX}C_{TX}}} \rightarrow C_{TX} = \frac{1}{(2\pi f_{TX})^2 L_{TX}}$$

C_ADJ = To be adjusted according to coil inductivity. Calculate C_TX with the given formula.
C_ADJ = 2 x C_TX
It's recommended to use COG or NP0 ceramic capacitors
Use dielectric strength V_r >= 50V capacitors for (C9 - C19 and C30 - C40)

f_{TX} = 3.2 MHz

C_{TX} = 0.916 nF

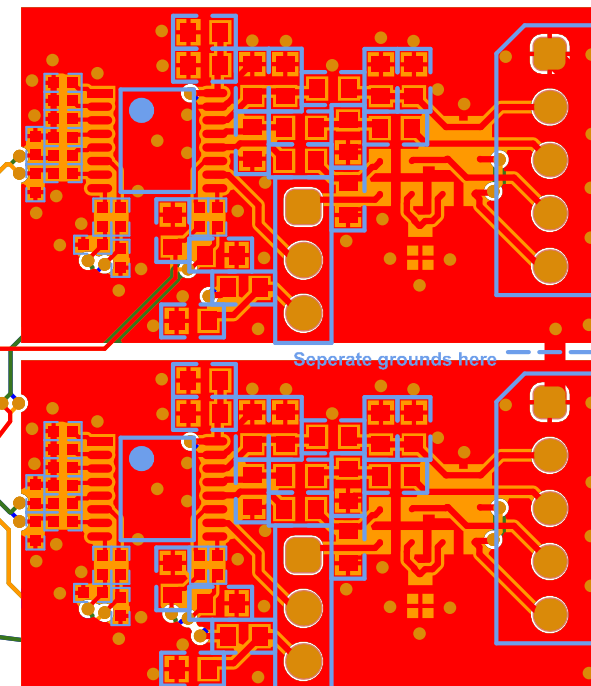
C_{ADJ} = 1.832 nF

SENT

RENEASAS

Project name	RAA2P4500A80X2.PrjPcb	Version	1.0	Sheet 1 of 1
Sheet title	Channel	Size	A3	
Date	09.09.2024	System Application Engineering Team	Drawn by S.HOEFLER	

RAA2P4500A80X2
13NOV2024



RENESAS

PCB ML4 1.6mm

AG 1.5mm

39.00

55.00

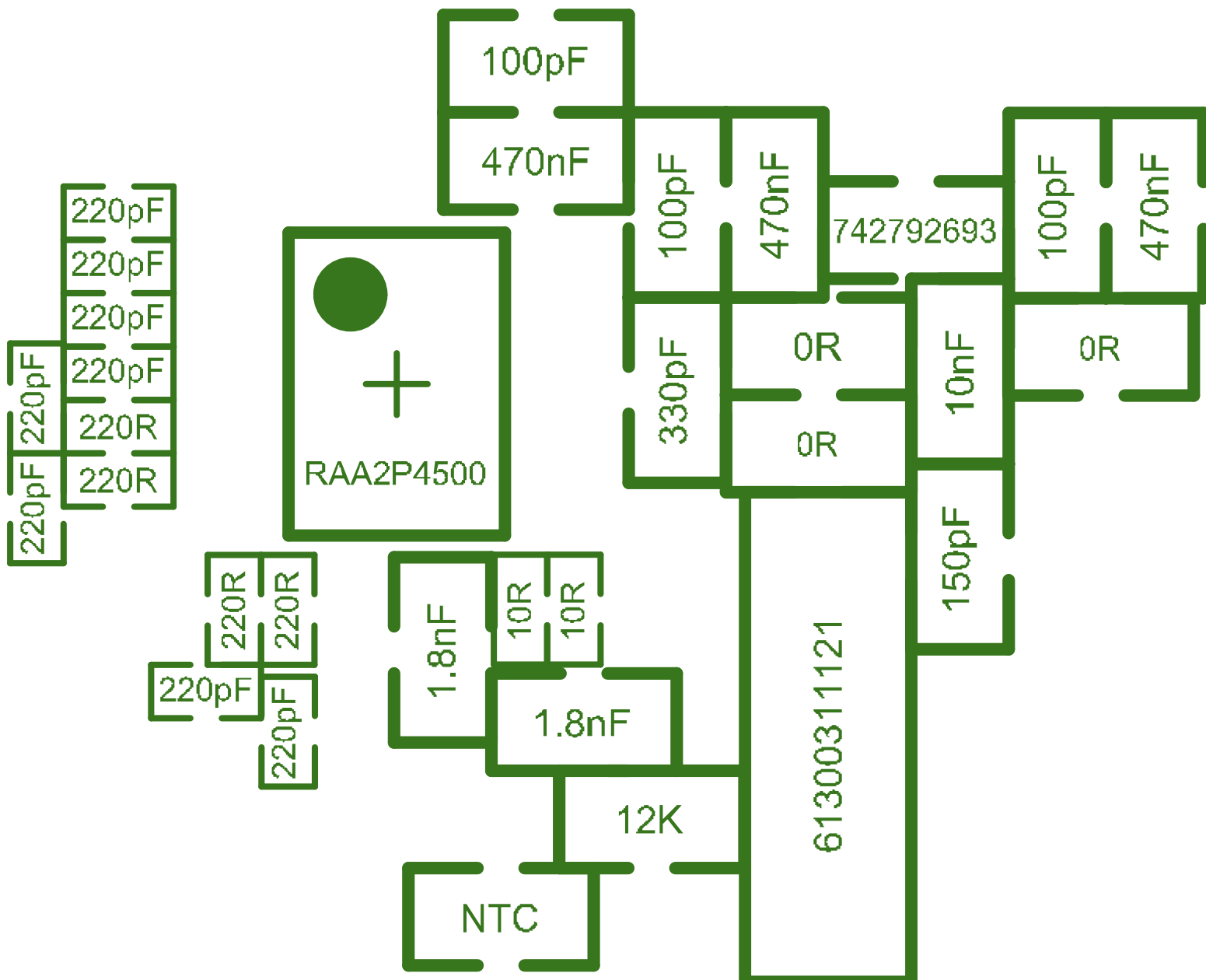
97.50

d2.5mm

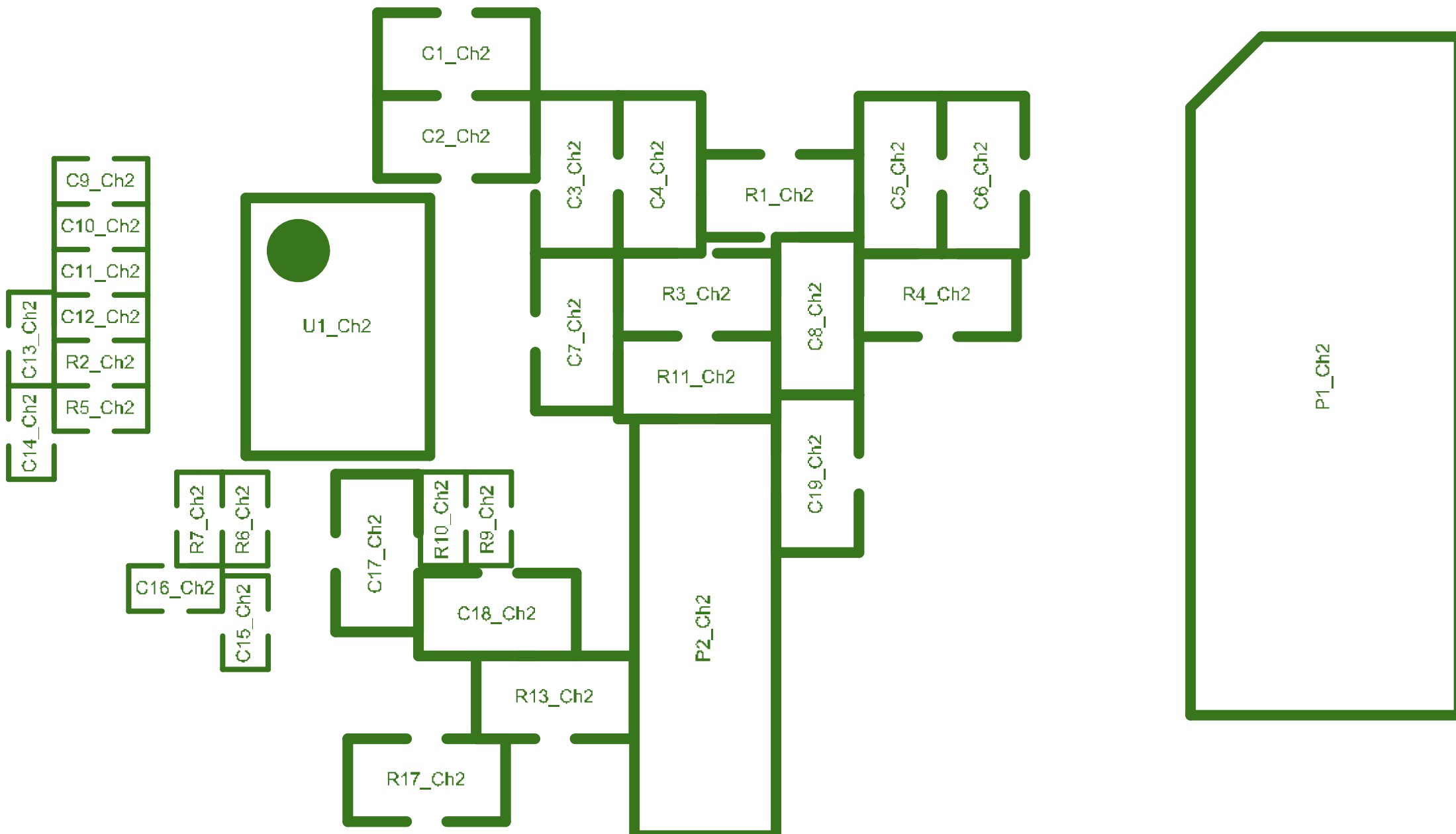
d5.5mm

62.50

55.00

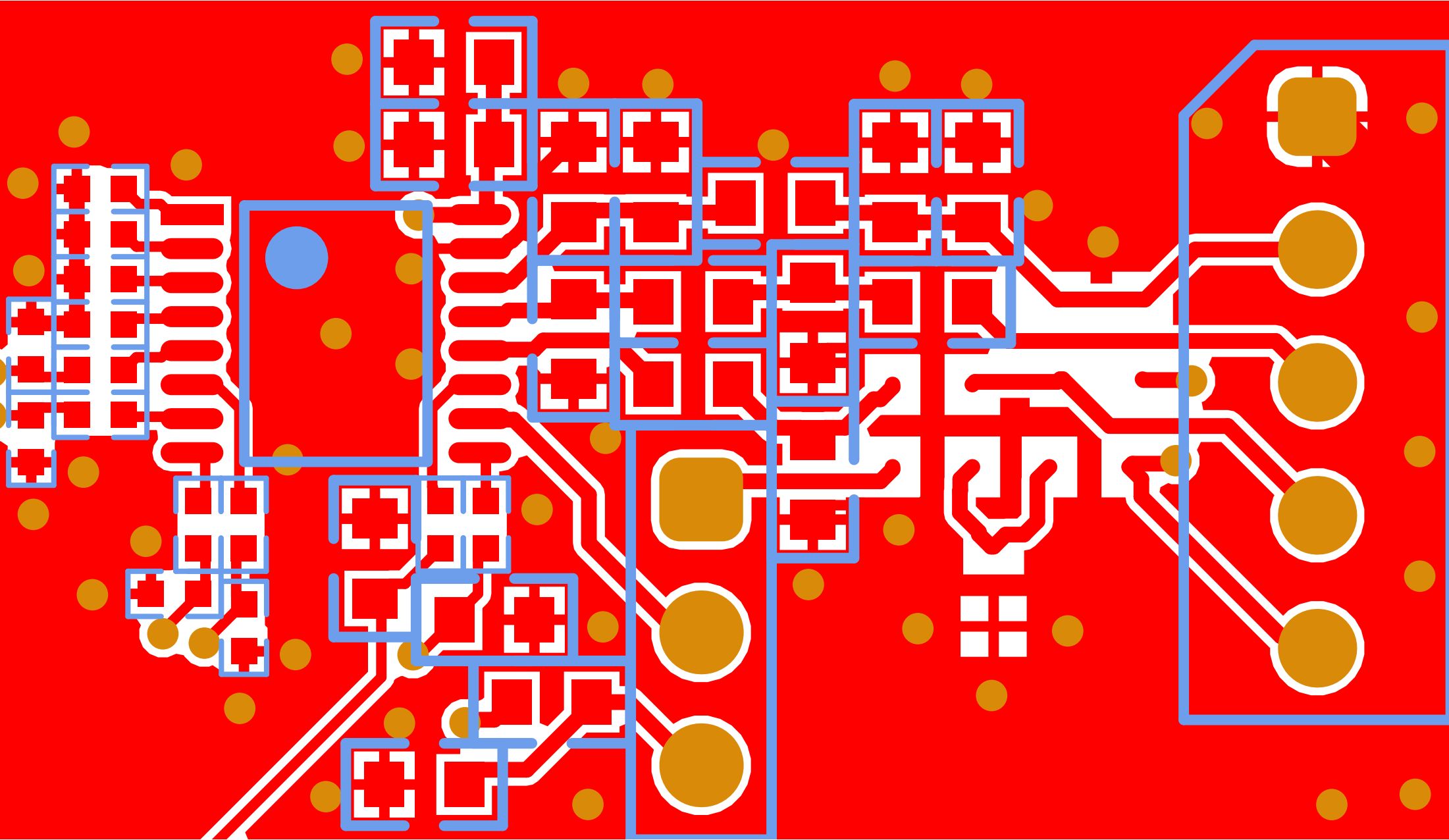


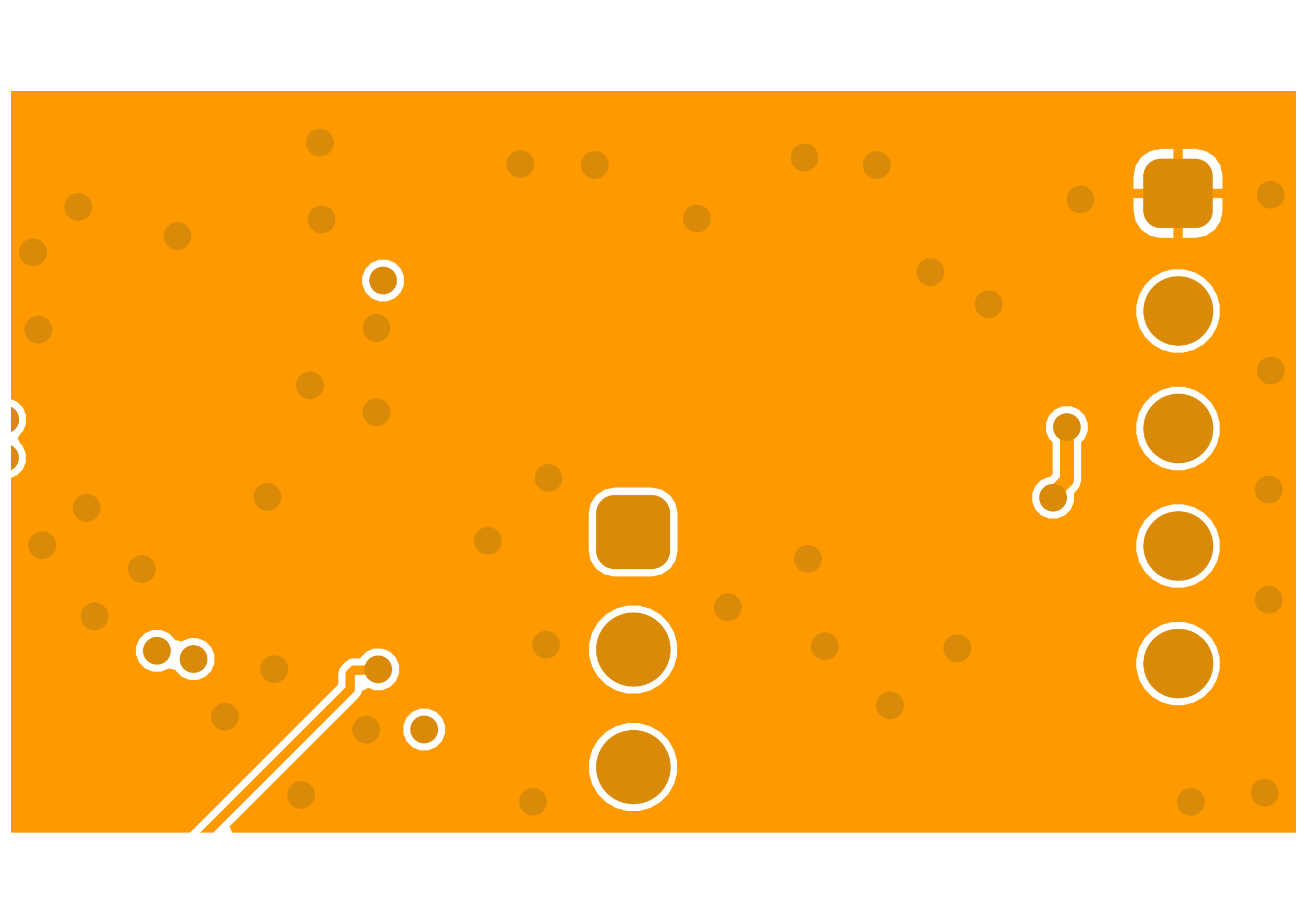
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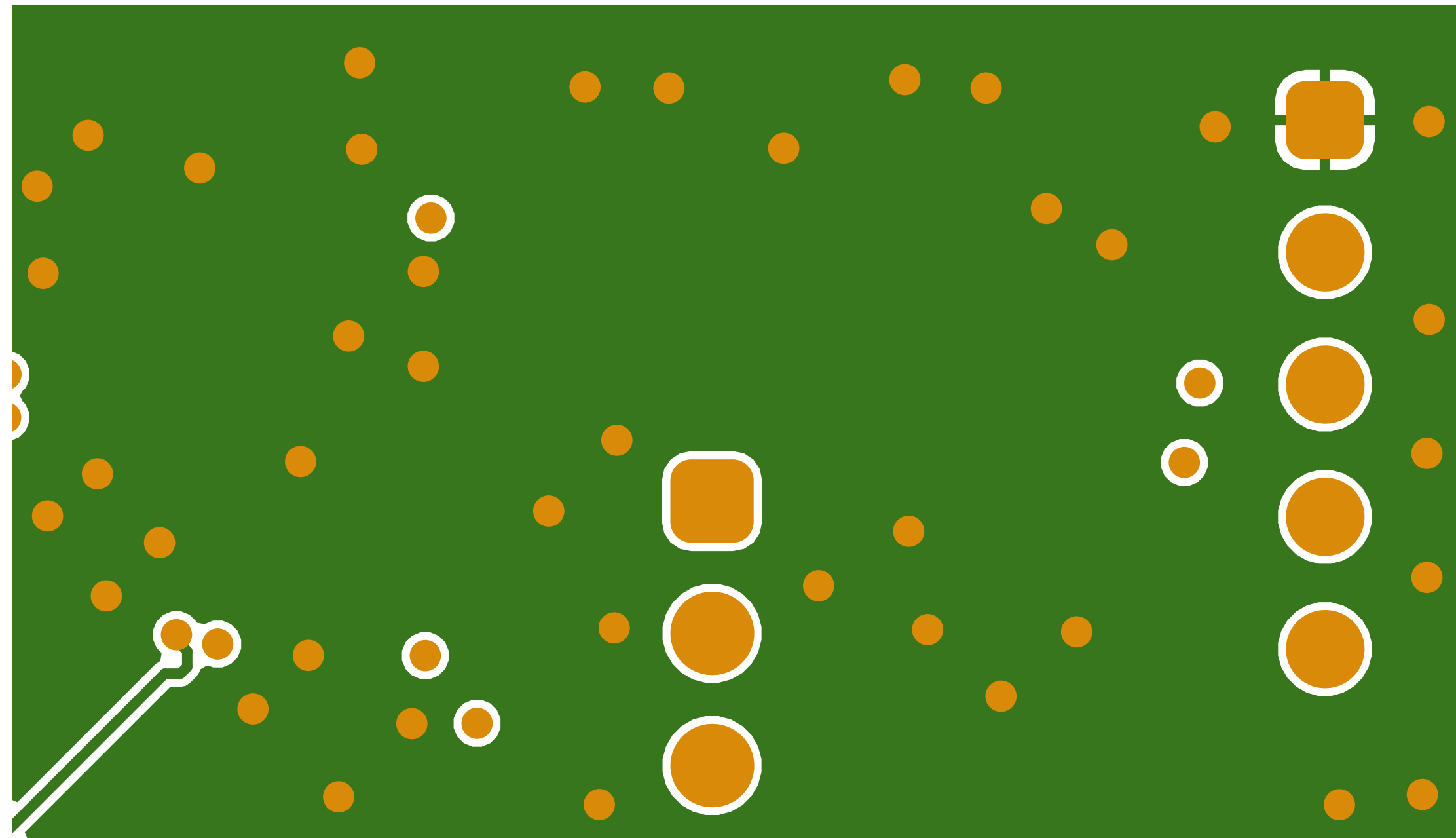


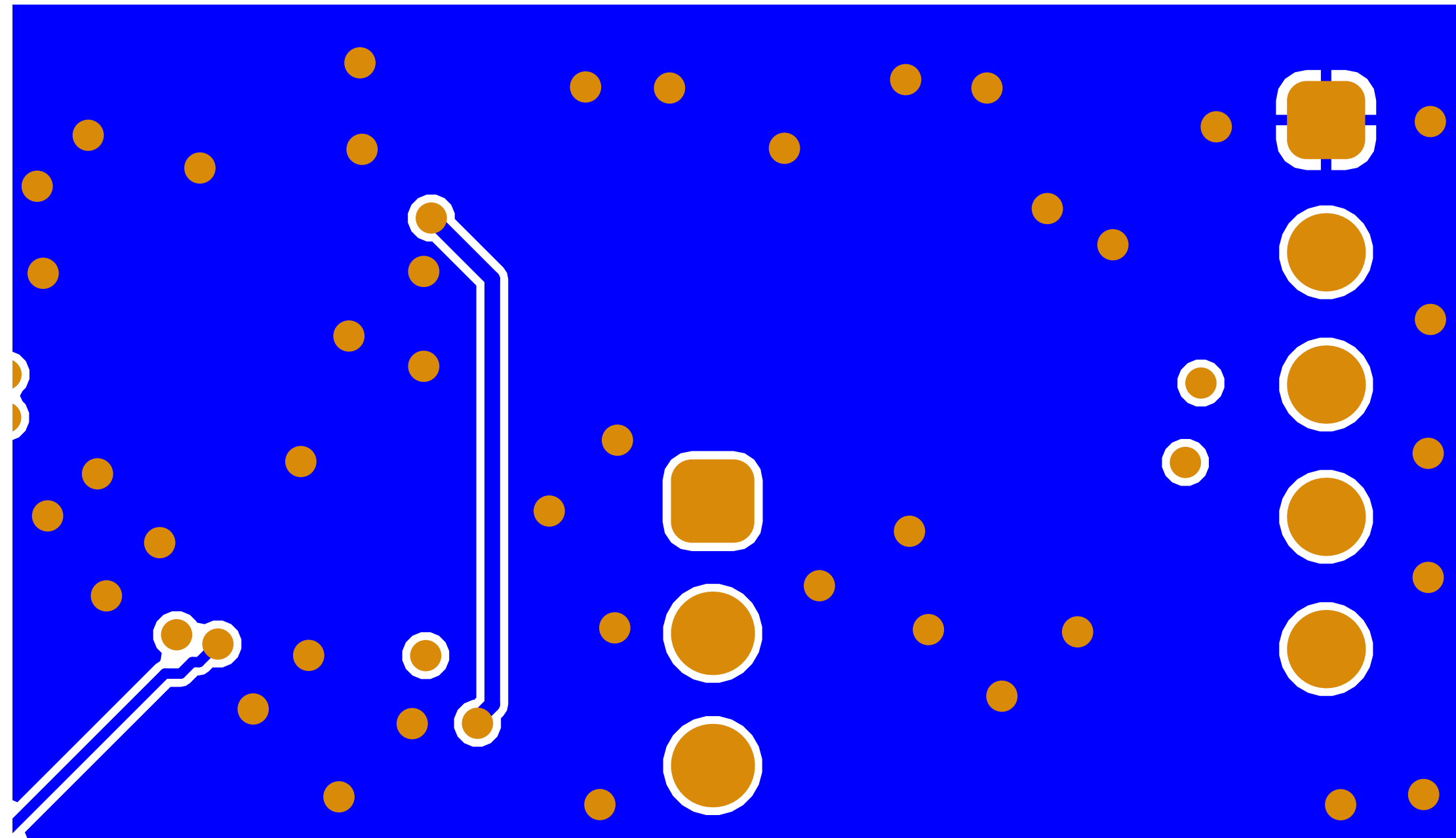
PCB Manufacturing requirements

Project Name	RAA2P4500A80X2
Number of copper layers	4
PCB Base material	FR-4
Final PCB Thickness	1.6 mm (62.9 mil) \pm 10%
Thickness of copper coating	35um
Final cover	ENIG
Minimal copper width	0.2 mm (7.8 mil)
Minimal copper to copper distance	0.15 mm (5.9 mil)
Via hole/pad diameter	0.15 / 0.45 mm (5.90 / 17.7 mil)
Slotted holes	Yes
Panel size	97.5 x 62.5 mm (3838 x 2460 mil)
Silk screen color	White on TOP
Solder mask color	Blue
Blind Vias	No




















Board Stack Report

Stack Up		Layer Stack		
Layer	Board Layer Stack	Name	Material	Thickness
1		Top Overlay		0mm
2		Top Solder	Solder Resist	0.01mm
3		Top Layer		0.035mm
4		Dielectric 1	FR-4	0.32mm
5		Inner1		0.035mm
6		Dielectric2	FR-4	0.8mm
7		Inner2		0.035mm
8		Dielectric3	FR-4	0.32mm
9		Bottom Layer		0.035mm
10		Bottom Solder	Solder Resist	0.01mm
11		Bottom Overlay		0mm
	Height : 1.6mm			

Designator	Value	Quantity	Footprint	Description
C9_Ch1, C9_Ch2, C10_Ch1, C10_Ch2, C11_Ch1, C11_Ch2, C12_Ch1, C12_Ch2, C13_Ch1, C13_Ch2, C14_Ch1, C14_Ch2, C15_Ch1, C15_Ch2, C16_Ch1, C16_Ch2	220pF	16	C0402 3D	Capacitor 0402 220pF X7R
R2_Ch1, R2_Ch2, R5_Ch1, R5_Ch2, R6_Ch1, R6_Ch2, R7_Ch1, R7_Ch2	220R	8	R0402 3D	Resistor 0402 220R <5%
C1_Ch1, C1_Ch2, C3_Ch1, C3_Ch2, C5_Ch1, C5_Ch2	100pF	6	C0603 3D	Capacitor 0603 100pF X7R
C2_Ch1, C2_Ch2, C4_Ch1, C4_Ch2, C6_Ch1, C6_Ch2	470nF	6	C0603 3D	Capacitor 0603 470nF X7R
R3_Ch1, R3_Ch2, R4_Ch1, R4_Ch2, R11_Ch1, R11_Ch2	78263118 2, 0R	6	R0603 3D	Resistor 0603 0R
C17_Ch1, C17_Ch2, C18_Ch1, C18_Ch2	1.8nF	4	C0603 3D	Capacitor 0603 1.8nF NPO
R9_Ch1, R9_Ch2, R10_Ch1, R10_Ch2	10R	4	R0402 3D	Resistor 0402 10R <5%
C7_Ch1, C7_Ch2	330pF	2	C0603 3D	Capacitor 0603 330pF X7R
C8_Ch1, C8_Ch2	10nF	2	C0603 3D	Capacitor 0603 10nF X7R
C19_Ch1, C19_Ch2	2.2nF	2	C0603 3D	Capacitor 0603 150pF X7R
P1_Ch1, P1_Ch2		2	66100511622	WR-WTB Male Vertical Shrouded Header, pitch 2.54mm, 5pins
P2_Ch1, P2_Ch2		2	61300311121	WR-PHD Pin Header, THT, pitch 2.54mm, Single Row, Vertical, 3p
R1_Ch1, R1_Ch2	5.6R	2	R0603 3D	
R13_Ch1, R13_Ch2	12K	2	R0603 3D	Resistor 0603 12k <5%
R17_Ch1, R17_Ch2	NTC	2	R0603 3D	NTCS0603E3103GLT NTC0603 10K

