

RAA489300_EVB_RevB

Contents

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Board silk

Board Name	RAA489300EVAL REV B
PCB No.	
PCB Ver.	
S/N No.	
Country of production	Made IN USA
Logo	RENESAS logo
Display 1	
Display 2	
Display 3	

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The component values are subject to change until Silicon validation without notice.

DISCLAIMER

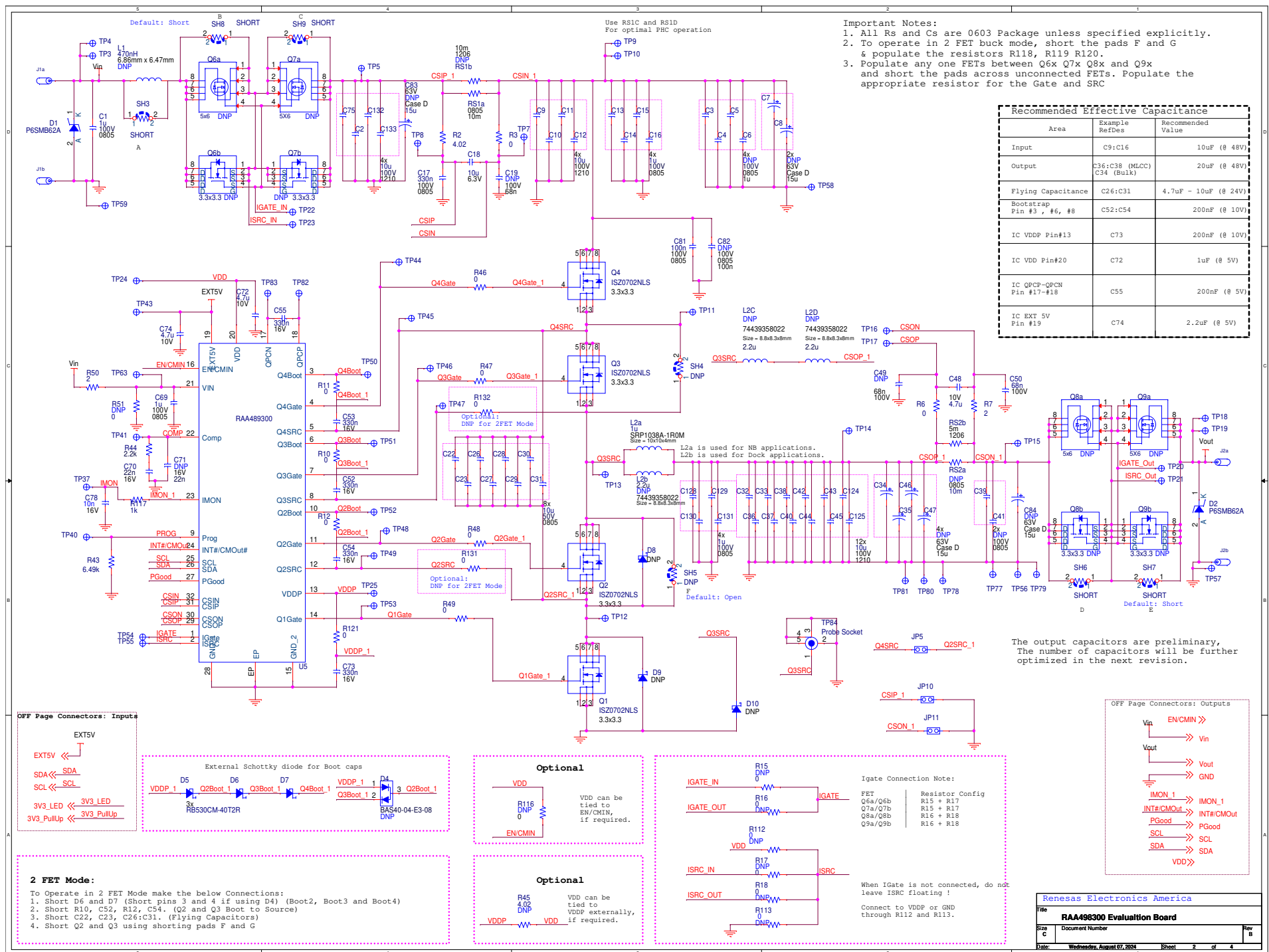
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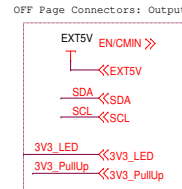
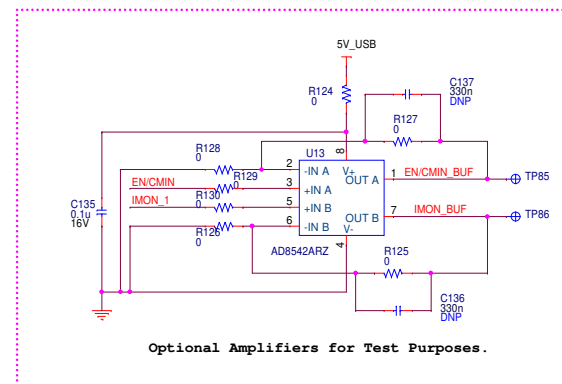
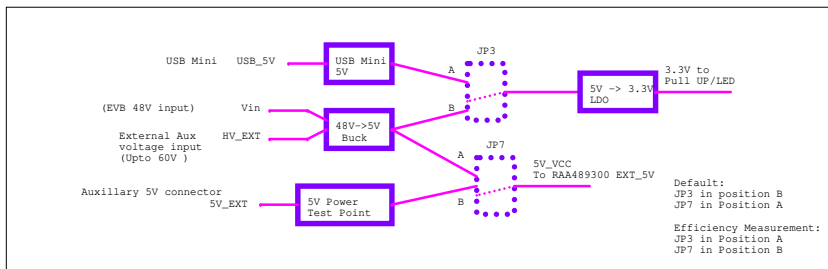
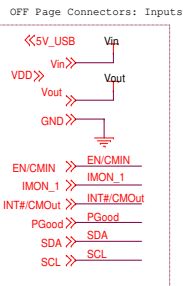
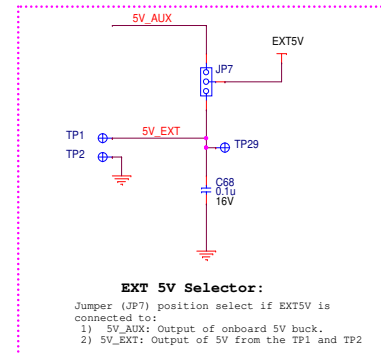
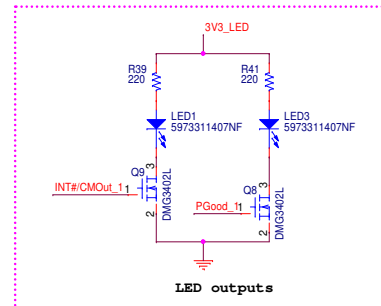
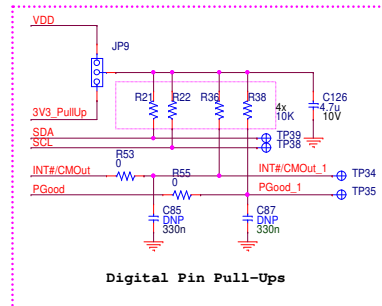
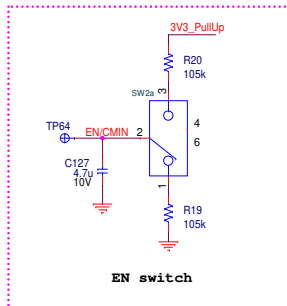
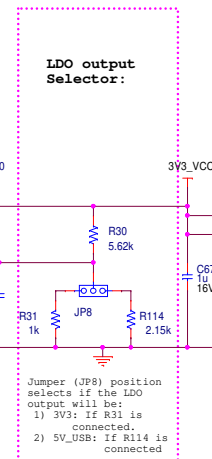
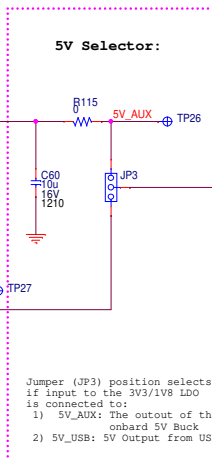
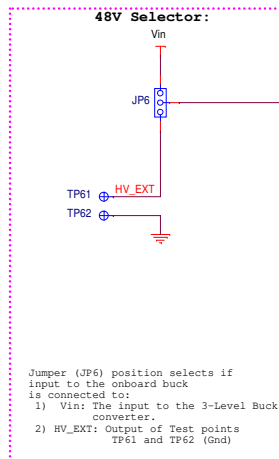
Revision History

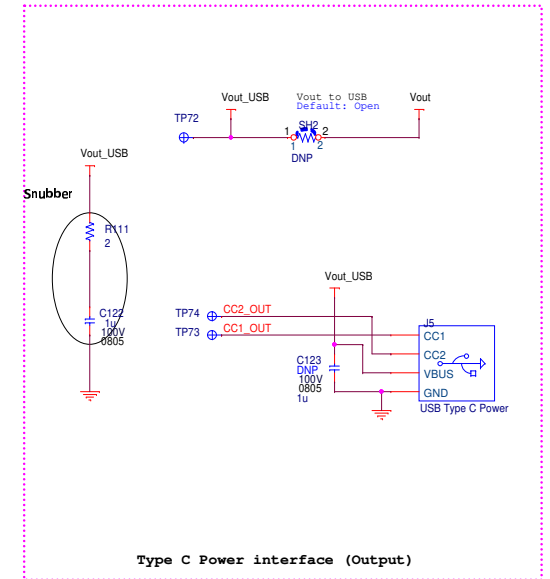
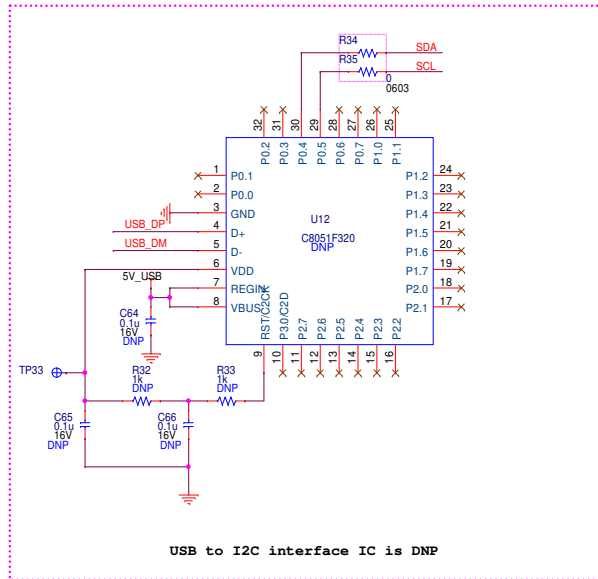
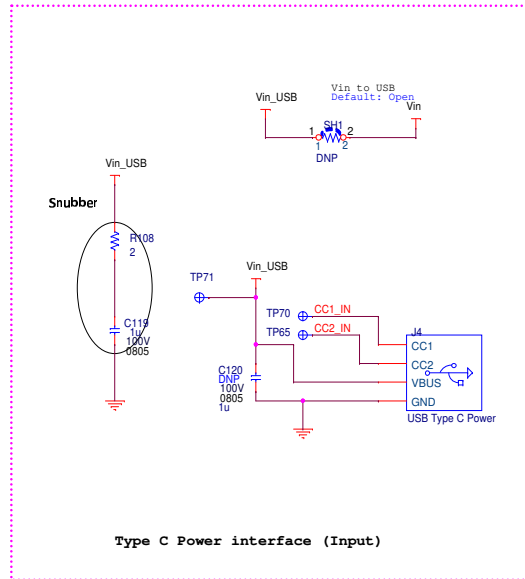
Date	Rev	Description
2022.07.28	0	*First edition
2022.08.04	0v1	Added USB C connectors Made cosmetic changes Included additional pages
2022.09.08	1v0	Resize packages of some Rs and Cs. Rename some nets. Part number change.
2022.09.21	1v1	Added instructions and descriptions for 2 FET mode operation Added jumpers for 2 FET mode
2022.11.07	1v2	Incorporated minor changes from DE review. Modified boot network routing. Modified 2 level configuration
2023.02.06	1v3	Changes by HY Kim Rcomp + C Comp Updated Prog typo Updated CSIP Filters Added Schottky diodes across FETs
2023.03.06	1v4	Rcomp changed to 2.2k Ccomp changed to 22nF Added more input caps on CSIP: 4x10uF Modified CSIP filters for AC loop: 4ohm + 330n Modified Output Capacitors.
2023.05.15	1v5	Cosmetic Overhaul! Added new page to restructure the design. Added support for new USB HiD i2c dongles. Added support for new modified configuration of 2 Level Mode Incorporated Shorting resistors instead of Pads Added Amplifier to buffer outputs in test mode.

Renesas electronics		Approval	
		Check	
Revision	1v8	Creation	Rahul Ramesh
Date	Mar 6, 2023		

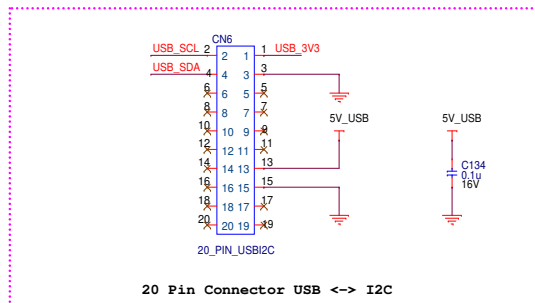
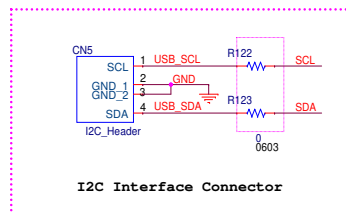
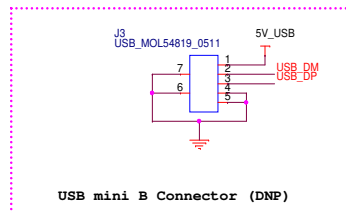
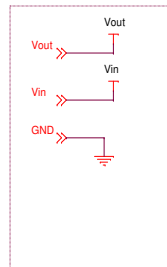
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File	RAA489300_EVB_REV B (Title)	
Size	Document Number	Rev
Date	Tuesday, June 13, 2023	Sheet 1 of 3







OFF Page Connectors: Inputs



OFF Page Connectors: Outputs

