Product Advisor (PA)

Subject: Datasheet Change for the Listed Intersil TW8836* Products
Publication Date: 9/15/2016
Effective Date: 9/15/2016

Revision Description:
Initial Release

Description of Change:
This advisory is to inform you that Intersil has made corrections to the datasheet associated with the listed Intersil TW8836* Products. Details regarding the change are contained on the following page(s).

Affected Products:

TW8836AT-LB2-GE	TW8836AT-LB2-GET	TW8836-BB2-CR	TW8836-LB2-CER5702
TW8836AT-LB2-GER5303	TW8836AT-LB2GETR5303	TW8836-LB2-CE	

Reason for Change:
The corrections align the product characteristics with the associated datasheet. The changes are primarily typo corrections and expansions of register descriptions. Contact your local sales representative for a copy of the latest datasheet.

Impact on fit, form, function, quality & reliability:
The change will have no impact on the form, fit, function, quality, reliability and environmental compliance of the devices.

Product Identification:
There have been no changes to the die/silicon or product itself. There will be no change in the external marking of the packaged parts.

Qualification status: Not applicable; datasheet corrections only
Sample availability: 9/15/2016
Device material declaration: Available upon request

Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Intersil within 30 days of the publication date.

For additional information regarding this notice, please contact your regional change coordinator (below)			
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Page	Contents	Before	After
1	Analog Video Decoder	automatic gain control for the CVBS channel	automatic gain control for the Y or CVBS channel
6,7,8	Pin2, 4 description	YIN2- is on Pin2	YIN2- is on Pin4
6, 7, 14	Pin 114 description		Added FPB0
	Pin 115 description		Added FPB1
	Pin 116 description		Added FPG0
	Pin 117 description		Added FPG1
	Pin 118 description		Added FPR0
	Pin 119 description		Added FPR1
15	Added note 8.		EPAD or exposed DAP (Die Attach Paddle) should be connected to GND for digital ground (VSS) and thermal performance.
16	Thermal Information - for TFBGA Theta JC referencing Note 11: "For ThetaJC, the "case temp" location is taken at the package top center." instead of Note 10.		
12	Pin 66, GPIO06 I/O		I/O
12	Pin 69, GPIO05 I/O		I/O
11	Pin 62, GPIO44 I/O	I/O	I
11	Pin 62, GPIO44 I/O	General Purpose I/O	General Purpose Input Port
13	Pin 86, GPIO41		I/O
	Pin 87, GPIO40		I/O
12	Pin 67 internal connection		-
15	Pin 121, description	MCU Port/UART TXD Output	MCU Port/UART TXD1 Output
15	NOTES:	5. Pull-up resistor 38kΩ (minimum), 54kΩ (typical), 83kΩ (maximum). Pull-up resistors are connected internally to prevent input pin floating when it is open, not to drive external devices. To drive an external device high, a pull-up resistor should be used.	5. Pull-up resistor 38kΩ (minimum), 54kΩ (typical), 83kΩ (maximum). Pull-up resistors are connected internally to prevent input pin floating when it is open, not to drive external devices. To drive an external device high, an external pull-up resistor with 47k ohm should be used. To drive an external device low, an external pull-down resistor with 8.2k ohm max. is recommended.
22	Image Scaling description	and water-glass scaling for displaying 16:9 input on a 4:3 display.	(deletion)
28	Windows#8 register	Window#8 (0x38~0x38F)	Window#8 (0x380~0x38F)
38	SPI Clock Control register bits	SPI Clock Control - 0x4E1 (Bit 5-4), - 0x4E1 (Bit 2-0)	SPI Clock Control - 0x4E1 (Bit 5-4), - 0x4E1 (Bit 3-0)

38	TW8836 MCU feature - Memory description	256 B code cache and 2 k XDATA memory	256 bytes code cache and 2 k bytes XDATA memory
44	Register 009		Addition of 009 as FLAG
45	068[7] name	FD_POL	FD_FOL
	06A name	ENCVDLY	ENCVDLY_LO
	070 default	-	00h
	077 default	04h	00h
46	0B2 default	00h	-
46	0B3 default	00h	-
46	0D4[1] name	DISDLY_POR	DIS_DLY
47	11C[7] name	DTSTUS	DETSTUS
50	206 name	YSCALE[15:8]	YSCALE[15-8]
50	0x20B	HDELAY2	HDELAY2[7-0]
50	210 name	HAPOS_LO[7-0]	HAPOS[7-0]
50	213 name	HSPOS_LO[7-0]	HSPOS[7-0]
50	215 name	VAPOS_LO[7-0]	VAPOS[7-0]
	218 name	VS_POS[5-0]	VSPOS[5-0]
	220[5:4] name	VA_POS_HI	VAPOS[9-8]
	220[3:0] name	VS_POS_HI	VSPOS[9-6]
	221[5:4] name	HA_POS_HI	HAPOS[9-8]
	221[1:0] name	HS_POS_HI	HSPOS[9-8]
51	250[0] name	RSP_PPOS_HI	RSP_PROS[8]
	251 name	RSP_PPOS_LO	RSP_PROS[7-0]
52	2F9[6]	REV_EN	TCREV_EN
	305[0]	I2COSDRAD	I2COSDRAD[8]
	307[7:0]	I2COSDRAD	I2COSDRAD[7-0]
	310[4]		-
61	4DE	4DE[7:6] - 4DE[5:4] DUMMY_EN	4DE[7:5] - 4DE[4] DUMMY_EN
	4DF	4DE[7:6] - 4DE[5:4] WR_CNT_NUM4	4DE[7:5] - 4DE[4] WR_CNT_NUM4
	4F0[3]	W_IMPROVE_MCU	MCU_WAIT_CTRL
	4F2[7]	Keep_ctrl	MCU_SYNC_CTRL
	4F2[6]	Keep reg_ctrl	DMA_SYNC_CTRL
	4F3	I2C_MODE_RG	4F3[7:6] I2C_REG_MEM 4F3[5:4] I2C_DMA_MODE 4F3[3:0] I2C_WR_CNT_NUM
61, 135	4EC[7-1]	RG_DIVDT4	"-" (reserved)
62	Addition of 50C		50C[7] PERIOD_ERR 50C[4] PER_DET_ENA
63	527[7:0]	H_RISE_TO_FALL 7:0]	H_RISE_TO_FALL [7:0]
	529[7:0]	H_RISE_TO_ACT_END [11:0]	H_RISE_TO_ACT_END [7:0]
64	64D[4:0]	64D[4:0] RTUNE	64D[4] RTUNE_ON 64D[3:0] RTUNE
	0x82	DPL	DPL0
	0x83	DPH	DPH0

	0x92 default	00h	07h
65	0xE2		Removed (duplicated)
65	0x9E	0x9E[7:6] UART0FFEN 0x9E[4] UART0FFOVF 0x9E[3:0] UART0FFBYT	0x9E[7] U0EN 0x9E[6:5] - 0x9E[4] U0OV 0x9E[3:0] U0CNT
	0x9F	0x9F[7:6] UART1FFEN 0x9F[4] UART1FFOVF 0x9F[3:0] UART1FFBYT	0x9F[7] U1EN 0x9F[6:5] - 0x9F[4] U1OV 0x9F[3:0] U1CNT
	0xF9		deletion
66	0xxFF[3:0] default	00	0
67	0x008[7:6]	1 = 4mA	1 = 8mA
	0x008[3:0]	A = pwm2 output	A = PWM1 output
	Register 009		Addition of 009 as FLAG
68	0x047[5]	0 = No inversion 1 = Inversion	0 = Rising edge 1 = Falling edge
69	0x04B[7]	Enable delay test	Enable delay line test (fro ATE only)
	0x04B[6]	Swap UART1 function to pin 60, 61	Swap UART1 function to pin 70, 71
70	0x052[5]		ITU656 even field VSYNC delay 0=No delay 1=Delay the even field Vsync by one line
	0x052[2:0]	YpbPr	YPbPr
	0x053[3:0]	4,5: 24-bit 601 or 16/18/24-bit RGB	4,5: 24-bit RGB or YPbPr
71	0x061[6]	Enable 8-bit output in TCON output	Enable 8-bit output in TCON output With this mode, pin #114 ~ #119 become FPB0/FPB1/FPG0/FPG1/FPR0/FPR1 outputs.
72	0x062[7]	Use the value from NPXL, reg062[3:0]#reg063[7:0], for deinterlacer operation	Use the value from NPXL, reg062[3:0]#reg063[7:0], for deinterlacer operation 1= Use the value from NPXL as Hperiod. reg062[3:0]#reg063[7:0], for de-interlacer operation 0= Hperiod follows to input.
	0x067[3]	Reserved	0 = field is not reversed. 1 = field is reversed.
	0x068[4:3]	Delay field toggle position	For test only, use default setting.
	0x068 ENCHDLY_HI	0x068[1:0]	0x068[2:0]
73	0x06A	ENCVDLY	ENCVDLY_LO
	0x07A[3:0]	An 11-bit register.	12-bit register.
	0x07B	An 11-bit register.	12-bit register.

74	0x07C[6]	Enable data value range limit	Enable data value range limit 0: No limit with 0 ~ 255 1: Limit with 16 ~ 235
76	0x0B4[7:4]	Reserved	0x0B4[7] TSC_DBG, Reserved
77	0x0D4[2]	PL_LSO	PD_LSO
	0x0D4[0]	PL_LSO	PD_POR
	0x0D6[7]	(None)	Reserved
78	0x0ED[5:4]	3 = 108 ~ 216 MHz	3 = 108 ~ 150 MHz
79	0x0F8[7:4]	Reserved	0x0F8[7:6] CLK_SEL, Reserved 0x0F8[5:4] Reserved
81	0x105[3] and [2]		Not used. Set to 0.
	0x106[6]		Internal current reference selection of AFE. Use as default value.
	0x106[5]		Voltage reference selection of ADC. Use as default value.
83	0x111	They have value of 0 to 2.55 (FFh).	They have value of 0 to 255 (FFh).
84	0x11A[7]	CCVLDEN	Reserved
87	0x134[5:0] default	1A/20/1C/2A	1A/20/1C/11
92	0x1E1[6]	GPLL freq multiplication select, 1: X2	GPLL freq multiplication select, 0 = X4 1 = X8
93	0x1E6[7:6]	3 = 2X	3 = N/A
94	0x1E9[1]	LLCLK polarity control. 1 = Inversion	Reserved
	0x1E9[0]	Deinterlacer mode clock control. 1 = Enable deinterlacer	Reserved
	0x1F6[1-0]	Internal use only, set to default value	0~2 = Reserved 3 = Continuous common-mode restore
	0x1F8[2:0]	0 = YIN0 1 = YIN12 = YIN2 3 = YIN3 4 = CIN0 5 = CIN16 = VIN0 7 = SOG0	0 = YIN0 1 = YIN1 2 = YIN2 3 = YIN3 4 = CIN0 5 = CIN1 6 = VIN0 7 = SOG0
95	0x1F9[2:0]	0 = YIN0 1 = YIN12 = YIN2 3 = YIN3 4 = CIN0 5 = CIN16 = VIN0 7 = SOG0	0 = YIN0 1 = YIN1 2 = YIN2 3 = YIN3 4 = CIN0 5 = CIN1 6 = VIN0 7 = SOG0
	0x201 PWEN description	1 = Enable Panoramic/water glass display	1 = Enable Panoramic display
	0x203	XSCALE_LO	XSCALE[7-0]
96	0x204	XSCALE_HI	XSCALE[15-8]
	0x205	YSCALE_LO	YSCALE[7-0]
	0x206	YSCALE_HI	YSCALE[15-8]
	0x207	PXSCALE	PXSCALE[15-8]

	0x207 description	Initial Scaling value for the Panoramic/water glass display in increment of 4. MSB 8-bit of a 12-bit register.	Initial Scaling value for the Panoramic display in increment of 4. MSB 8-bit of a 12-bit register.
	0x209	HDSCALE	HDSCALE[7-0]
	0x208	Increment step value for the Panoramic/water glass display.	Increment step value for the Panoramic display.
	0x20A[3:0]	HDSCALE_HI	HDSCALE[11-8]
	0x20C	HACTIVE2	HACTIVE2[7-0]
	0x20B	HDELAY2	HDELAY2[7-0]
	0x20D[7:6]	LNTT_HI	LNTT[9-8]
	0x20E[6:4]	HACTIVE2_HI[10-8]	HACTIVE2[10-8]
	0x20E[3:0]	HPADJ_HI	HPADJ[11-8]
	0x20F	HPADJ_LO	HPADJ[7-0]
98	0x21E[3]	1 = Main scaler line buffer bypass	1 = Main scaler line buffer bypass 0 = non-bypass
	0x220[5:4]	VA_POS_HI	VAPOS[9-8]
	0x220[3:0]	VS_POS_HI	VSPOS[9-6]
	0x221[5:4]	HA_POS_HI	HAPOS[9-8]
	0x221[1:0]	HS_POS_HI	HSPOS[9-8]
	0x240[7:4]	CS_WID	CSP_WID
	0x243[6:4]	RCK_POS_HI	RCK_POS[10-8]
	0x243[2:0]	RCK_WID_HI	RCK_WID[10-8]
	0x244	RCK_POS_LO	RCK_POS[7-0]
	0x245	RCK_WID_LO	RCK_WID[7-0]
	0x246[5:4]	ROE_POS_HI	ROE_POS[9-8]
	0x246[2:0]	ROE_WID_HI	ROE_WID[10-8]
99	0x247	ROE_POS_LO	ROE_POS[7-0]
	0x248	ROE_WID_LO	ROE_WID[7-0]
	0x249[2:0]	RSP_POS_HI	RSP_POS[10-8]
	0x24A	RSP_POS_LO	RSP_POS[7-0]
	0x24B[6:4]	CPL_POS_HI	CPL_POS[10-8]
100	0x210	HA_POS	HA_POS[7-0]
	0x211	HALEN_LO	HALEN[7-0]
	0x212[7:4]	PXSCALE	PXSCALE[3-0]
	0x212[3:0]	HALEN_HI	HALEN[11-8]
	0x213	HS_POS_LO	HS_POS[7-0]
	0x214	HS_LEN	HSLEN
	0x215	VA_POS_LO	HS_POS[7-0]
	0x216	HALEN_LO	HALEN[7-0]
	0x217[7:4]	PXINC[11:8]	PXINC[11-8]
	0x217[3:0]	HALEN_HI	HALEN[11-8]
	0x218[7:6]	VS_LEN	VSLEN
	0x218[5:0]	VS_POS	VSPOS[5-0]
	0x219	LNTT_LO	LNTT[7-0]
	0x21C[7:4]	HTOTAL_HI	HTOTAL[11-8]
	0x21D	HTOTAL_LO	HTOTAL[7-0]

	0x24C	CPL_POS_LO	CPL_POS[7-0]
	0x250[0]	RSP_PPOS_HI	RSP_PPOS[8]
	0x251	RSP_PPOS_LO	RSP_PPOS[7-0]
101	0x28C[7]	SH_FREQS	SH_FREQ
102	0x2BF[6:4]	RGB/YcbCr byte swap for color change	RGB/YcbCr byte swap for color change 0 = RGB (default) 1 = GBR 2 = BRG 3 = RBG 4 = GRB 5 = BGR 6, 7 = N/A
104	0x2F9[6]	REV_EN	TCREV
	0x2F9[6]	1: REV output	1: TCREV output
	0x300[1]	FONT_SWITC	FONT_SWITCH
105	0x306	I2COSDRAD	I2COSDRAD[7-0]
117	0x400[2]	0 = Disable all SPIOSD windows	0 = Disable SPIOSD operation 1 = Enable SPIOSD operation
131		0x04B7 – High Byte Register	0x4B7 – High Byte Register
132	0x4C2[1]	I2C to XMEM DMA Status	I2C to XMEM DMA Status 0 = I2C cannot access XMEM 1 = I2C can access XMEM
	0x4C2[0]	Enable I2C to XMEM DMA	Enable I2C to XMEM DMA 0 = Disable XMEM access by I2C 1 = XMEM access by I2C enabled
	0x4C3[3:0]	DMA Command length low byte	DMA Command length low byte Set number of command for DMA operation with 0x4F2[4]#0x4C3[3:0]
	0x4C5[7:4]	DMA read wait cycle	DMA read wait cycle. Use default value
	0x4C5[3:0]	SPI read/write wait cycle	SPI read/write wait cycle. Use default value
133	0x4D9[3]	0 = Low 1 = High	0 = Low 1 = High (Normal)
	0x4D9[2:0]	Busy bit in status command	Busy bit location in SPI status register. Normally '0'.
134	0x4DE[4]	DUMMY ENABLE	DUMMY_EN
	0x4DF[4]	DMA_LENGTH	WR_CNT_NUM4
	0x4DF[4]	DMA Command write byte count bit4	DMA Command length bit4
	0x4E0[0]	0 = Select PCLK from PCLK divider 1 = Select 108M	Select SPICLK/MCUCLK source either from SSPLL1/SSPLL2 (which is selected by 0x04B[5]) or 108MHz 0 = SSPLL1/SSPLL2 1 = 108MHz

	0x4E1[5:4]	SPI clock selection 0 = System clock (27MHz) 1 = Internal R-C oscillator (32kHz) 2 = PCLK	SPI and MCU clock source selection 0 = System clock (27MHz) 1 = Internal R-C oscillator (32kHz) 2 = PCLKSelected clock by 4E0[0] (either SSPLL1, SSPLL2 or 108MHz)
	0x4E1[3:0]	PLL clock divider	SPICLK/MCUCLK clock divider
135	0x4E8	Timer3 Divider High Byte Registers	UART0 baud rate clock divider high byte
	0x4E9	Timer3 Divider Low Byte Registers	UART0 baud rate clock divider low byte
	0x4EA	Timer4 Divider High Byte Registers	UART1 baud rate clock divider high byte
	0x4EA	TIMER4 BAUD RATE CLOCK DIVIDER HIGH BYTE REGISTER	UART1 BAUD RATE CLOCK DIVIDER HIGH BYTE REGISTER
	0x4EB	Timer4 Divider Low Byte Registers	UART1 baud rate clock divider low byte
	0x4EB	TIMER4 BAUD RATE CLOCK DIVIDER LOW BYTE REGISTER	UART1 BAUD RATE CLOCK DIVIDER LOW BYTE REGISTER
142	0x641[7]	Load/Shift signal polarity selection 0 =Active High 1= Active Low	This bit is used by the LVDSTX analog to select when to load the byte data into the serializer. 0=Load on falling edge of pclk 1=Load on rising edge of pclk
	0x641[4]	Reserved data output 0=Normal data output format 1=Reserved data output format	Reserved data output order 0=Normal data output order 1=Reserved 7bit data output order
	0x642[7-6]	Charge pump control	Charge pump current control 0 =1uA 1=5uA 2=10uA 3=15uA
	0x642[5-4]	Low pass filter control	Low pass filter phase margin adjustment 0 = Normal 1 = 5pF added 2,3 = N/A
143	0x647[1-0]	Output current control	LVDS output swing: 0 = 210mV 1,2 = 280mV 3 = 350mV
145	0x64F[5:0]	Reserve control bits	Reserved control bits
145 ~ 146	SFR		Moved around in address order
145	0x8C	Timer 1, high byte	Timer 0, high byte
146	0x9E[3-0], 0x9F[3-0]	R/W	R

147	0xF9		(removed)
148	0xFA	It cannot be set by software Interrupt Vector Address.	It cannot be set by software Interrupt Vector Address listed below.