# Product Advisory Notice (PA)

**Subject:** Datasheet Specification Change for Listed Intersil ISL78322ARZ* Products
**Publication Date:** 12/1/2016
**Effective Date:** 12/1/2016

**Revision Description:**
Revision a: corrected header only, changed from PA16092 to PA16098; no other changes to the document

**Description of Change:**
This notice is to inform you that Intersil has updated the datasheet to remove the skip mode function (PFM) and associated documentation from the datasheet. The change applies to the following products:

| | | |
|---|---|---|
| ISL78322ARZ | ISL78322ARZ-T | ISL78322ARZ-T7A |
| ISL78322ARZ-TR5303 | ISL78322ARZ-TR5492 | ISL78322ARZ-TR5506 |

**Reason for Change:**
Skip mode is no longer supported and is not recommended for use in new designs. No change is required for existing designs. Details regarding the change are contained on the following pages. The updated data sheet is available on the Intersil web site at:
http://www.intersil.com/content/dam/intersil/documents/isl7/isl78322.pdf

**Product Identification:**
There have been no changes to the die/silicon or product itself. There will be no change in the external marking of the packaged parts. Product affected by this change is identifiable via Intersil's internal traceability system.

**Qualification status:** Not applicable
**Sample availability:** 12/1/2016
**Device material declaration:** Available upon request

*Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Intersil within 30 days of the publication date.*

| For additional information regarding this notice, please contact your regional change coordinator (below) | | | |
|---|---|---|---|
| Americas: PCN-US@INTERSIL.COM | Europe: PCN-EU@INTERSIL.COM | Japan: PCN-JP@INTERSIL.COM | Asia Pac: PCN-APAC@INTERSIL.COM |

# Datasheet Change Summary

- Updated Title and Features

From:

Dual 2A/1.7A Low Quiescent Current 2.25MHz High Efficiency Synchronous Buck Regulator

**Features**

- Dual 2A/1.7A high efficiency synchronous buck regulator with up to 97% efficiency, low $I_Q$ (40µA)
- 180° out-of-phase outputs reduce ripple current and EMI
- Start-up with prebiased output prevents negative current flow in output stage
- Selectable forced PWM mode and PFM mode
- External synchronization up to 8MHz
- Negative current detection and protection
- 100% maximum duty cycle for lowest dropout
- Internal current mode compensation
- Peak current limiting, hiccup mode short circuit protection and over-temperature protection
- Pb-free (RoHs compliant)
- AEC-Q100 qualified component

To:

Dual 2A/1.7A, 2.25MHz High-Efficiency, Synchronous Buck Regulator

**Features**

- Dual 2A/1.7A high-efficiency, synchronous buck regulator with up to 97% efficiency
- 2.8V to 5.5V input supply range
- 180° out-of-phase outputs reduce ripple current and EMI
- Start-up with prebiased output prevents negative current flow in output stage
- External synchronization up to 8MHz
- Negative current detection and protection
- 100% maximum duty cycle for lowest dropout
- Internal current mode compensation
- Peak current limiting, hiccup mode short-circuit protection, and over-temperature protection
- Pb-free (RoHs compliant)
- AEC-Q100 qualified component



**Applications**

- DC/DC POL modules
- µC/µP, FPGA, and DSP power
- Automotive embedded processor power supply systems

**Related Literature**

- For a full list of related documents, visit our website

- Removed all Skip Mode (PFM) information from document including text and figures:
  a. Removed Quiescent Supply Current (top row only) from Electrical table
  b. Removed Peak Skip Limit from Electrical table
  c. Removed SYNC Logic Input Leakage Current from Electrical table
  d. Removed Skip Mode section.
  e. Updated Figures 1, 3, and 6 through 12 to remove “PFM”.

- Updated Exposed Pad pin description on page 4.

FROM:

| PIN NUMBER | SYMBOL | DESCRIPTION |
|---|---|---|
| - | EXPOSED PAD | The exposed pad must be connected to the SGND pin for proper electrical performance. Add as much vias as possible for optimal thermal performance. |

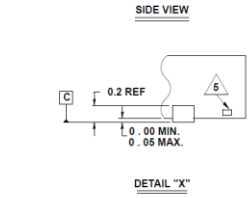
TO:

| PIN NUMBER | SYMBOL | DESCRIPTION |
|---|---|---|
| - | EXPOSED PAD | The exposed pad must be connected to the PGND1 and PGND2 pins for proper electrical performance. Add as many vias as possible for optimal thermal performance. |



- Updated POD L12.4x3

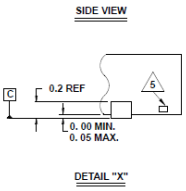
FROM:




NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.

To:

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3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).