4-Lane 4-Port Gen2 PCI Express® Switch

89HPES4T4G2
Product Brief

Device Overview

The 89HPES4T4G2, a 4-lane 4-port Gen2 PCI Express® switch, is a member of IDT's PRECISE™ family of PCI Express switching solutions. The PES4T4G2 is a peripheral chip that performs PCI Express Base switching with a feature set optimized for servers, storage, communications, and consumer applications. It provides connectivity and switching functions between a PCI Express upstream port and three downstream ports or peer-to-peer switching between downstream ports.

Features

- High Performance PCI Express Switch
  - *Four Gen2 PCI Express lanes supporting 5 Gbps and 2.5 Gbps operations*
  - *Four switch ports*
    - *One x1 upstream port*
    - *Three x1 downstream ports*
  - *Low latency cut-through switch architecture*
  - *Support for Max Payload Size up to 256 bytes*
  - *Supports one virtual channel and eight traffic classes*
  - *PCI Express Base Specification Revision 2.0 compliant*
- Flexible Architecture with Numerous Configuration Options
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion*
  - *Ability to load device configuration from serial EEPROM*
- Legacy Support
  - *PCI compatible INTx emulation*
  - *Bus locking*
- Highly Integrated Solution
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates four 5 Gbps embedded SerDes with 8b/10b encoder/decoder (no separate transceivers needed)*
    - *Receive equalization (RxEQ)*
- Reliability, Availability, and Serviceability (RAS) Features
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports ECRC and Advanced Error Reporting*
  - *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
  - *Compatible with Hot-Plug I/O expanders used on PC motherboards*
  - *Supports Hot-Swap*
- Power Management
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Support PCI Power Management Interface specification (PCI-PM 2.0)*

Block Diagram

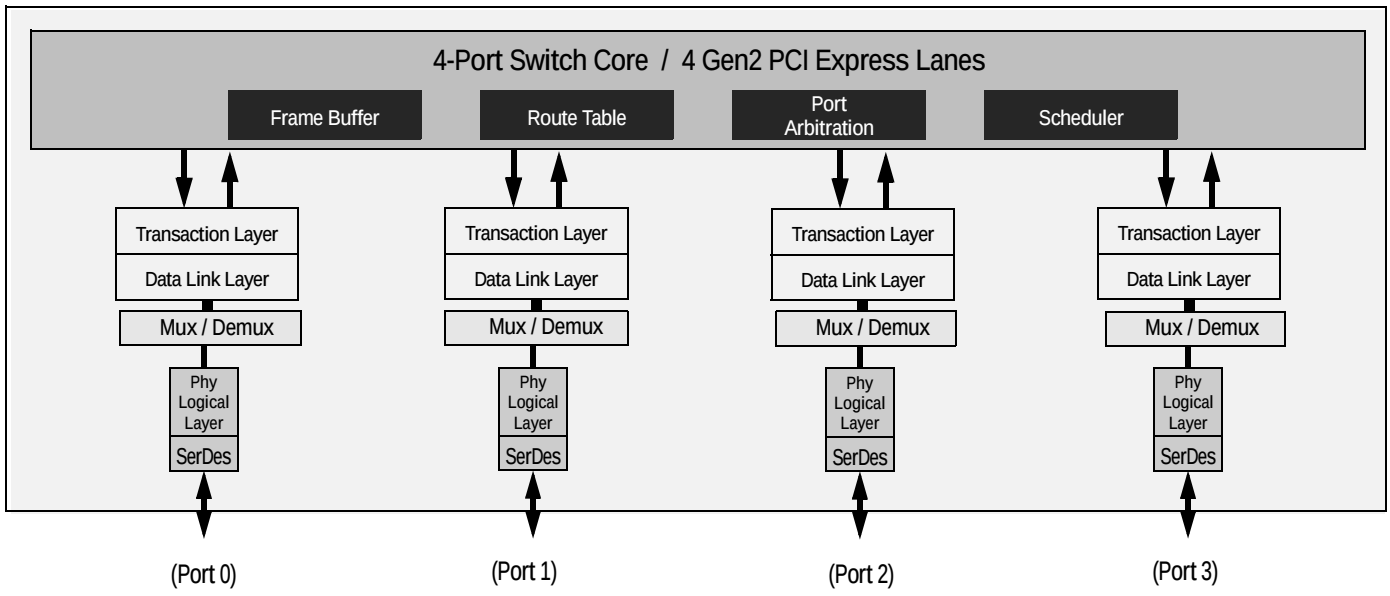

Figure 1 Internal Block Diagram

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- *Supports device power management states: D0, $D3_{hot}$ and $D3_{cold}$*

– *Support for PCI Express Active State Power Management (ASPM) link state*

- *Supports link power management states: L0, L0s, L1, L2/L3 Ready and L3*

– *Supports PCI Express Power Budgeting Capability*

– *Configurable SerDes power consumption*

- *Supports optional PCI-Express SerDes Transmit Low-Swing Voltage Mode*
- *Supports numerous SerDes Transmit Voltage Margin settings*

– *Unused SerDes are disabled*

◆ Testability and Debug Features

– *Built in Pseudo-Random Bit Stream (PRBS) generator*

– *Numerous SerDes test modes*

– *Ability to read and write any internal register via the SMBus*

– *Ability to bypass link training and force any link into any mode*

– *Provides statistics and performance counters*

◆ General Purpose Input/Output Pins

– *Each pin may be individually configured as an input or output*

– *Each pin may be individually configured as an interrupt input*

– *Some pins have selectable alternate functions*

◆ Packaged in a 19mm x 19mm, 324-ball BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect the PES4T4G2 provides the most efficient high-performance I/O connectivity device for applications requiring high throughput, low latency and simple board layout. It provides PCI Express connectivity across 4 lanes and 4 ports. Each lane provides 5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 2.0.

The PES4T4G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 2.0. The PES4T4G2 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

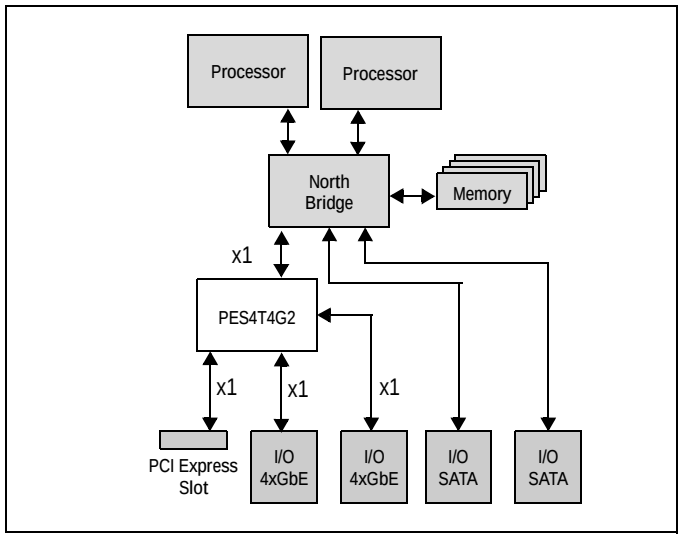

Figure 2 I/O Expansion Application

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