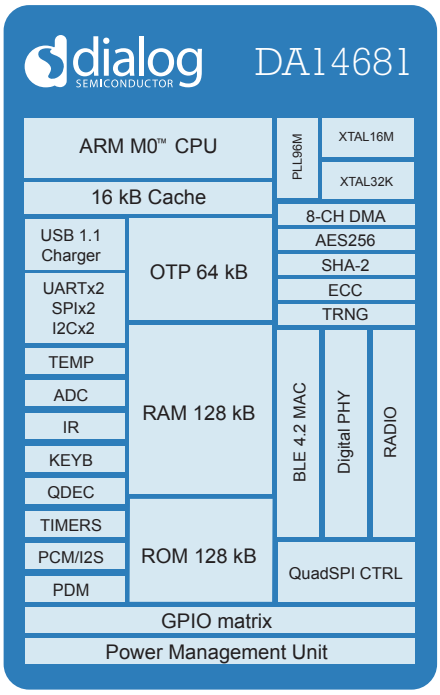
SmartBond™ DA14681

The most integrated and flexible Bluetooth® low energy SoC with expandable memory execution space

Create next-generation Bluetooth low energy solutions without compromising on functionality or battery lifetime, thanks to Dialog's SmartBond DA14681.

It's the world's first single-chip solution for wearables, smart home and other rechargeable devices. This highly integrated solution supports the full Bluetooth 4.2 features. As a SmartBond device, it offers the highest performance, lowest power consumption and smallest footprint. Delivering processing capacity when you need it and saving power when you don't, it can manage multi-sensor arrays and enable always-on sensing. Plus our **SmartSnippets™** tooling helps you optimize your software for power consumption.

With an integrated Power Management Unit comprising system power rails, a battery charger and a fuel gauge, it supports rechargeable batteries natively and can power a complete sensor-based system. Meanwhile, a dedicated hardware crypto engine delivers banking-level security (including Apple HomeKit support) with end-to-end encryption to keep personal data safe.



Applications

- (Multi-sensor) wearable devices:
  - Fitness / activity trackers
  - Sport watches
  - Smartwatches
- Smart home
- Consumer appliances
- Home automation
- Voice-controlled remote controls
- Rechargeable keyboards
- Toys
- Industrial automation

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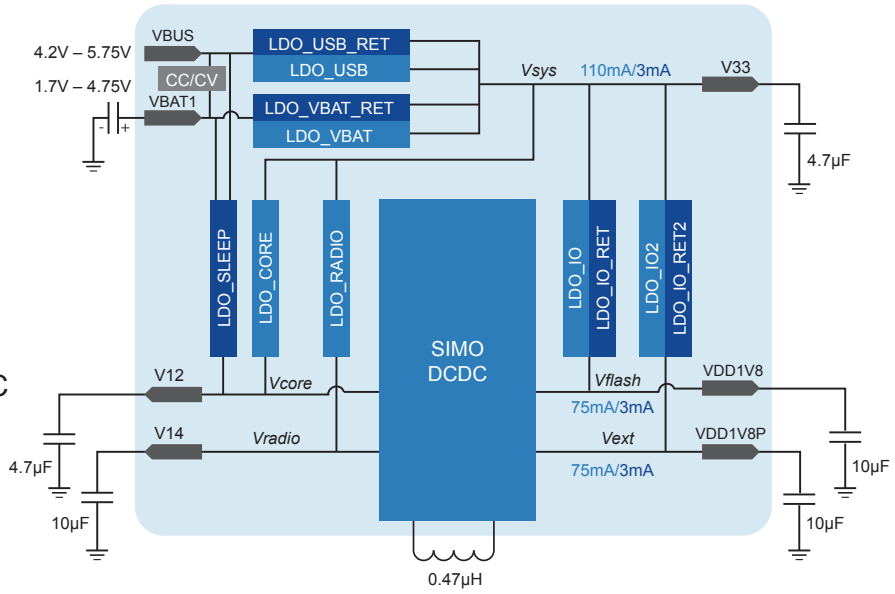
SoC Features

- Complies to Bluetooth 4.2, ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan)
- Flexible processing power
  - 32 kHz up to 96 MHz 32-bit ARM Cortex-M0 with 16 kBytes, 4-way associative cache
  - Three optimised power modes (Extended sleep, Deep sleep and Hibernation) reducing current down to 840 nA
- Memories
  - 64 kB One-Time-Programmable (OTP) memory
  - 128 kB Data SRAM with retention capabilities
  - 16 kB Cache SRAM with retention capabilities
  - 128 kB ROM (including boot ROM and Bluetooth low energy stack)
  - Execution from external QSPI FLASH up to 32 MB
- Power management
  - Integrated Buck DC-DC converter (1.7 V - 4.75 V)
  - Three power supply pins for external devices
  - Supports Li-Polymer, Li-Ion, coin cells, NiMH and alkaline batteries
  - Charger (up to 5.0 V) with programmable curves
  - High accuracy state-of-charge fuel gauge
  - Programmable threshold for brownout detection
- Clocks
  - 16 MHz crystal and RC oscillators
  - 32 kHz crystal and RC oscillators
  - 10.5 kHz RCX oscillator as a 32 kHz crystal replacement
  - Low power PLL up to 96 MHz
- Three general purpose timer/counters with PWM, one of them 16-bit up/down timer/counter with PWM available in extended sleep mode
- Application cryptographic engine with ECC, AES-256, SHA-1, SHA-256, SHA-512 and a FIPS 140-2-compliant True Random Number Generator
- Digital interfaces
  - 37 (AQFN) or 21 (WL-CSP) general purpose I/Os with programmable voltage levels
  - Quad-SPI FLASH interface
  - Two UARTs, one with hardware flow control
  - Two SPI+™ interfaces
  - Two I²C bus interfaces at 100 kHz, 400 kHz
  - Three-axis capable Quadrature Decoder
  - PDM interface with HW sample rate converter (2 mics or 2 speakers)
  - I²S/PCM master/slave interface up to 8 channels
  - Keyboard scanner with de-bouncing
  - Infrared (IR) interface (PWM)
  - USB Full Speed (FS) device interface

- Analog interfaces
  - 8-channel 10-bit ADC with averaging capability achieving 11.5 ENOB
  - Three matched white LED drivers
  - Temperature sensor
- Radio transceiver
  - 2.4 GHz CMOS transceiver with integrated balun
  - 50 Ω matched single wire antenna interface
  - 0 dBm transmit output power and -94 dBm receiver sensitivity
  - Supply current at VBAT1 (3 V): 3.4 mA (TX), 3.1 mA (RX)
- Packages
  - AQFN with 60 pins, 6 mm x 6 mm x 0.9 mm
  - WL-CSP with 53 balls, 3.406 mm x 3.010 mm x 0.5 mm

Power Management

There are 3 power rails that can be used to supply external devices namely V_{sys}, V_{flash} and V_{ext}. There are also internal rails used for the core and the radio (V_{core} , V_{radio}). All of the rails are supplied by a normal LDO, a Retention LDO or one of the outputs of the Single Inductance Multiple Output (SIMO) DCDC converter. When the SoC is active, the DCDC is enabled. When the SoC is in sleep mode, then the Retention LDOs are supplying the rails. The normal LDOs are used while powering up the system or during transitions from active to sleep and vice-versa.



The driving capability of the various rails is depicted in the figure: light blue for active, dark blue for sleep. LDOs as well as DCDC outputs can be switched on/off depending on the application's requirements. A flexible Constant Current / Constant Voltage (CC/CV) charger supplying currents from 200 uA to 400 mA allows for native re-chargeable batteries support. Finally, a State-of-Charge engine, monitors the remaining capacitance of the battery when the system is active. The Power Management Unit reduces Bill of Material and enables full control of the power budget of the final product.

Application CPU

The ARM M0™ CPU is equipped with a configurable 16 kB cache which can operate in direct, two-way or four-way associative mode. Moreover, the cache line size can be programed to be 8, 16 or 32 bytes. The SoC allows for eXecute In Place (XIP) operation directly from the QSPI FLASH (up to 32 MB) or the OTP. There are 2 separate buses, one serving the code execution path (CPU, FLASH) and another which serves data storage (DMA, Peripherals) hence eliminating latencies in application execution. The CPU can be clocked by the XTAL16 crystal oscillator (16 MHz), or by a low-power internal PLL which boosts the frequency to 96 MHz, enabling complex applications or algorithms without the use of an external or dedicated MCU.

System Booting

The DA14681 supports booting from a serial interface or from a non-volatile memory (QSPI FLASH or OTP). It also comes with a pre-defined header residing in OTP which contains configuration flags but also trim values and preferred settings programmed during silicon manufacturing and/or final product testing by the customer. Booting latency might vary from 15 ms (NVM booting path) to some hundreds of ms (serial path) depending on the serial interface used and the speed/size of the booting transaction.

Sleep Modes

The DA14681 comprises multiple power domains which are powered by the Vcore rail and can be switched on or off by software. This flexibility combined with manipulating clocks and retainable RAM cells, leads to the three different sleep modes of the system: Extended Sleep, Deep Sleep and Hibernation. The first mode is used between Bluetooth low energy activities, the second is a clock-less mode with RAM retained (used to store pairing parameters) while the third is a clock-less mode with all RAM off, achieving the minimum current dissipation.

Software and Tools

The DA14681 is supported by Dialog SmartSnippets Studio, a royalty-free software development platform for all SmartBond devices, which contains:

- SmartSnippets Toolbox: A tool suite covering all software developer needs, including power profiling, FLASH or OTP programming and testing
- SmartSnippets IDE: An Eclipse CDT based IDE pre-configured plugins allowing easy out of the box set-up of the build/debug environment
- SmartSnippets DA1468x Software Development Kit and Documentation

Specification Parameters

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{BAT}	Supply voltage	Recommended operating condition	1.7		4.75	V
I_{BAT_IDLE}	Supply current	CPU is idle (WFI), DCDC on, VBAT=3V	0.4	0.6	1	mA
$I_{BAT\_RUN\_16MHz}$	Supply current	CPU executes code from RAM, DCDC on, peripherals on, VBAT=3V	1.2	1.4	1.9	mA
$I_{BAT\_RUN\_96MHz}$	Supply current	CPU executes code from RAM, DCDC on, peripherals on, VBAT=3V	5.7	6.2	6.9	mA
$I_{BAT\_EXT\_SLP}$	Supply current	Cache (16kB) and Data (32kB) retained. XTAL32k used. FLASH in power down.	1.7	2.6	14.7	µA
$I_{BAT\_DP\_SLP}$	Supply current	All clocks off. FLASH off. 24kB RAM retained.	1.5	2.4	13.8	µA
I_{BAT_HIBERN}	Supply current	All clocks off. FLASH off. No RAM retained.	0.6	0.7	5.8	µA
P_{SENSE}	Radio sensitivity level	Normal operating conditions; PER=30.8%; DCDC disabled		-94		dBm
P_{INT_IMD}	Radio Intermod. distortion interferer	Worst case interferer level	-35	-31		dBm
P_O	Radio output power level	Maximum gain	-1	0	1	dBm
INL/DNL	ADC integral/differential non-linearity		-2		2	LSB

Ordering Information

Part number	Package	Size (mm)	Shipment	Pack Quantity
DA14681-01000U22	WL-CSP53	3.406 x 3.010 x 0.5	Reel	100/1000/5000
DA14681-01000A92	AQFN60	6 x 6 x 0.9	Reel	100/1000/4000

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