89HP0608S 1.5Gbps to 6Gbps SAS/SATA Signal Repeater

Integrated Device Technology

FEATURES

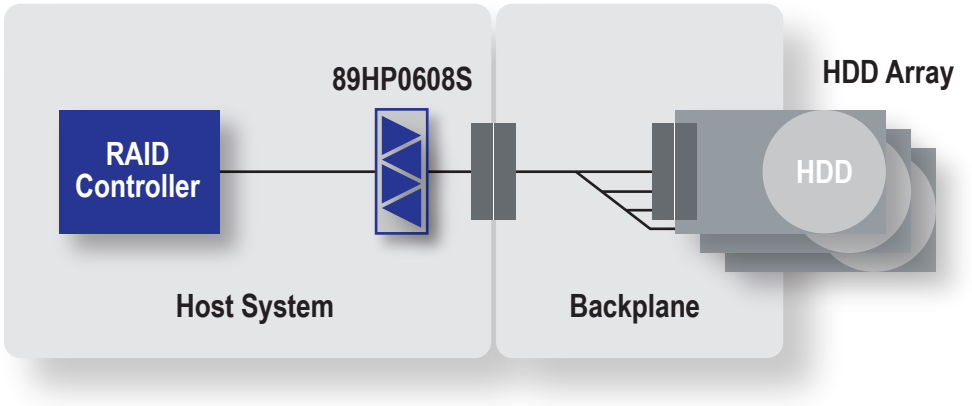
- Compensates for cable and PCB trace attenuation and ISI jitter
- Programmable receiver equalization up to 30dB
- Programmable de-emphasis up to -8.5dB
- Recovers data stream even when the differential signal eye is completely closed due to trace attenuation and ISI jitter
- Full SAS/SATA protocol and Out-of-Band (OOB) support
- Configurable via external pins, while extended programming ranges are available via I^2C interface
- Supports automatic download of configuration from external EEPROM with a single or multiple repeaters on I^2C bus
- Leading edge power minimization in active and shutdown modes
- No external bias resistors or reference clocks required
- Channel mux mode, demux mode, 1 to 2 channels multicast, and Z-switch function mode
- Available in a 9x9mm 100-ball FPBGA package

BENEFITS

- Extends maximum cable length to over 10 meters and trace length over 65 inches in SAS/SATA applications
- Speeds up design time by allowing usage of longer trace and cable lengths
- Minimizes BER

APPLICATIONS

- Blade servers, rack servers
- SAS/SATA instrumentation
- Storage systems
- Cabled SAS/SATA devices



Device Overview

The IDT 89HP0608S is a 1.5Gbps to 6Gbps Repeater IC featuring IDT EyeBoost™ technology that compensates for cable and board trace attenuations and ISI jitter, thereby extending connection reach. The 89HP0608S contains eight half-duplex data channels. Each channel consists of an input equalizer and amplifier, signal detection with glitch filter, as well as programmable output swing, slew rate, and de-emphasis with delay control. Since all of these features are user programmable, they allow for application specific optimization.

Besides the per channel programmable features, the 89HP0608S provides global programmable settings - termination resistance values and transfer modes.

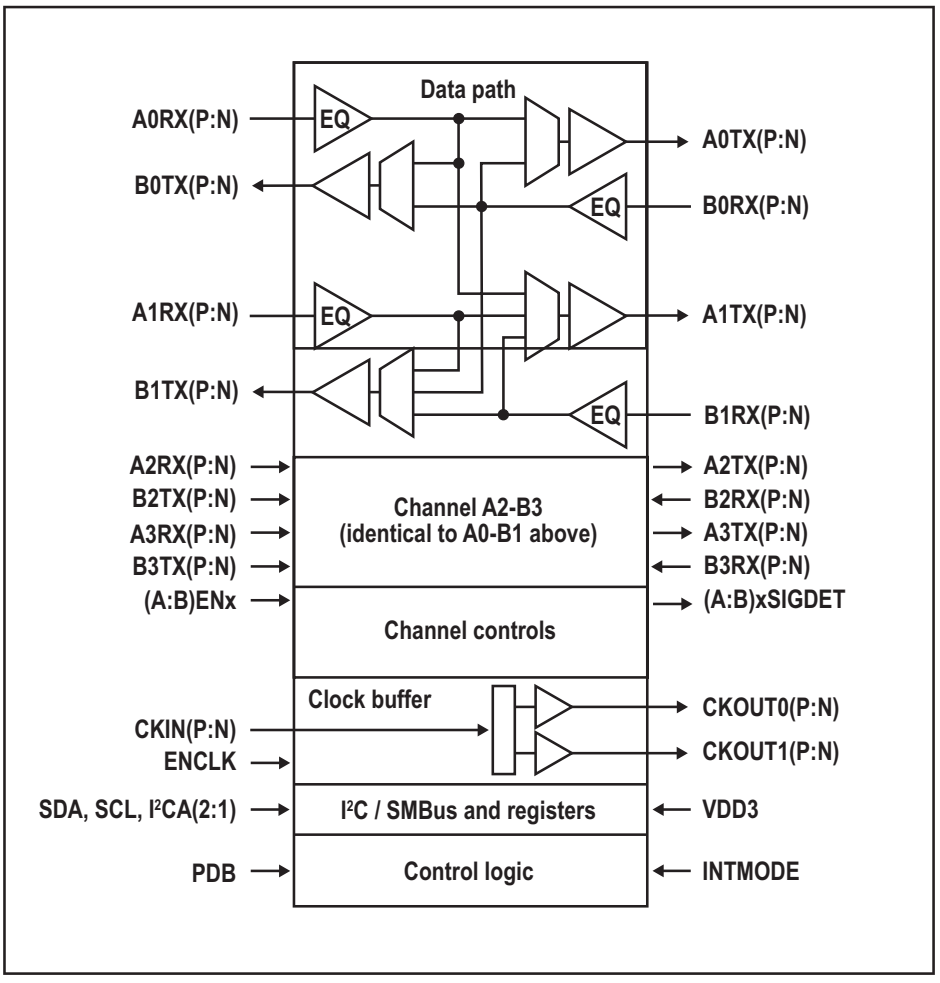
The 89HP0608S, with its many programmable receiver and transmitter features, is ideal for the needs of SAS/SATA applications.

All modes of active data transfer are designed with minimized power consumption. Also, a wide selection of power reducing modes allows the user to eliminate power of unused blocks. In full shutdown mode, the part consumes less than 80mW in worst case environmental conditions.

89HP0608S Block Diagram

The 89HP0608S contains eight high speed channels. Each channel can routed to different outputs. Depending on user configuration via mode selections, input traffic can be muxed, demuxed, or looped back. To facilitate buffering of system clocks, the repeater provides 1:2 clock buffer as shown in the figure below. Powerdown (PDB) and channel enable input pins (A0EN, etc.) are provided for easy state and channel control. Status output pins are available for monitoring critical states, such as the detection of high speed input signals (A0SIGDET, etc.).

Each channel's configuration and performance can be optimized via programming pins or via the I²C interface (SCL, SDA, A0-A2). The programming option allows the user to optimize the repeater's performance in a wide range of applications, making it an ideal solution for most applications requiring cancellation of trace or cable attenuation and ISI jitter.



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