Rapid Charge™ AC/DC Digital Quasi-Resonant PWM Controller with High Resolution Voltage/Current Control

1 Description

The iW1781 is a high performance AC/DC power supply controller for rapid charge that uses digital control technology to build peak-current mode PWM flyback power supplies. The device operates in quasi-resonant mode to provide high efficiency and a number of key built-in protection features. The iW1781 can achieve tight multi-level constant voltage and multi-level constant current regulation without a traditional secondary-feedback circuit. It also eliminates the need for loop compensation components while maintaining stability over all operating conditions.

The iW1781 supports USB Power Delivery (USB PD) and other proprietary rapid charging protocols with secondary-to-primary digital communication handled by secondary-side rapid charge interface circuits, including third party ICs. The iW1781 is optimized to work with Dialog's iW657P USB PD controller and other rapid charge protocol ICs for AC/DC adapters, to achieve fast and smooth voltage transition upon request by mobile devices (MD). When paired with the iW657P, the iW1781 eliminates the discrete decoders on the primary side, minimizes the external component count and simplifies system designs. The iW657P can communicate with the iW1781 through one optocoupler for all the necessary rapid charge information including output voltage requests, output current limits, output voltage undershoot and output over-voltage.

The iW1781 also has a product option which offers Dialog's exclusive **SmartGrouping** control to provide a predictable frequency spectrum for mobile devices with highly sensitive touch panels. **SmartGrouping** technology provides two-dimensional control of both the grouping size and grouping frequency with switching events at a fixed frequency inside the group.

Dialog's innovative proprietary technology ensures that power adapters designed with the iW657P and iW1781 can provide multiple levels of output voltage and constant current limit negotiated by MDs. Furthermore, the chipset can achieve <20mW no-load power consumption at 5V/3A output setting and fast dynamic load response in typical AC/DC rapid charge adapter designs.

2 Features

- Support USB PD, optional QC2.0/3.0 and other proprietary rapid charge protocols with secondary-side interface circuits

- Pairs with iW657P to provide optimized USB PD solutions

- Support multi-level V_{BUS} from 3V to 20V in 25mV increments with multi-level current limits

- Proprietary secondary-to-primary digital communication with single optocoupler for all the rapid charge information:

  - » Output voltage request

  - » Output current limit

  - » Output voltage undershoot detection for fast dynamic load response

  - » Over-voltage protection

- Tight multi-level constant-voltage and multi-level constant-current regulation with primary-side feedback and control

- Ultra-low no-load power consumption with lowest system cost (<20mW at 230V_{AC} with typical 5V/3A setting)

- No audible noise over entire operating range

- Proprietary optimized load adaptive maximum constant frequency PWM switching with quasi-resonant operation achieves best size, efficiency, and common mode noise

- Multi-mode PWM/PFM control improves efficiency at various load conditions

- Optional **SmartGrouping** control provides a predictable frequency spectrum for mobile devices with highly sensitive touch panels

- User-configurable 4-level cable drop compensation independent of output voltage

- **EZ-EMI™** design enhances manufacturability

- Built-in single-point fault protections against output short-circuit including soft short and half short, output over-voltage, and output over-current

- **SmartDefender™** smart hiccup technology helps address issues of soft shorts in cables and connectors by effectively reducing the average output power at fault conditions without latch

- User-configurable external shutdown control

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3 Applications

- Rapid charge AC/DC power adapter for smart phones, tablets and other MDs equipped with USB PD, direct charge and other protocols
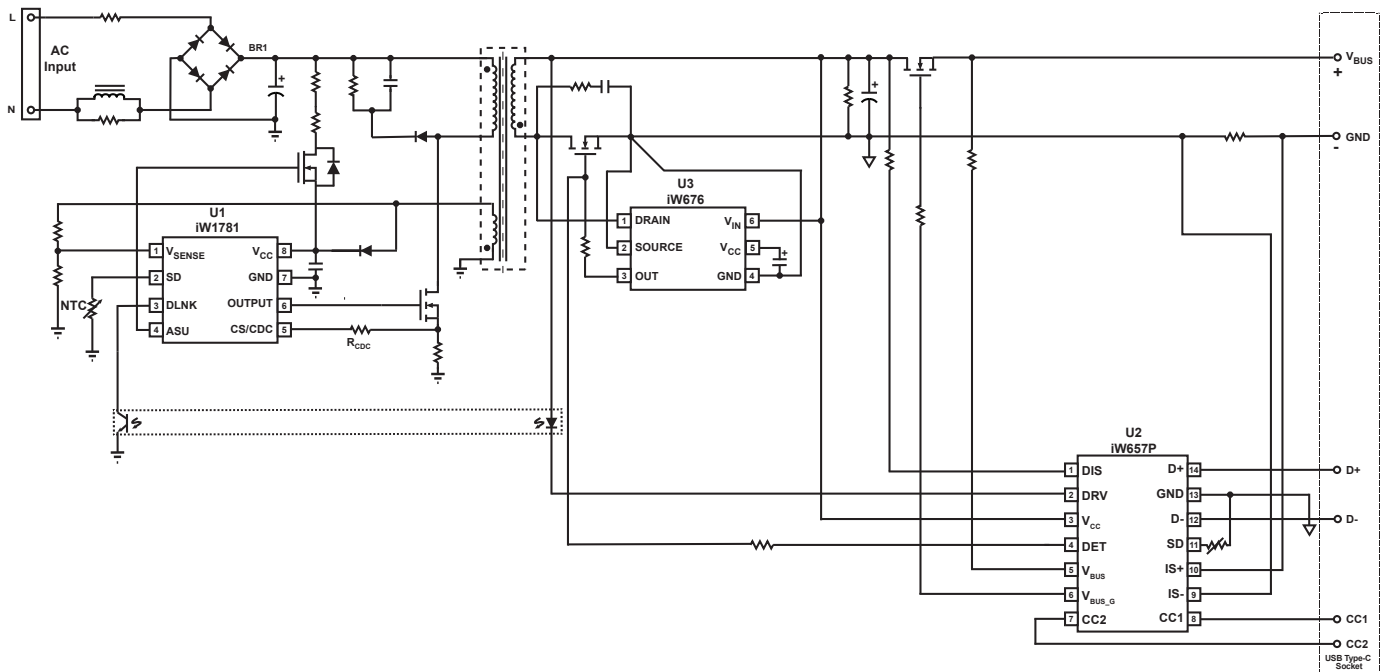
Figure 2.1 : iW1781 typical application circuit for standard USB PD with optional QC2.0/QC3.0 enabled (Using iW657P as Secondary-Side Controller for USB PD and iW676 as Synchronous Rectifier Controller.)

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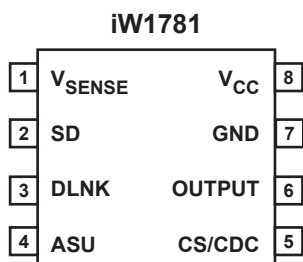
4 Pinout Description

iW1781

1	V_{SENSE}	V_{CC}	8
2	SD	GND	7
3	DLNK	OUTPUT	6
4	ASU	CS/CDC	5

Figure 4.1 : 8-Lead SOIC-8 Package

Pin Number	Pin Name	Type	Pin Description
1	V_{SENSE}	Analog Input	Auxiliary voltage sense. Used for primary-side regulation.
2	SD	Analog Input	External shutdown control. Can be configured for external over-temperature protection (OTP) by connecting an NTC resistor from this pin to Ground.
3	DLNK	Analog Input	Digital communication link signal. Used for secondary-side to primary-side communication for all rapid change information, which includes output voltage requests, output current limits, output voltage undershoot, and over-voltage protection.
4	ASU	Output	Control signal. Used for active start-up device (BJT or depletion mode N-FET).
5	CS/CDC	Analog Input	Primary-side current sense and external cable drop compensation (CDC). Used for cycle-by-cycle peak-current control and limit in primary-side CV/CC regulation. Also used for CDC configuration.
6	OUTPUT	Output	Gate drive for external MOSFET switch.
7	GND	Ground	Ground
8	V_{CC}	Power Input	IC power supply.

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5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to the Electrical Characteristics section.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 8, I_{CC} = 20mA max)	V_{CC}	-0.3 to 25.0	V
Continuous DC supply current at V_{CC} pin (V_{CC} = 15V)	I_{CC}	20	mA
ASU output (pin 4)		-0.3 to 19.0	V
OUTPUT (pin 6)		-0.3 to 20.0	V
V_{SENSE} input (pin 1, I_{VSENSE} ≤ 10mA)		-0.7 to 10.0	V
CS/CDC input (pin 5)		-0.3 to 4.0	V
SD (pin 2)		-0.3 to 4.0	V
DLNK (pin 3)		-0.3 to 4.0	V
Maximum junction temperature	T_{JMAX}	150	°C
Operating junction temperature	T_{JOPT}	-40 to 150	°C
Storage temperature	T_{STG}	-65 to 150	°C
Thermal resistance junction-to-ambient	θ_{JA}	160	°C/W
ESD rating per JEDEC ESD rating per JEDEC JS-001-2017		±2,000	V
Latch-up test per JESD78E		±100	mA

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6 Physical Dimensions
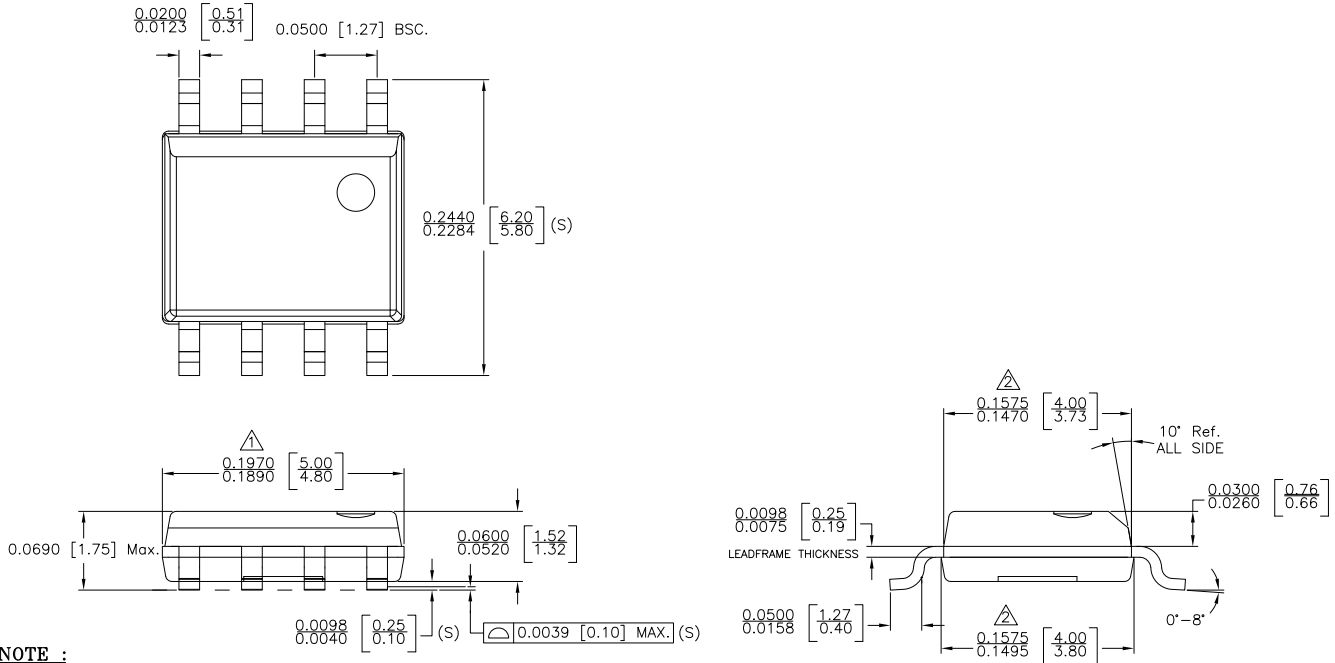
NOTE :

⚠1 DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT
   EXCEED .006 INCH PER SIDE.
⚠2 DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS.
   INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT
   EXCEED .010 INCH PER SIDE.
3. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MS-012.
4. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED
   AS SPECIAL CHARACTERISTIC.(S)
5. CONTROLLING DIMENSIONS IN INCHES. [mm]

STATUS: RELEASED	SCALE: DO NOT SCALE
TERMINAL FINISH: 100% Sn or NiPdAu (PPF)	
TITLE: 8 SOIC PACKAGE OUTLINE	
REV: A	REVISION NOTE: NEW DRAWING	DATE: 02-MAR-2015

7 Ordering Information

Part Number	Options						Package	Description
	Protocol Supported	Default k_{CC} at Start-up	CC Shutdown Voltage	V_{BUS} Resolution	Latch Conditions	CV Operation Modes		
iW1781-00	USB PD and other protocols	0.263	66% of V_{BUS}	25mV/step	N/A	PWM/PFM	SOIC-8	Tape & Reel[1]
iW1781-21	USB PD and other protocols	0.263	No CC Operation	25mV/step	OVP/OTP	PWM/PFM	SOIC-8	Tape & Reel[1]
iW1781-30	USB PD and other protocols	0.263	3V for V_{BUS} < 9V 6.5V for 9V ≤ V_{BUS} < 12V 10V for V_{BUS} ≥ 12V	25mV/step	N/A	PWM/*Smart-Grouping*/PFM	SOIC-8	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 2,500/reel. Minimum packing quantity is 2,500.

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Trademarks

Product Summary   **Rev. 0.4 Preliminary**   **26-Jan-2022**