

1 Description

The iW3623 is a high-performance AC/DC off-line power supply controller for LED luminaires. The iW3623 combines power factor correction and LED current regulation into one controller. It achieves PF > 0.95 and THD < 10% for $100-277V_{AC}$ input voltage range.

over all operating conditions without the need for loop compensation components.

The iW3623 operates in quasi-resonant mode to provide high efficiency. The device uses Dialog's advanced *PrimAccurate*™ primary-side sensing technology to achieve excellent line and load regulation without a secondary-feedback circuit. In addition, the iW3623's pulse-by-pulse waveform analysis technology allows accurate LED current regulation. The iW3623 maintains stability



2 Features

- Isolated AC/DC off-line LED driver
- Power factor > 0.95 for wide input voltage range $100 - 277V_{AC}$
- Total harmonic distortion (THD) < 10%
- Under 5% 100Hz/120Hz output current ripple
- Resonant control to achieve high efficiency
- LED current foldback with external NTC
- Small size design
 - Small size input bulk capacitor
 - Small size output capacitor
 - Small transformer

- *PrimAccurate*™ primary-side sensing eliminates the need for optocoupler feedback and simplifies design
- Tight LED current regulation ± 5%
- Under 0.5 second start-up time
- Hot-plug LED module support
- Multiple protection features:
 - » LED open circuit protection
 - Single-fault protection
 - Over-current protection
 - LED short-circuit protection
 - Current sense-resistor-short-circuit protection
 - Input over-voltage and brown-out protection

3 Applications

- Non-dimmable LED lamps and luminaires
- Optimized for up to 45W output power





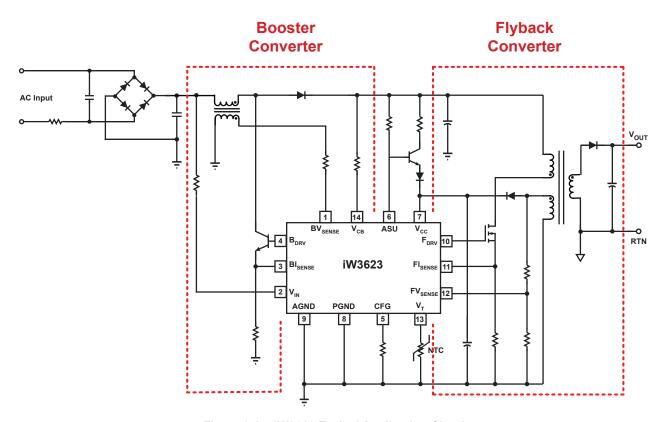


Figure 3.1: iW3623 Typical Application Circuit



4 Pinout Description

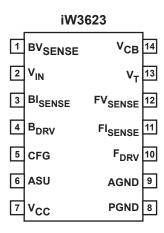


Figure 4.1: 14-Lead SOIC Package

Pin Number	Pin Name	Туре	Pin Description
1	BV _{SENSE}	Analog Input	Boost inductor voltage feedback
2	V _{IN}	Analog Input	Rectified AC line voltage feedback
3	BI _{SENSE}	Analog Input	Boost current sense (used for cycle-by-cycle peak current limit)
4	B _{DRV}	Output	Base drive for boost BJT
5	CFG	Analog In/Out	Chooses input start-up voltage and brown-out shutdown voltage
6	ASU	Output	Active start-up control
7	V _{cc}	Power	Power supply for control logic and voltage sense for power-on reset circuitry. A decoupling capacitor of $0.1\mu F$ or so should be connected between the V_{CC} pin and GND.
8	PGND	Ground	Power ground
9	AGND	Ground	Signal ground
10	F _{DRV}	Output	Gate drive for flyback MOSFET
11	FI _{SENSE}	Analog Input	Primary current sense (used for cycle-by-cycle peak current control and limit)
12	FV _{SENSE}	Analog Input	Auxiliary voltage sense (used for primary-side regulation and ZVS)
13	V _T	Analog Input	Output power limit and shutdown control
14	V _{CB}	Analog Input	Boost output voltage feedback



5 Absolute Maximum Ratings

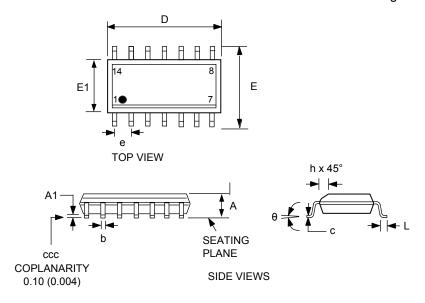
Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 7)	V _{cc}	-0.3 to 18	V
F _{DRV} output (pin 10)		-0.3 to 18	V
B _{DRV} output (pin 4)		-0.3 to 4.0	V
CFG input (pin 5)		-0.3 to 4.0	V
CFG output (pin 5)		-0.3 to 18	V
FV _{SENSE} input (pin 12, I ≤ 10mA)		-0.7 to 4.0	V
BV _{SENSE} input (pin 1, I ≤ 3mA)		-0.7 to 4.0	V
V _{IN} input (pin 2)		-0.3 to 18	V
V _{CB} input (pin 14)		-0.3 to 18	V
FI _{SENSE} input (pin 11)		-0.3 to 4.0	V
BI _{SENSE} input (pin 3)		-0.3 to 4.0	V
ASU output (pin 6)		-0.3 to 18	V
V _T input (pin 13)		-0.3 to 4.0	V
Maximum junction temperature	T _{JMAX}	150	°C
Operating junction temperature	T _{JOPT}	-40 to 150	°C
Storage temperature	T _{STG}	-65 to 150	°C
Thermal Resistance Junction-to-PCB Board Surface Temperature	ΨЈВ	45	°C/W
ESD rating per JEDEC JESD22-A114		±2,000	V
Latch-up test per JESD78A		±100	mA



6 Physical Dimensions

14-Lead SOIC Package



ο	Inc	hes	Millimeters		
Symbol					
တ	MIN	MAX	MIN	MAX	
Α	0.053	0.069	1.35	1.75	
A1	0.004	0.010	0.10	0.25	
b	0.013	0.020	0.33	0.51	
С	0.007	0.010	0.19	0.25	
D	0.337	0.344	8.55	8.75	
E1	0.150	0.157	3.80	4.00	
Е	0.228	0.244	5.80	6.20	
е	0.050 BSC		1.27 BSC		
L	0.016	0.050	0.40	1.27	
h	0.010	0.020	0.25	0.50	
θ	0°	8°	0°	8°	
ССС	0.0	04	0.10		

Compliant to JEDEC Standard MS12F

Controlling dimensions are in inches; millimeter dimensions are for reference only

This product is RoHS compliant and Halide free.

Soldering Temperature Resistance:

- [a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1
- [b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; package can withstand 10 s immersion < 260°C

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.

The package top may be smaller than the package bottom. Dimensions D and E are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.

Figure 6.1: 14-Lead SOIC Package

7 Ordering Information

Part no.	Options	Package	Description
iW3623-0		SOIC-14	Tape & Reel ¹

Note 1: Tape & Reel packing quantity is 2,500/reel. Minimum ordering quantity is 2,500.



IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

© 2024 Renesas Electronics Corporation. All rights reserved.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu Koto-ku, Tokyo 135-0061, Japan www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/

Product Summary Rev. 1.8 12-Jun-2024