

8-Channel LED Driver for LCD Panel Backlighting

1.0 Features

- Fully integrated power FET with minimum external components
- Patented BroadLED™ adaptive switch mode technology for high current matching at maximum efficiency.
 - » Current matching accuracy $\pm 2\%$
 - » Enables use of cheaper, loosely binned LED arrays for lower BOM cost
- 8-channel output each at 65V with 9V to 28V input supply voltage range
- Serial Peripheral Interface (SPI) compatible for high bandwidth PWM-based dynamic local dimming
- LED failure (open and short-circuit) detection
- Supports V_{SYNC} range 50-480Hz
- Integrated DC-DC boost controller
 - » 10V gate drive voltage
 - » Programmable switching frequency from 100KHz to 200KHz.
 - » Internal soft start to limit the in-rush current
- PWM dimming range from 0% to 99.9% with 12-bit resolution
- PLL locked V_{SYNC} and synchronized PWM
- Supports one-pin global direct PWM with phase shift
- Comprehensive protection features
 - » LED open fault detection
 - » Single-pin, resistor programmable LED short level (3V/6V/9V/12V) fault detection
 - » Over-temperature shutdown
 - » Boost controller output OCP, OVP and UV protection
 - » Boost input UVLO (Hys.=110mV) protection
- QFP44 supports 230mA/channel and SOP32 supports 175mA/channel within 50 degree temperature rise on Dialog EVB.
- Packages include: QFP44 with 10mm x 10mm body at 0.8mm pitch, SOP32 with 10.4mm x 20.74mm at 1.27mm pitch
- Pin-out optimized for single-layer PCB layout
- Green & Pb-free (RoHS compliant) BOM

2.0 Description

The iW7019 is a high efficiency driver for LEDs. It fully integrates one internal step-up PWM DC-DC converter to drive up to 8 separate strings of multiple series-connected LEDs.

Users can provide versatile configurations of the iW7019 through SPI interface registers.

The iW7019 can maintain very high efficiency even with the existence of LED channel total forward voltage mismatch, with the proprietary digital power management and patent pending adaptive switch (BroadLED™) mode LED current regulation technology.

The iW7019 has multiple features to protect the LED channels from fault conditions, and these protections are LED PWM cycle-by-cycle based to ensure system reliability and provide consistent operation.

3.0 Applications

- Direct & segment-edge LED backlit LCD TV
- Edge type global dimming LED backlit LCD TV

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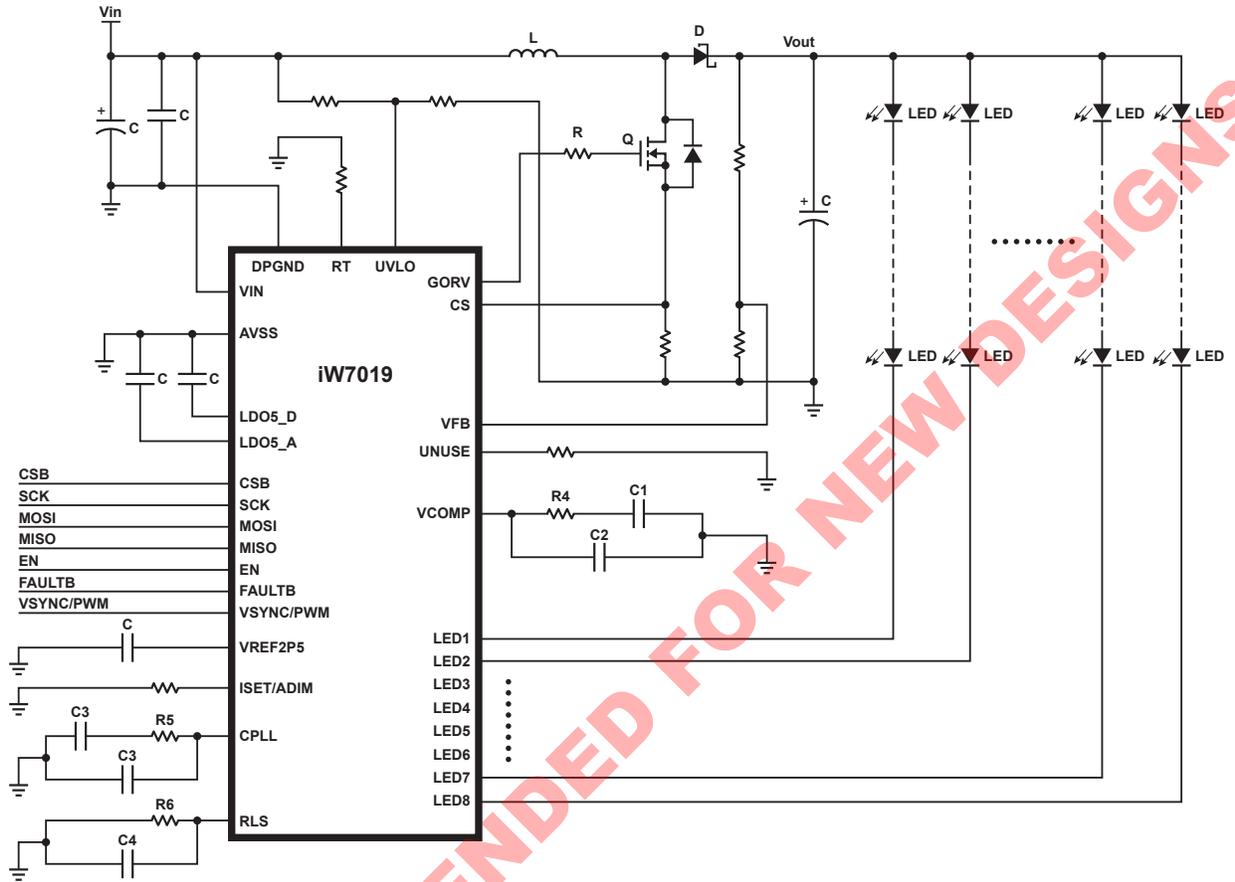


Figure 3.1 : iW7019 Application Diagram

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4.0 Pinout Description

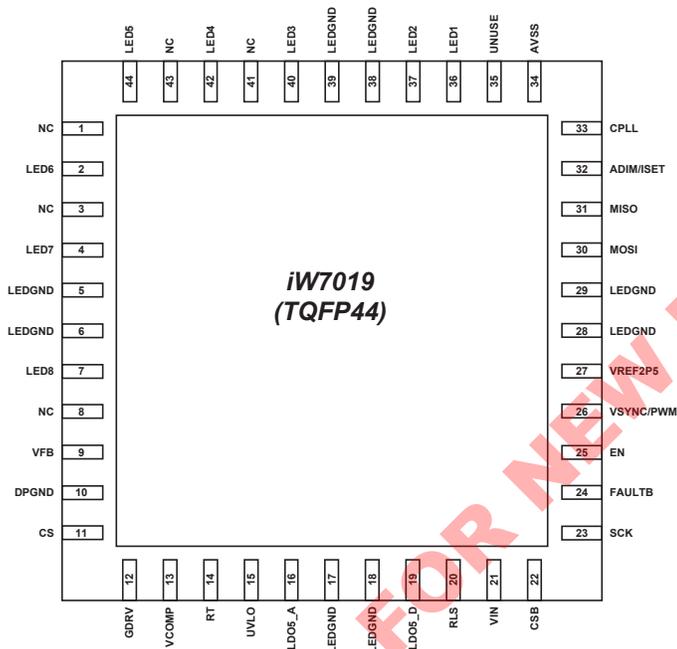


Figure 3.2 : Pin Configuration for TQFP44 Package

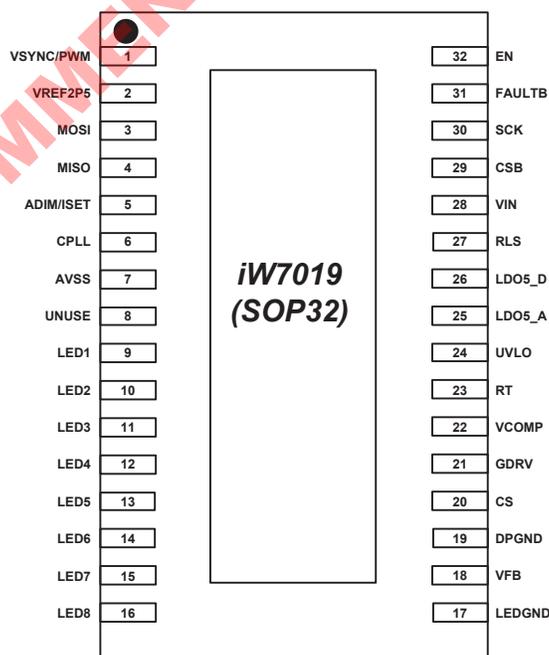


Figure 3.3 : Pin Configuration for SOP32 Package

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Pinout Description (continued)

Pin # QFP44	Pin # SOP32	Name	Type	Pin Description
1	X	NC		
2	14	LED6	Analog Output	LED cathode connection for string 6
3	XX	NC		
4	15	LED7	Analog Output	LED cathode connection for string 7
5	17	LEDGND	Ground	Ground for LED driver
6	17	LEDGND	Ground	Ground for LED driver
7	16	LED8	Analog Output	LED cathode connection for string 8
8	X	NC		
9	18	VFB	Analog In	Boost controller feedback pin (settled value is 1.2V)
10	19	DPGND	Digital Ground	Digital Ground and Boost Pre-Driver's ground
11	20	CS	Analog In/Out	Boost pre-driver sense input
12	21	GDRV	Analog Out	Boost gate drive for external MOSFET
13	22	VCOMP	Analog In	Boost controller loop compensation
14	23	RT	Analog In	Programmable boost switching frequency (100K/150K/200K)
15	24	UVLO	Analog In	Boost UVLO comparator input. Voltage level is greater than 1.2V for a healthy boost VIN. Customer has to put resistor divider on
16	25	LDO5_A	Analog Output	Internal LDO output and analog power section supply.
17	17	LEDGND	Ground	Ground for LED driver
18	17	LEDGND	Ground	Ground for LED driver
19	26	LDO5_D	Analog Output	Internal LDO output and digital power section supply.
20	27	RLS	Analog Input	Short Level Threshold voltage setting(3/6/9V/12V, with default at 6V), using different resistor selection.
21	28	VIN	Supply Input	Input voltage to the main supply rail.
22	29	CSB	Digital Input	Slave select input for SPI (Chip Select Bar). Active LOW. Logic high is defined as 5.0V
23	30	SCK	Digital Input	SCK, serial clock input for Serial Peripheral Interface (SPI). Logic high is defined as 5.0V.
24	31	FAULTB	Analog Output	Fault status (Active Low) - Open drain. Pull-up to LDO5A with a 100KOhm +5% resistor.
25	32	EN	Digital Input	Enable Input. Logic high is defined as 5.0V.
26	1	VSYNC/PWM	Digital Input	Vertical SYNC input. [optional direct PWM control] logic high is defined as 5.0V.
27	2	VREF2P5	Analog Output	Analog reference for Analog Dimming.

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Pinout Description (continued)

Pin # QFP44	Pin # SOP32	Name	Type	Pin Description
28	17	LEDGND	Ground	Ground for LED driver
29	17	LEDGND	Ground	Ground for LED driver
30	3	MOSI	Digital Input	Master output, slave input for SPI.
31	4	MISO	Digital 3 Stat Output	Master input, slave output for SPI. Logic high is defined as 3.3V.
32	5	ADIM/ISET	Analog In	Dedicate Current setting / Analog dimming input
33	6	CPLL	Analog In/Out	PLL compensation output / External Clock In
34	7	AVSS	Ground	Quiet analog ground.
35	8	UNUSE	Analog Input	Set unused channel number.
36	9	LED1	Analog Output	LED cathode connection for string 1
37	10	LED2	Analog Output	LED cathode connection for string 2
38	17	LEDGND	Ground	Ground for LED driver
39	17	LEDGND	Ground	Ground for LED driver
40	11	LED3	Analog Output	LED cathode connection for string 3
41	X	NC		
42	12	LED4	Analog Output	LED cathode connection for string 4
43	X	NC		
44	13	LED5	Analog Output	LED cathode connection for string 5
		EXPGND	Ground	Exposed PAD for LED driver

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5.0 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded.

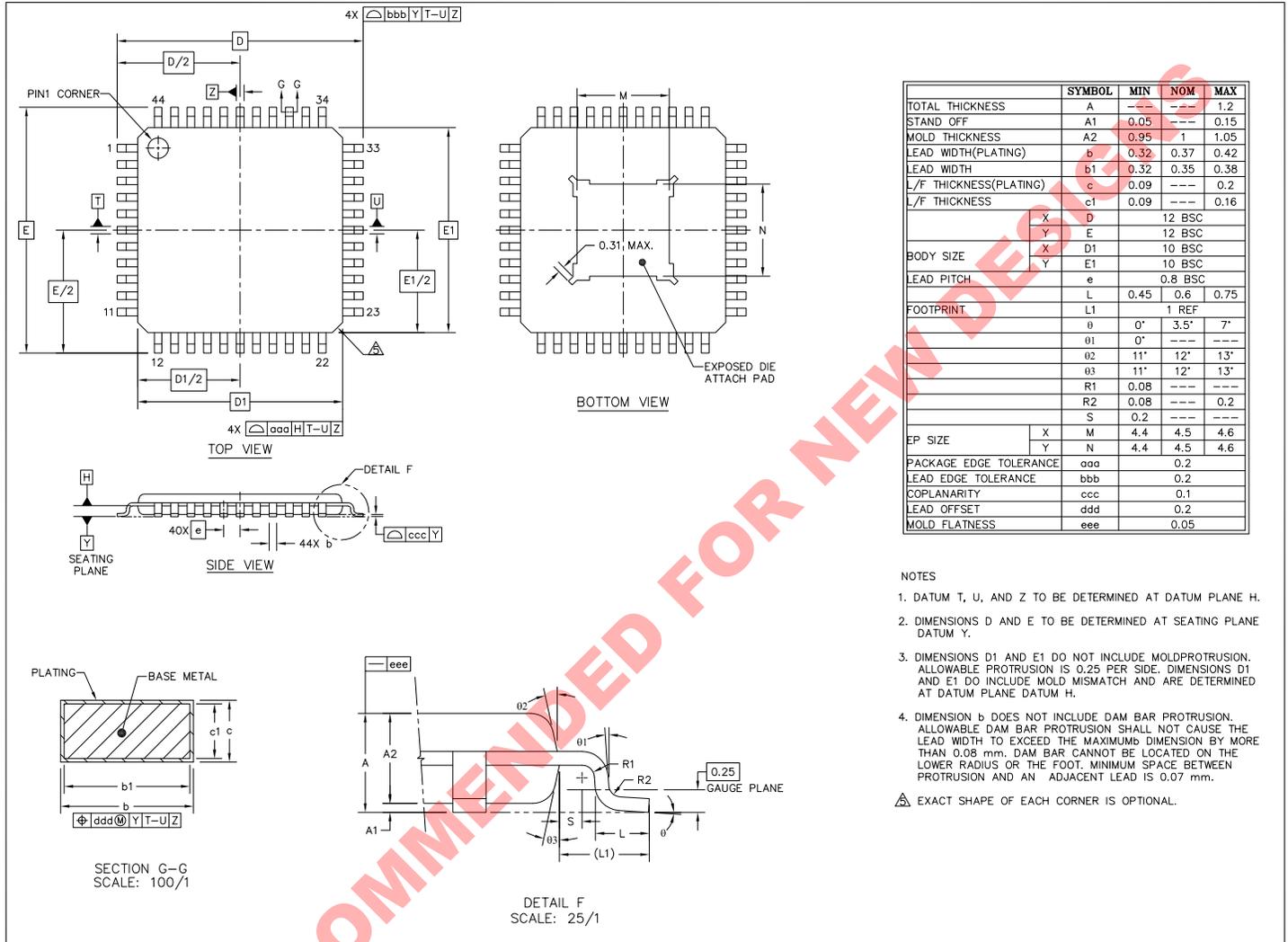
Parameter	Symbol	Value	Units
V_{IN} supply voltage	V_{IN}	-0.3 to 40	V
LDO5 output voltage	V_{LDO5}	-0.3 to 7	V
AGND / AVSS / GNDn to GND		-0.3 to 0.3	V
LEDn voltage	V_{LEDn}	-0.3 to 65	V
Logic I/O pins (SCK, MISO, MOSI, CSB, & VSYNC)		-0.3 to 7	V
Voltage on all other pins except for LEDn pins		-0.3 to 7	V
Power dissipation at $T_A \leq 25^\circ\text{C}$	P_D	TBD	mW
Maximum operating junction temperature	T_{JMAX}	-40 to 150	$^\circ\text{C}$
Storage temperature	T_{STG}	-40 to 150	$^\circ\text{C}$
Lead temperature during IR reflow for ≤ 15 seconds	T_{LEAD}	270	$^\circ\text{C}$
Latch-up current		>100	mA
ESD rating per JEDEC JESD22-A114 - HBM		$\pm 2,000$	V

6.0 Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{IN} supply voltage (V_{IN})	9		28	V
LEDn voltage	0.5		65	V
Thermal Resistance Junction (θ_{JA}): SOP32		69.2		$^\circ\text{C}/\text{W}$
Thermal Resistance Junction (θ_{JA}): TQFP44		41.5		$^\circ\text{C}/\text{W}$
Junction Temperature (T_J)	-40		150	$^\circ\text{C}$
Operate Temperature ($C_{operate}$)	-40		85	$^\circ\text{C}$

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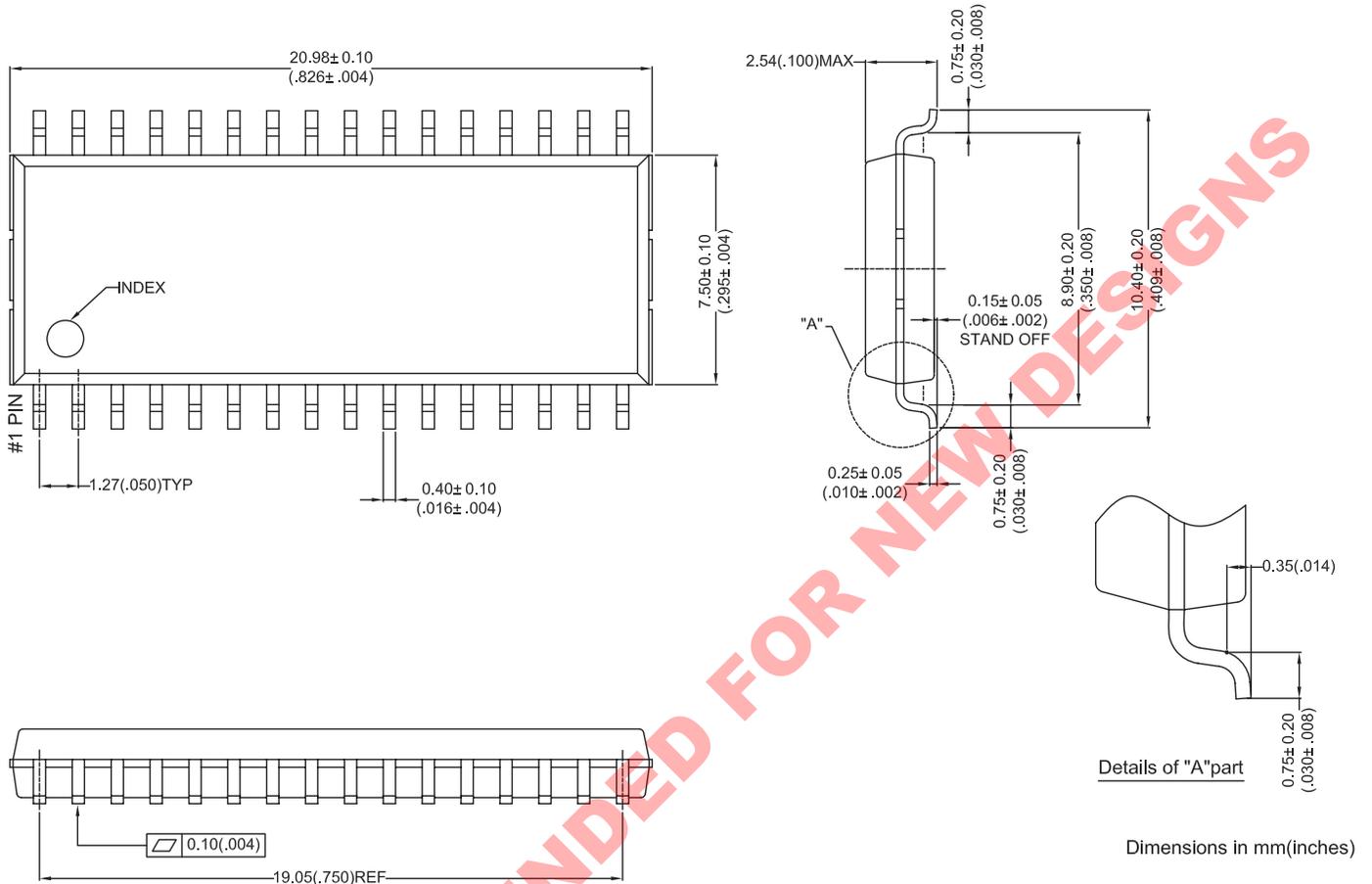
7.0 Physical Dimensions



- NOTES
- DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
 - DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
 - DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
 - DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.
- △ EXACT SHAPE OF EACH CORNER IS OPTIONAL.

Figure 7.1 : Physical Dimensions, TQFP-44 Package

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This product is RoHS compliant and Halide free. Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 3

Figure 7.2 : Physical Dimensions, SOP-32 Package.

8.0 Ordering Information

Part Number	Package	Description
iW7019-00-TQ2E	TQFPEP-10mm-44L	Tape & Reel ¹
iW7019-00-SO32	SOP300-32	Tape & Reel ²

Note 1: Tape & Reel packing quantity is 1,250/reel. Minimum ordering quantity is 1,250.

Note 2: Tape & Reel packing quantity is 1,000/reel. Minimum ordering quantity is 1,000.

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