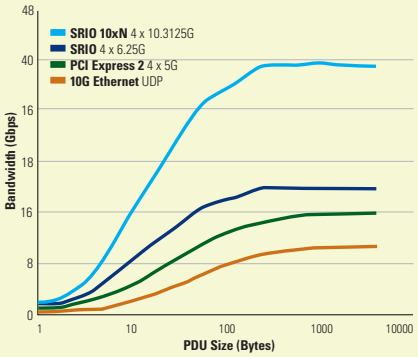
RapidIO® Interconnect for Servers and Supercomputing

RAPIDIO FOR SERVER AND SUPERCOMPUTING

- **Scalability**
  - Peer-to-peer, "any-to-any" topologies from 1Gbps to 20 Gbps with native processor interface
  - Mesh, star, dual star, hypercube, etc.
  - Scales to 64k processing nodes, 66 bit memory addressing
  - 3-layer protocol terminated in hardware with no software intervention
  - Direct processor interface up to 20 Gbps with NO NIC
  - Smallest form factor with 1/10th footprint per Gflop in ARM based server vs. x 86 with Ethernet NIC.
- **Latency**
  - 100 ns cut through latency for switches
  - End-to-end sub microsecond packet termination latency with reliable transmission, orders of magnitude better than ethernet
- **Power**
  - Typical power approximately 300 mW per 10 Gbps in switch
  - No additional power from NICs meaning approximately 1/10th the power required for scale out with Ethernet systems requiring NICs
  - Lowest power per payload bit vs. other interconnect protocols

PROTOCOL COMPARISON



Up to 20 Gbps per port with native processor interface

- Highest protocol efficiency in embedded systems with 94% payload versus header efficiency
- Serial RapidIO standard supports arbitrary system topology with true peer-to-peer networking
- Twice the performance per link compared to 10 Gb Ethernet
- RapidIO messaging support for transfers of large blocks of data, superior to PCIe and 10 GbE in target applications

RapidIO for Multi Processor Systems

RapidIO is the interconnect that was developed for peer-to-peer inter-processor communication between devices on a board, between boards across a backplane and between chassis through cabling. RapidIO is optimized for low latency, low power interconnect in embedded systems where thousands of processors need to communicate in a system with "any-to-any" traffic. RapidIO's largest market was in wireless bases station where it is used to connect large number of processing nodes with up to 20 Gbps interconnect directly on processors without NICs, adaptors and software intervention. This provides a uniform interconnect inside the system in very tight small form factors. All of these attributes have emerged as major requirements in both servers and supercomputing systems today. RapidIO also addresses the overall energy requirements of both data centers and supercomputing.

RapidIO: the Ideal Scalable Interconnect for Servers and Super Computing

Historically, a server was a computer connected to an ethernet network with network interface controller. Over time this LAN topology was pushed inside the rack with large quantities of processors all connected to a top-of-rack switch through NIC's. This in effect collapses a LAN based topology into a rack, but carries all the drawbacks of the historic architecture. RapidIO has solved the multi processor problem by addressing the interconnect problem from the processor to processor angle rather than the processor to "network" angle. RapidIO-connected servers and supercomputers can use both backplane based and top-of-rack-based switching with latencies as low as 100ns through switches and less than 1 microsecond end-to-end between processing nodes.

The New Wave: X86, ARM and PowerPC based Servers with RapidIO

Servers can be designed with processors from all vendors, either with native RapidIO interface or with external connect with IDT PCIe® to S-RIO bridging devices. ARM and PowerPC based processors are available in the industry with 20 Gbps RapidIO interfaces. This allows for highly dense scalable server systems with low power and small form factors for x86 based RapidIO servers. Supercomputing systems based on RapidIO and ARM processors are leading the industry for energy efficiency with products that are as high as twice the energy efficiency of the top tier of the Green 500.

Interconnect: Scalability-Latency-Hardware Termination

SCALABILITY	LOW LATENCY	HARDWARE TERMINATED	GUARANTEED DELIVERY
Ethernet	PCIe	PCIe	Ethernet in s/w only
RapidIO			

RapidIO interconnect combines the best attributes of PCIe and Ethernet in a multi-processor fabric

RAPIDIO GEN2 FEATURES

- 20 Gbps per port with native Processor interface on integrated SoC's
- 300 mW per 10 Gbps
- 2W for PCIe2 to S-RIO2 NIC
- Production switching and bridging porfolio with over 6 million devices shipped connecting over 30 million processing nodes
- 100ns cut through latency through switches
- Sub microsecond latency for end-to-end transactions
- 100 cm long reach per lane over 2 connector across backplanes @ 6.25 Gbaud
- Top-of-rack scalable RapidIO switch devices available from industry with 20 Gbps per port
- Built-in reliable transmission
- Extensive portfolio of switches and bridging products in production.

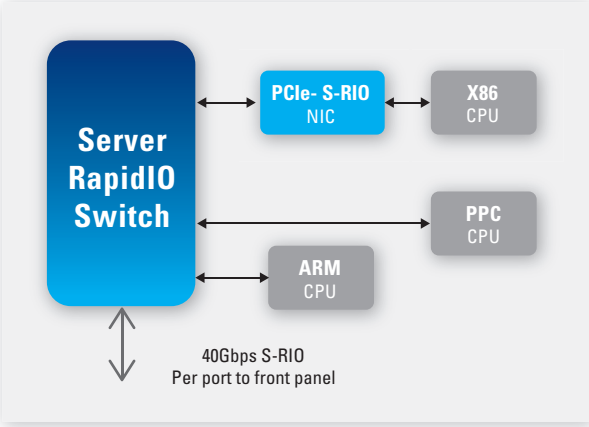
RAPIDIO 10xN TECHNOLOGY ENHANCEMENTS

- 40 Gbps per port with native Processor interface on integrated SoC's
- Large Lane Count 40 Gbps backplane switching
- PCIe 3 to S-RIO 10xN NICs
- 100 cm long reach over 2 connector across backplanes @ 10.3125 Gbaud
- 64/67 encoding for greater efficiency over 8b/10b encoding

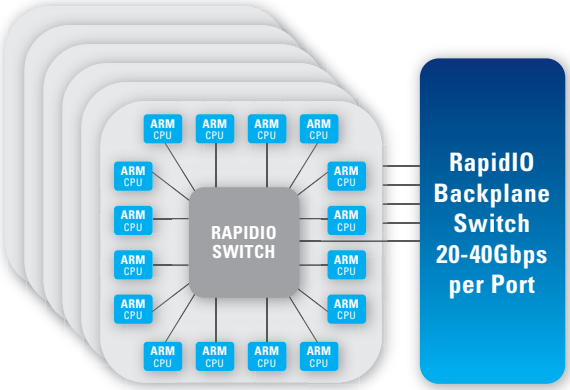
TARGET APPLICATIONS

- Super Computer
- Blade Server
- Micro Server
- Top-of-Rack RapidIO switching
- X86, ARM, PowerPC based servers

Discover what IDT know-how can do for you:
www.IDT.com/go/rapidio

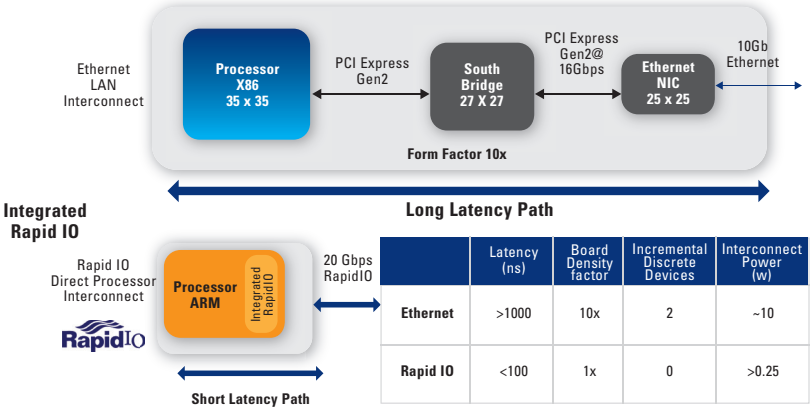


Scalable Server Design with multiple processor options: X86, PowerPC, ARM



ARM based Server with Rapid IO

RapidIO vs. Ethernet Processor Access



	Latency (ns)	Board Density factor	Incremental Discrete Devices	Interconnect Power (w)
Ethernet	>1000	10x	2	~10
Rapid IO	<100	1x	0	>0.25

Footprint, latency, power comparison with x86 + Ethernet Server

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