October 13, 2010

Key Features of Renesas Electronics' new SH7268 and SH7269 MCUs

1. [SH7268]

*Upper Row: Operating Temperature −40~+85℃, Lower Row: Operating Temperature −20~+85℃

Item	Spec	
Product Classification	SH7268	
Product Code*	R5S72680P266FP	R5S72681P266FP
	R5S72680W266FP	R5S72681W266FP
Power Supply Voltage	3.3V/1.25V	
Maximum Operating Frequency	266MHz	
Operating Temperature	−40~+85℃ or −20~+85℃	
CPU Core	SH2A-FPU	
CPU Instruction Number	112 (Including FPU related instructions)	
Built-In RAM	• Large Capacity Memory: 2.5 Mbytes (For Video Display/Work Area, 128KB is shared with data retention area) • High Speed Memory: 64 Kbytes	
Cache Memory	16 Kbytes (Instruction 8K/Operand 8K Separated, 4-way set associative)	
External Memory	Bus Clock Maximum 66.67MHz	
	Direct Connect to SRAM and SDRAM by Bus State Controller	
	Address Space 64 Mbytes × 7	
	Data Bus Width: 8/16/32 bits	
Built-In Peripheral Functions	OpenVG1.1 Compliant 2D Graphics Accelerator	
	Multifunction 16-bit Timer (MTU2) × 5 channels	
	16-bit Timer (CMT) × 2 channels	
	A/D Converter (10-bit resolution) × 6 channels	
	USB 2.0 Compliant (Hi-Speed) Selectable Host or Function	

Item	Spec
	Serial communication interface with FIFO (SCIF) × 8 channels (Clocked synchronous or asynchronous mode selectable)
	I^2C Bus Interface × 2 channels
	Serial Sound Interface × 4 channels
	Renesas SPDIF Interface
	Motor Control PWM Timer × 2 channels
	NAND Flash Interface
	Video Display Controller
	Video Decoder (Direct connect to Analog Composite)
	JPEG Codec Unit
	SD Host Interface (SD Card License required)
	MMC Host Interface
	Real Time Clock
	CD-ROM Decoder
	Sampling Rate Convertor × 3 channels
	IEBus Interface
	– / CAN Interface × 3 channels
	On-chip Debugging Functions • Advanced User Debugger-II (AUD-II) • User Debug Interface (H-UDI) • User Break Controller × 2 channels
	Direct Memory Access Controller × 16 channels
	Sound Generator × 4 channels
	Interrupt Controller
	Watchdog Timer
	Clock Pulse Generator (CPG): Input clock can be multiplied by 20 (max.) by the internal PLL circuit
Boot Modes	Boot Mode0: Booting from memory (bus width: 16 bits) connected to CS0 area

Item	Spec
	Boot Mode1: Booting from memory (bus width: 32 bits) connected to CS0 area
	Boot Mode2: Booting from a NAND flash memory
	Boot Mode3: Booting from a serial flash memory
	Boot Mode4: Booting from a NAND flash memory with SD controller
	Boot Mode5: Booting from a NAND flash memory with MMC controller
Power-down modes	Sleep mode
	Software standby mode
	Deep standby mode
	Module standby mode
Package	208-pin QFP (28mm × 28mm) 0.5mm pitch

2. [SH7269]

*Upper Row: Operating Temperature −40~+85℃, Lower Row: Operating Temperature −20~+85℃

Item	Spec	
Product Classification	SH7269	
Product Code* (QFP Package)	R5S72690P266FP	R5S72691P266FP
	R5S72690W266FP	R5S72691W266FP
Product Code* (BGA Package)	R5S72690P266BG	R5S72691P266BG
	R5S72690W266BG	R5S72691W266BG
Power Supply Voltage	3.3V/1.25V	
Maximum Operating Frequency	266MHz	
Operating Temperature	−40~+85℃ or −20~+85℃	
CPU Core	SH2A-FPU	
CPU Instruction Number	112 (Including FPU related instructions)	
Built-In RAM	• Large Capacity Memory: 2.5 Mbytes (For Video Display/Work Area, 128KB is shared with data retention area)	

Item	Spec
	• High Speed Memory: 64 Kbytes
Cache Memory	16 Kbytes (Instruction 8K/Operand 8K Separated, 4-way set associative)
External Memory	Bus Clock Maximum 66.67MHz
	Direct Connect to SRAM and SDRAM by Bus State Controller
	Address Space 64 Mbytes × 7
	Data Bus Width: 8/16/32 bits
Built-In Peripheral Functions	OpenVG1.1 Compliant 2D Graphics Accelerator
	Multifunction 16-bit Timer (MTU2) × 5 channels
	16-bit Timer (CMT) × 2 channels
	A/D Converter (10-bit resolution) × 8 channels
	USB 2.0 Compliant (Hi-Speed) Selectable Host or Function
	Serial communication interface with FIFO (SCIF) × 8 channels (Clocked synchronous or asynchronous mode selectable)
	Serial I/O with FIFO (SIOF)
	I^2C Bus Interface × 4 channels
	Serial Sound Interface × 6 channels
	Renesas SPDIF Interface
	Motor Control PWM Timer × 2 channels
	NAND Flash Interface
	Video Display Controller
	Video Decoder (Direct connect to Analog Composite)
	JPEG Codec Unit
	SD Host Interface × 2 channels (SD Card License required)
	MMC Host Interface
	Real Time Clock
	CD-ROM Decoder
	Sampling Rate Convertor × 3 channels
	IEBus Interface

Item	Spec	
	–	CAN Interface × 3 channels
	On-chip Debugging Functions • Advanced User Debugger-II (AUD-II) • User Debug Interface (H-UDI) • User Break Controller × 2 channels	
	Direct Memory Access Controller × 16 channels	
	Sound Generator × 4 channels	
	Interrupt Controller	
	Watchdog Timer	
	Clock Pulse Generator (CPG): Input clock can be multiplied by 20 (max.) by the internal PLL circuit	
Boot Modes	Boot Mode0: Booting from memory (bus width: 16 bits) connected to CS0 area	
	Boot Mode1: Booting from memory (bus width: 32 bits) connected to CS0 area	
	Boot Mode2: Booting from a NAND flash memory	
	Boot Mode3: Booting from a serial flash memory	
	Boot Mode4: Booting from a NAND flash memory with SD controller	
	Boot Mode5: Booting from a NAND flash memory with MMC controller	
Power-down modes	Sleep mode	
	Software standby mode	
	Deep standby mode	
	Module standby mode	
Packages	• 256-pin QFP (28mm × 28mm) 0.4mm pitch • 272-pin BGA (17mm × 17mm) 0.8mm pitch	