September 7, 2010

Key Features of Renesas Electronics' New V850E2M MCUs

Product		V850E2/MN4			
		μPD70F3510	μPD70F3512	μPD70F3514	μPD70F3515
CPU	Core	V850E2M		V850E2M × 2	
	Minimum instruction execution time	5ns (during 200MHz operation using internal system clock)			
Internal Memory	Flash memory (MB)	1		1	2
	RAM (KB)	64 + 64 (Low speed)		64 × 2 + 64 (Low speed)	
External Bus interface		Can connect to SRAM/SDRAM separate bus × 2 (Data bus : 32-bit × 2)			
I/O port		Input 7 pins, I/O 181 pins			
Timer	16-bit timer	16 channels × 4 units			
	32-bit timer	4 channels × 1 unit			
	16-bit encode timer	2			
	WDT	1		2	
Serial interface		UART (FIFO) : 4 CSI (FIFO) : 4 UART : 6 CSI : 6 I2C : 6		UART (FIFO) : 4 CSI (FIFO) : 4 UART : 6 CSI : 6 I2C : 6	
			CAN : 2		CAN : 2
A/D converter		10-bit resolution × 12 (The resolution is 12-bit when using a 5.0V A/D converter power supply.)			
DMA controller		16			
Ethernet controller		-	1 (10/100 Base)		

USB controller	USB2.0 Function controller (Full speed): 1 USB2.0 Host controller (Full speed): 1
On chip debug	built-in
Operating Frequency	144M ~ 200MHz (Multiplied by 20 using a PLL)
Operating power supply	VDD = 1.1 ~ 1.3 V EVDD = 3.0 ~ 3.6 V AVDD = 3.0 ~ 3.6 V / 4.5 ~ 5.5 V
Package	304-pin FBGA (19 × 19mm)
Note) The number of channels indicate those that are incorporated in the product. The actual number of channels differs according to the pin count.	