November 12, 2013

Main Specifications of RXv2 Core

	Main Specification
CPU	RXv2
Max Operating Frequency (Target)	300 MHz
Register	• General purpose: Sixteen 32-bit registers • Control: Ten 32-bit registers • Accumulator: Two 72-bit registers
Instruction Set Specification	• 109 instruction sets • Flexible length instruction (1Byte-8Byte) • Supporting 3 operand format
Endian Mode	• Instructions: little endian • Data: Selectable as little or big endian
Address Space	4 GB
Addressing Mode	12 (register–register operations, register–memory operations) (immediate–register operations, immediate–memory operations, memory–memory transfer, and bitwise operations etc.)
FPU	Single precision (32-bit) floating point (Data types and floating-point exceptions in conformance with the IEEE754 standard)
Multiplier	High Speed Multiplier (32 bit × 32 bit = 64 bit)
Divider	High Speed Divider
Product sum Operation	High Speed (32 bit × 32 bit + 80 bit = 80 bit)
Performance (Target)	• Over 2.00 DMIPS/MHz (Dhrystone 2.1) • Over 4.0 Coremark/MHz

	Main Specification
Current Consumption (Target value based on MCU)	Under 0.3 mA/MHz

(Remarks) Other product and service names that appear in this press release are trademarks or registered trademarks of their respective owners.